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BDX-613-2070 (Rev.)

LOGIC CIRCUIT SIMULATION
AND AUTOMATIC FABRICATION

By W. W. Davis

Published February 1979

Final Report

Prepared for the United States Department of Energy
Under Contract Number DE-AC04-76-DP00613.

**Kansas City
Division**

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Printed in the United States of America

Available From the National Technical Information Service, U.S. Department of Commerce, 5285 Port Royal Road, Springfield, Virginia 22161.

Price:	Microfiche	\$3.00
	Paper Copy	\$5.25

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AND AUTOMATIC FABRICATION

By W. W. Davis

Published February 1979

Final Report
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LOGIC CIRCUIT SIMULATION AND AUTOMATIC FABRICATION

BDX-613-2070 (Rev.), Final Report, Published February 1979

Prepared by W. W. Davis

A complete computer-aided system was investigated to assist in performing required digital designs. The system contained graphics, digital simulation, PROM circuit synthesis, and numerical control (N/C) wiring control tape software. Only the N/C wiring software continues to be used; this program will be transferred to a minicomputer.

TWL-TR2/G

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A prime contractor with the United States
Department of Energy under Contract Number
DE-AC04-78-DP00613

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SUMMARY

The purpose of this project was to determine a better method of meeting increased complexity in the circuits necessary to satisfy test equipment digital design requirements. The feasibility of an extensive computer-aided design system was investigated and implementation of this system was attempted on an existing computer system at Bendix Kansas City.

The computer-aided design system was subdivided into four parts.

- The interactive graphics software was generated for layout of circuit design using graphics terminals. The created digital design was computer plotted for documentation.
- Circuit synthesis software was adapted and extensively modified for universal asynchronous PROM applications.
- Digital simulation software was adapted to meet system requirements.
- Circuit fabrication numerical control (N/C) tape was generated for circuit fabrication on the semiautomatic wiring machine.

A comprehensive graphics program was generated with commands for creating lines, rectangles, circles, labels, and a model library. Data base information created in the first could be used by the other software portions and data created by these passed back to the graphics section for documentation. The circuit synthesis program SHIVA was obtained from Auburn University and extensively modified for programmable read only memory (PROM) applications. The simulation program HAL1900 was obtained from Lawrence Livermore Laboratories (LLL) and modified for PROM applications. The circuit fabrication section processed interconnect and placement data to generate the N/C control tape (for a semiautomatic wiring machine) plus associated documentation. Currently, Bendix is saving a substantial amount each month through this portion and at times has experienced nearly eight times the workload originally forecast--27,000 wirewraps per year. Each of these software sections may be used individually.

Interactive graphics, digital simulation, and circuit synthesis merits do not justify the time spent with the computer system. The N/C wiring process remains the most effective means of fabrication in low production quantities. Therefore, the N/C fabrication

tape generating software is the only package being utilized. The N/C tape software will be adapted for minicomputer application at a convenient time in the future.

DISCUSSION

SCOPE AND PURPOSE

The intent of this project was to provide engineers with a computer aid in design and fabrication of a circuit or system. The project used graphics terminals for the advantages of interactive graphics, ease of input, and quick interpretation of graphic output. The engineer would start with a basic functional block diagram and proceed to develop each "block" of the circuit until the design requirements were fulfilled. The circuit would be drawn on the screen using standard symbols from a library. A digital simulation program would generate and display input and output waveforms, confirming the proposed design. When the engineer was satisfied the circuit was correct, a hardcopy of the drawing would be made "on-line". The interconnect information used by the wirewrap program would be used to generate a tape for the numerically controlled (NC) wirewrap machine.

ACTIVITY

The system was divided into four basic sections. Data base information created in the first section would interface to the following three sections; data generated by these sections would pass back to the first for documentation. Each of the sections may be used individually.

Graphics

The graphics section is the interface between the engineer and the computer. Information is conveyed in a form similar to normal design processes. Commands for creating lines, rectangles, circles, labels, arrays of the same, plus rotation, and a model library may be used to create a drawing. A grid may be defined for easy component alignment and a zoom feature may be called upon for detailed work. Move and edit commands provide for continued evolution of designs. Data from a completed design is used for final drawing on the plotter. Data may be retrieved and modified indefinitely as required. Special graphics options provide outputs for hybrid microcircuits and printed circuit boards. Use of the graphics section is shown in Figure 1, and a more detailed screen view is shown in Figure 2.

Interconnection of points as drawn on the screen corresponds to the interconnection of pins on actual integrated circuits. This information may be transferred to either wirewrap or logic simulation portions.

Figure 1. Interactive Graphics Terminal

An option to specify a truth table for read-only memory specification is also accessible from the graphics software. The data may be output on punched paper tape for use on the PROM programmers currently in use at Bendix. For PROM truth table synthesis, the desired input and output waveforms may be drawn and used to access the synthesis software portion.

Synthesis

The first section that would be used in normal design process is logic synthesis. The desired inputs and outputs of the circuit are entered in the computer and results displayed. For non-unique solutions, the engineer would answer questions to determine the desired results. The truth table that is generated is saved for the overall analysis of the circuit. The basic part of the ROM synthesis program, called SEQMAC, is a modified version of the program SHIVA, which was written at Auburn University. The program is interactive and will read either a state table or a timing diagram. It will minimize the resulting sequential machine and, in the process, will write certain sets of states that are candidates for inclusion in the minimal machine. For certain machines the minimum may not be found in a reasonable amount of time. In this case, the user may select sets of states and the program will determine if they constitute an equivalent machine. The program will then produce a paper tape to be used in programming a ROM for the construction of the circuit. An example of a synthesis run is shown in Appendix A.

Simulation

The second section is the analysis of a defined circuit. The analysis would show the time related responses of selected inputs and outputs. This simulation provides the engineer with a breadboard capability to design circuits, which should be less costly than hardware test circuits. For digital logic simulation, the program HAL1900 (obtained from LLL) was selected as the basis because of its accurate device modeling. The original program was intended to run interactively, but with the limited memory size on the computer, it is presently run in the batch mode. A card deck is punched with data to describe the circuit topology in terms of standard integrated circuits from the library and models defined by the user. The output is a list of signal transitions and transients that occurred and a waveform type plot of up to 20 signal lines. Besides the Boolean analysis of the gates, the program also considers the rise and fall time of signals and will indicate race conditions. After the output is reviewed, the engineer can then change any cards necessary and rerun the program until the correct results are obtained.

The basic elements for a circuit description are AND, NAND, OR, NOR, and ROM gates. (The capability to simulate ROMs was added to the program at Bendix.) The elements are defined with switching characteristics, propagation delay, and transition time, to closely model real-world devices. The input signals are defined using two states, 0 and 1, and transition time, resolved to 1 ns increments.

The program features a capability (the macrocompiler) to model devices made up of basic gates. This permits the engineer to model a device or section of circuit and use several within the overall circuit. The models reduce the task of defining the circuit by avoiding the detailed interconnections of all basic gates. The task is further reduced if the device is modeled and put on the program library. The model may be used to describe other models up to four levels. An example of a simulation run is in Appendix B.

Fabrication

The major development of this endeavor was the wirewrap program. Once the interconnections of components have been input for the analysis section, the information may also be used to generate a tape for the semiautomatic wirewrap machine. The additional information required is the component placement on the circuit board.

The data for the program is a description of wiring options, component pin dimensions, component location, and interconnections for circuit definition. Wiring options include shortest distance or right angle wire length and specified length to specified components. The component pin dimensions are set up in the "model definition." The options for definition include dual in-line package, matrix, and pin-by-pin. If no model definition is specified, a library of dual in-line packages will be used by default. Once the components are defined, their location on the board is specified in the "board layout" section. Components are specified by name, type of pin configuration, pin 1 location from user selected reference point, orientation, ground, and voltage supply pins.

The last section is the interconnection list. Signal lines are defined by listing the component pins that are tied together. The wiring information is then sorted to wrap by level, first level one and then level two. It also wires the longest wires first, to be held by short wires. (The user need not be aware of either sort.) There are two outputs from the program, the

printer listing and the punched tape, if the option is selected. The tape is carried to the fabrication site and mounted on the machine. The printer output lists the input definition and the interconnection list in two formats. The interconnections are listed by signal (which pins are connected) and by component (which signals are connected to component pins). There is also a printer plot to approximate a picture of the board layout and a listing of the tape.

A detailed description of input format is stored in the computer and continually updated. The current edition may be obtained at the user terminal with the commands shown in Figure 3. The resulting instructions and sample printout are contained in Appendix C.

Currently, Bendix is saving a substantial amount each month through the use of semiautomatic wiring and at times has experienced nearly eight times the workload originally forecast--27,000 wirewraps per year.

ACCOMPLISHMENTS

- The success of the semiautomatic wiring activity and associated cost savings make the fabrication section the most important. This section will be adapted to a minicomputer.
- A minicomputer based graphics system has been purchased.

FUTURE WORK

No future activity is planned in support of this project. Semi-automatic wiring software will be implemented on an existing minicomputer system, with dedicated hardware to be purchased when usage justifies.

WIREWAP DOCUMENTATION

ENTER THE FOLLOWING AT
USER TERMINAL

Ⓢ = SEND KEY

= = WWD0C	Ⓢ
C	Ⓢ

FIRST PAGE OF PRINTOUT WILL
BE IDENTIFIED BY WW 064

Figure 3. User Terminal
Instruction Card

Appendix A

SYNTHESIS PROGRAM EXAMPLE

Figure A-1. Example Problem to be Analyzed

EXAMPLE #1

1-FREE 2-STAND 3-TIMING3
 ENTER NUMBER STATES, INPUTS, OUTPUTS 080203
 ENTER INPUT 1010101
 01010101
 ENTER INPUT 200001111
 00001111
 TO CHANGE ENTER LINE NUMBER ELSE 00
 ENTER OUTPUT 101000100
 01000100
 ENTER OUTPUT 200010001
 00010001
 ENTER OUTPUT 300000001
 00000001
 TO CHANGE ENTER LINE NUMBER ELSE 00
 STATE TABLE

	NEXT STATES				OUTPUTS			
INPUTS	1	2	3	4	1	2	3	4
PRESENT STATE								
1	1	0	2	0	1	0	5	0
2	3	0	2	0	1	0	5	0
3	3	0	4	0	1	0	3	0
4	0	5	4	0	0	1	3	0
5	0	5	0	6	0	1	0	5
6	0	7	0	6	0	1	0	5
7	0	7	0	8	0	1	0	4
8	1	0	0	8	1	0	0	4

MINIMIZE YES NOYES
 PAIR IMPLICATION

1 5 IMPLIES
 1 6 IMPLIES
 1 7 IMPLIES
 1 8 IMPLIES
 2 5 IMPLIES
 2 6 IMPLIES
 2 7 IMPLIES
 3 4 IMPLIES
 3 5 IMPLIES
 3 6 IMPLIES
 3 7 IMPLIES

4 5 IMPLIES
PAUSE 0

4 8 IMPLIES
7 8 IMPLIES
PAUSE 0

THE COMP. SETS ARE GIVEN HERE IN OCTAL FORMAT
EXPAND THEM INTO BINARY NOTATION. NAME STATES
STARTING FROM RIGHT. A 1 REPRESENTS THE
PRESENCE OF THE STATE IN THE SET.
EXAMPLE.. 52 = 101010 = (2,4,6)

MAXIMAL COMPATIBLES

301
034
021
041
022
042
102
044
104
210

PAUSE 0

AGH
CDE
AE
AF
BE
BF
EG
CF
CG
DH

PAUSE 0

PRIME COMPATIBLES

301
034
021
041
022
042
102
044
104
210

PAUSE 0

AGH

CDE

AE

AF

BE

BF

BG

CF

CG

DH

NO ESSENTIAL P. C.

NUMBER OF PRIME CLASSES= 10

THE LIMITS ON THE NO. OF STATES
IN THE MINIMAL MACHINE ARE

LOWER = 3 HIGHER= 8

TIME= 4.062 ENTER NEW TIME LIMIT 13 or 0 FOR INTERACTION

020

MINIMAL CLASS

301

034

042

PAUSE 0

REDUCED TABLE

PRES.STATE NEXT STATE OUTPUTS

1	1	1	3	1	1	1	5	4
2	2	2	2	3	1	1	3	5
3	2	1	3	3	1	1	5	5

STATE ASSIGNMENT

1	0
2	3
3	1

PAUSE 0

ROM TRUTH TABLE

INPUT	STATE	STATEOUT	OUTPUT
00	00	00	000
00	11	11	000
00	01	11	000
01	00	00	000
01	11	11	000
01	01	00	000
10	00	01	100
10	11	11	010
10	01	01	100
11	00	00	011
11	11	01	100
11	01	01	100

PAUSE 0

1-SHIVA OR TAPE1 INPUT 2-STOP 3-OTHER

EXAMPLE #2

AUTOM

1-SHIVA OR TAPE1 INPUT 2-STOP 3-OTHER3

1-FREE 2-STAND 3-TIMING1

ENTER NUMBER STATES-NUMBER INPUTS-NUMBER OUTPUTS 080401

ENTER LINE 1 OF FLOW TABLE-,- 7,0 5,1 4,-

ENTER LINE 2 OF FLOW TABLE1,- 4,- -,- -,0

ENTER LINE 3 OF FLOW TABLE3,- -,0 -,- 7,1

ENTER LINE 4 OF FLOW TABLE5,0 -,- 1,- -,-

ENTER LINE 5 OF FLOW TABLE-,1 6,- -,1 -,1

ENTER LINE 6 OF FLOW TABLE-,1 5,- 1,1 -,1

ENTER LINE 7 OF FLOW TABLE6,- -,1 2,- 8,-

ENTER LINE 8 OF FLOW TABLE3,- -,- 1,0 -,-

ENTER LINE NUMBER TO MODIFY. ELSE 00

FLOW TABLE

-,- 7,0 5,1 4,-

1,- 4,- -,- -,0

3,- -,0 -,- 7,1

5,0 -,- 1,- -,-

-,1 6,- -,1 -,1

-,1 5,- 1,1 -,1

6,- -,1 2,- 8,-

3,- -,- 1,0 -,-

PAUSE 0

STATE TABLE

INPUTS PRESENT STATE	NEXT STATES				OUTPUTS			
	1	2	3	4	1	2	3	4
1	0	7	5	4	0	1	2	0
2	1	4	0	0	0	0	0	1
3	3	0	0	7	0	1	0	2
4	5	0	1	0	1	0	0	0
5	0	6	0	0	2	0	2	2
6	0	5	1	0	2	0	2	2
7	6	0	2	8	0	2	0	0
8	3	0	1	0	0	0	1	0

MINIMIZE YES NOYES
PAIR IMPLICATION

1 2 IMPLIES 4 7,
1 3 IMPLIES 4 7,
1 4 IMPLIES 1 5,
1 5 IMPLIES 6 7,
1 6 IMPLIES 5 7, 1 5,
2 4 IMPLIES 1 5,
2 7 IMPLIES 1 6,
2 8 IMPLIES 1 3,
3 4 IMPLIES 3 5,
3 5 IMPLIES
3 6 IMPLIES
3 8 IMPLIES

PAUSE 0

4 7 IMPLIES 5 6, 1 2,
4 8 IMPLIES 3 5,
5 6 IMPLIES 5 6,
5 7 IMPLIES
6 7 IMPLIES 1 2,
7 8 IMPLIES 3 6, 1 2,
PAUSE 0

THE COMP. SETS ARE GIVEN HERE IN OCTAL FORMAT
EXPAND THEM INTO BINARY NOTATION, NAME STATES
STARTING FROM RIGHT. A 1 REPRESENTS THE
PRESENCE OF THE STATE IN THE SET.
EXAMPLE.. 52 = 101010 = (2,4,6)

MAXIMAL COMPATIBLES

~~0~~65
312
~~0~~13
~~0~~15
214
16~~0~~

PAUSE 0

ACEF

BDGH

ABD

ACD

CDH

EFG

PAUSE 0

PRIME COMPATIBLES

~~0~~65
312
~~0~~25
~~0~~45
~~0~~61
~~0~~64
112
212
~~3~~~~0~~2
31~~0~~
~~0~~13
~~0~~15
214
16~~0~~
~~0~~~~0~~5
~~0~~21
~~0~~41
~~0~~12
1~~0~~2

PAUSE

2~~0~~2
11~~0~~
~~3~~~~0~~~~0~~
~~0~~~~0~~3
~~0~~11
2~~0~~4
12~~0~~
~~0~~~~0~~1

~~002~~
~~010~~

PAUSE 0

ACEF

BDGH

ACE

ACF

AEF

CEF

BDG

BDH

EGH

DGH

ABD

ACD

CDH

EFG

AC

AE

AF

BD

EG

PAUSE 0

BH

DG

GH

AE

AD

CH

EG

A

B

D

NO ESSENTIAL P. C.

NUMBER OF PRIME CLASSES= 29

THE LIMITS ON THE NO. OF STATES
IN THE MINIMAL MACHINE ARE

LOWER= 2 HIGHER= 6

TIME= .893 ENTER NEW TIME LIMIT 13 OR 0 FOR INTERACTION~~020~~

LOWER BOUND INCREASED TO 3

MINIMAL CLASS

064
310
003
PAUSE 0

REDUCED TABLE

PRES. STATE	NEXT STATE	OUTPUTS
1	1 1 3 2	2 1 2 2
2	1 0 3 2	1 2 1 0
3	3 2 1 2	0 1 2 1

STATE ASSIGNMENT

1	0
2	1
3	2

PAUSE 0

ROM TRUTH TABLE

INPUT	STATE	STATEOUT	OUTPUT
00	00	00	1
00	01	00	0
00	10	10	0
01	00	00	0
01	01	01	1
01	10	01	0
10	00	10	1
10	01	10	0
10	10	00	1
11	00	01	1
11	01	01	1
11	10	01	0

PAUSE 0

1-SHIVA OR TAPE1 INPUT 2-STOP 3-OTHER

AUTOM

1-SHIVA OR TAPE 1 INPUT 2-STOP 3-OTHER3

1-FREE 2-STAND 3-TIMING1

ENTER NUMBER STATES-NUMBER INPUTS-NUMBER OUTPUTS 090401

ENTER LINE 1 OF FLOW TABLE2,- 4,- -, 3,-

ENTER LINE 2 OF FLOW TABLE6,- 9,- -, -, -

ENTER LINE 3 OF FLOW TABLE-,- -, 7,- 8,-

ENTER LINE 4 OF FLOW TABLE2,- 1,- 6,- 5,-

ENTER LINE 5 OF FLOW TABLE-,- -, -, 6,-

ENTER LINE 6 OF FLOW TABLE1,0 -, 2,- -, 1

ENTER LINE 7 OF FLOW TABLE5,1 2,- -, -, -

ENTER LINE 8 OF FLOW TABLE5,- -,- -,- 1,Ø
 ENTER LINE 9 OF FLOW TABLE5,- 3,- -,- -,-
 ENTER LINE NUMBER TO MODIFY, ELSE ØØ

FLOW TABLE

2,- 4,- -,- 3,-
 6,- 9,- -,- -,-
 -,- -,- 7,- 8,-
 2,- 1,- 6,- 5,-
 -,- -,- -,- 6,-
 1,Ø -,- 2,- -,1
 5,1 2,- -,- -,-
 5,- -,- -,- 1,Ø
 5,- 3,- -,- -,-

PAUSE 0

STATE TABLE

NEXT STATES

OUTPUTS

INPUTS	1	2	3	4		1	2	3	4
PRESENT STATE									
1	2	4	Ø	3		Ø	Ø	Ø	Ø
2	6	9	Ø	Ø		Ø	Ø	Ø	Ø
3	Ø	Ø	7	8		Ø	Ø	Ø	Ø
4	2	1	6	5		Ø	Ø	Ø	Ø
5	Ø	Ø	Ø	6		Ø	Ø	Ø	Ø
6	1	Ø	2	Ø		1	Ø	Ø	2
7	5	2	Ø	Ø		2	Ø	Ø	Ø
8	5	Ø	Ø	1		Ø	Ø	Ø	1
9	5	3	Ø	Ø		Ø	Ø	Ø	Ø

MINIMIZE YES NOYES

PAIR IMPLICATION

1 2 IMPLIES 2 6, 4 9,
 1 3 IMPLIES 3 8,
 1 5 IMPLIES 3 6,
 1 6 IMPLIES 1 2,
 1 8 IMPLIES 2 5, 1 3,
 2 3 IMPLIES
 2 5 IMPLIES
 2 6 IMPLIES 1 6,
 2 7 IMPLIES 5 6, 2 9,
 2 8 IMPLIES 5 6,
 2 9 IMPLIES 5 6, 3 9,
 3 6 IMPLIES 2 7,
 3 7 IMPLIES

PAUSE 0

3 8 IMPLIES 1 8,
 3 9 IMPLIES
 4 5 IMPLIES 5 6,
 4 6 IMPLIES 1 2, 2 6,
 4 7 IMPLIES 2 5, 1 2,
 4 8 IMPLIES 2 5, 1 5,
 4 9 IMPLIES 2 5, 1 3,
 5 6 IMPLIES
 5 7 IMPLIES
 5 8 IMPLIES 1 6,
 5 9 IMPLIES
 6 9 IMPLIES 1 5,
 7 8 IMPLIES
 7 9 IMPLIES 2 3,
 8 9 IMPLIES
 PAUSE 0

THE COMP. SETS ARE GIVEN HERE IN OCTAL FORMAT
 EXPAND THEM INTO BINARY NOTATION, NAME STATES
 STARTING FROM RIGHT. A 1 REPRESENTS THE
 PRESENCE OF THE STATE IN THE SET.
 EXAMPLE.. 52 = 101010 = (2,4,6)

MAXIMAL COMPATIBLES

706
 722
 730
 047
 207
 063
 223
 446
 462
 470

PAUSE

BCGHI
 BEGHI
 DEGHI
 ABCF
 ABCH
 ABEP
 ABEH
 BCPI
 BEPI
 DEPI
 PAUSE 0

PRIME COMPATIBLES

~~706~~
~~722~~
~~730~~
~~506~~
~~702~~
~~704~~
~~322~~
~~522~~
~~622~~
~~720~~
~~330~~
~~530~~
~~630~~
~~710~~
~~047~~
~~207~~
~~063~~
~~223~~
~~446~~

PAUSE 0

~~462~~
~~470~~
~~302~~
~~602~~
~~304~~
~~504~~
~~604~~
~~700~~
~~122~~
~~222~~
~~422~~
~~320~~
~~520~~
~~620~~
~~130~~
~~230~~
~~430~~
~~310~~
~~510~~
~~610~~

PAUSE 0

~~007~~
~~043~~
~~045~~
~~046~~
~~205~~
~~061~~
~~062~~
~~221~~
~~444~~
~~460~~
~~070~~
~~006~~
~~202~~
~~104~~
~~404~~
~~300~~
~~600~~
~~022~~
~~120~~
~~420~~

PAUSE 0

~~030~~
~~110~~
~~210~~
~~410~~
~~005~~
~~041~~
~~044~~
~~021~~
~~060~~
~~001~~
~~010~~

PAUSE 0

BCGHI
BEGHI
DEGHI
BCGI
BGHI
CGHI
BEGH
BEGI
BEHI
EGHI
DEGH
DEGI
DEHI
DGHI

ABCF
ABCH
ABEF
ABEH
BCFI
PAUSE

BEFI
DEFI
BGH
BHI
CGH
CGI
CHI
GHI
BEG
BEH
BEI
EGH
EGI
EHI
DEG
DEH
DEI
DGH
DGI
DHI
PAUSE 0

ABC
ABF
ACF
BCF
ACH
AEF
BEF
AEH
CFI
EFI
DEF
BC
BH
CG
CI
GH
HI
BE
EG
EI

PAUSE 0

DE

DG

DH

DI

AC

AF

CF

AE

EF

A

D

NO ESSENTIAL P. C.

NUMBER OF PRIME CLASSES= 70

THE LIMITS ON THE NO. OF STATES
IN THE MINIMAL MACHINE ARE

LOWER= 2 HIGHER= 9

TIME= 2.390ENTER NEW TIME LIMIT 13 or 0 FOR INTERACTION030

LOWER BOUND INCREASED TO 3

TIME= 30.000ENTER NEW TIME LIMIT 13 OR 0 FOR INTERACTION060

TIME= 60.001ENTER NEW TIME LIMIT 13 OR 0 FOR INTERACTION150

TIME LIMIT

COMMAND-

Appendix B

SIMULATION PROGRAM EXAMPLE

Figure B-1. Example Circuit to be Analyzed

```

NC744,0744-51275-31-5860498,HAL,T200.
ATTACH,HAL,HAL.
ATTACH,TAPE9,HALSLIB.
REQUEST,DMFILE,*AX30,OV.
DISPOSE,TAPE8,*PR.
HAL.
REWIND,TAPE8.
COPY,TAPE8,OUTPUT.
DISPOSE,TAPE8.
EXIT.
REWIND,TAPE8.
COPY,TAPE8,OUTPUT.
DISPOSE,TAPE8.
DEF1,0,5,3,4,20
EXT1,E1,E2
ELEM,994A,6,2,4,5,2,3,7,14
994A,AND1,E1,+,C1
994A,AND2,E2,+,C1
994A,AND3,C1,+,O1
PTO1,1,01,C1,E2,E1
TRAN,01,C1,E1,E2
GO BEARS
01011
01019

```

STATIC LOAD CHECK

```

SIGNAL LOAD
C1 7.0 WIRED OR
C1 7.0
C1 0.0
O1 0.0
E1 7.0
E2 7.0
- 0.0
+ 21.0

```

***** NO ERRORS - BEGIN SIMULATION

DIAGNOSTIC OUTPUTS - TRAN AND PTO1

TIME SIGNAL TRANSITION

```

7.0 O1 -
19.0 E1 +
19.0 E2 +
24.0 C1 -

```

32.0	01	+
39.0	E1	-
39.0	E2	-
50.0	C1	+
58.0	01	-
59.0	E1	+
59.0	E2	+
64.0	C1	-
72.0	01	+

***** LIFE FUNCTIONS TERMINATED - SIMULATION COMPLETE

TIME	C1	01	E1	E2
0.	5	5	0	0
1.	5	5	0	0
2.	5	5	0	0
3.	5	5	0	0
4.	5	5	0	0
5.	5	5	0	0
6.	5	5	0	0
7.	5	5	0	0
8.	5	2	0	0
9.	5	1	0	0
10.	5	0	0	0
11.	5	0	0	0
12.	5	0	0	0
13.	5	0	0	0
14.	5	0	0	0
15.	5	0	0	0
16.	5	0	0	0
17.	5	0	0	0
18.	5	0	0	0
19.	5	0	0	0
20.	5	0	2	2
21.	5	0	3	3
22.	5	0	4	4
23.	5	0	4	4
24.	5	0	4	4
25.	2	0	4	4
26.	1	0	5	5
27.	0	0	5	5
28.	0	0	5	5
29.	0	0	5	5
30.	0	0	5	5
31.	0	0	5	5
32.	0	0	5	5
33.	0	3	5	5

Appendix C

WIREWRAP INSTRUCTIONS AND SAMPLE PRINTOUT

THE WIREWRAP PROGRAM EXECUTED IS ISSUE B.	100
THIS VARIES FROM ISSUE A IN THREE AREAS.	200
THE COMPUTER CONTROL CARD SECTION;	300
THE PROGRAM CONTROL CARD SECTION;	310
AND THE OUTPUT LISTING.	312
THE COMPUTER CONTROL CARDS ARE LISTED BELOW.	314
THE PROGRAM CONTROL CARD OPTION ADDED IS 'LIST PACK'.	320
THE ADDITIONAL OUTPUT INCLUDES,	322
ON PAGE 1 : THE TIME AND DATE	324
A LIST OF IC'S THAT OVERLAP AREAS	326
ON THE PRINTER PLOT SUMMARY : A LIST OF NUMBER OF WIRES PER PIN.	328
COMMENT CARDS OF THIS DOCUMENTATION ARE BLANK IN COLUMNS 1-4	330
NUMBERS IN : : INDICATE CARD COLUMN NUMBERS	410
LJ FOR LEFT JUSTIFIED WITHIN THE FIELD SPECIFIED	500
RJ FOR RIGHT JUSTIFIED	600
FF FOR FREE FIELD	700
R FLOATING POINT - REAL	800
I FIXED POINT - INTEGER - RIGHT JUSTIFIED	900
THE FORMAT FOR THIS ISSUE IS GIVEN IN THE FOLLOWING LINES	1000
	1100
	1200
	1300
	1400
	1500
	1600
	1700
	1800
	1900
	2000
	2100
	2200
	2300
	2400
	2500
	2600
	2700
	2800
	2900

IIIII,DDDD-INDEX-JC-PROJECT,NAME,TSEC.

IIIII IS THE IDENTIFICATION ON THE FIRST PAGE OF PRINTOUTS
 GENERALLY INITIALS AND DEPARTMENT NUMBER.
 DDDD FOUR DIGIT DEPARTMENT NUMBER,
 ZERO FILL, RIGHT JUSTIFY.
 INDEX EMPLOYEE INDEX NUMBER 5 DIGITS
 ZERO FILL, RIGHT JUSTIFY.
 JC JOB CATEGORY 32 FOR CIRCUIT ANALYSIS
 PROJECT USER IDENTIFICATION FIELD. 10 CHARACTERS MAX
 PROJECT NUMBER.
 NAME USERS NAME OR OTHER IDENT - OPTIONAL. 10 CHAR MAX
 TSEC EXPECTED NUMBER OF SECONDS FOR THE JOB TO RUN.
 T100 FOR SMALLER BOARDS IS USUALLY SUFFICIENT BUT MAY
 BE EXTENDED IF TIME LIMIT CAUSES ABNORMAL TERMINATION.

SWITCH#1.	3000
OPTIONAL - IF ABSENT, THE LISTING WILL PRINT AT CENTRAL SITE.	3010
SWITCH#2.	3012
OPTIONAL - IF PRESENT, THE LISTING OF THE TAPE WILL BE OMITTED.	3014
BEGIN,YRRAP.	3016
EOR	3100
EOR REPRESENTS THE END OF THE CONTROL CARDS	3400
IT IS MADE BY MULTIPUNCH IN COLUMN 1 789	3500
	3600
	3700
	3800
	3900
	4000
	4100
	4200
** PROGRAM CONTROL CARDS **	4300
	4400
ISSUE B	4500
BOARD IDENTIFICATION ORIGIN LOCATION X	4600
BOARD IDENTIFICATION 20 CHARACTERS MAX :1-20:FF	4700
ORIGIN LOCATION 20 CHARACTERS MAX :21-40:FF	4800
BOARD ORIENTATION FOR IC LAYOUT.	4900
COLUMN 51 BLANK - TOP SIDE WIRE	5000
OR X - FLIP BOARD LEFT TO RIGHT TO WIRE	5100
OR Y - FLIP BOARD TOP TO BOTTOM	5200
	5300
LIST BACK	5310
OPTIONAL - USED TO PRINT TWO POINTS PER LINE OF THE	5312
CONNECTIONS LISTING FOR SHORTER PRINTOUTS.	5314
TAPE ON	5400
OPTIONAL - NO TAPE WILL BE GENERATED IF ABSENT.	5500
	5600
RIGHT ANGLE	5700
OPTIONAL - DIAGONAL WIRE LENGTH WILL BE USED IF ABSENT.	5800
	5900
WIRE INCR WINC	6000
OPTIONAL - USED FOR LARGER BOARDS WHEN THE WIRE LENGTH MAY	6100
EXCEED 15.0 INCHES.	6200
WINC IS THE INCREMENT LENGTH OF WIRE SIZES, 1.0 WILL	6300
EXTEND THE LIMIT TO 30.0 INCHES. :11-15:R	6400

EXTRA LENGTH WIRES	6500
ICNAME1 EXTRAL1	6600
ICNAME2 EXTRAL2	6700
* *	6800
* *	6900
OPTIONAL - WITH THIS OPTION, ADDITIONAL WIRE LENGTH MAY BE	7000
SPECIFIED FOR WIRES CONNECTING TO THE IC'S LISTED.	7100
THE LIST IS TERMINATED BY THE "MODEL DEFINITION"	7200
CONTROL CARD.	7300
ICNAME1 EXAMPLE IC NAME. :1-10:LJ	7400
EXTRAL1 EXAMPLE WIRE LENGTH. :11-20:R	7500
THE EXTRA LENGT IS SPECIFIED IN INCHES	7600
AND WILL BE ADDED TO THE CALCULATED WIRE LENGTH.	7700
	7800
	7900
	8000
	8100
	8200
	8300
	8400
** MODEL DEFINITION SECTION **	8500
	8600
THIS SECTION MAY BE OMITTED IF AUGAT INPUT FORMAT IS USED.	8700
MODEL DEFINITION	8800
MODELNAME DELTAX DELTAY DINP	8900
MODELNAME USER DEFINED NAME FOR PIN CONFIGURATION :1-10:LJ	9000
DELTAX SPACING BETWEEN PINS IN INCHES IN THE X DIRECTION.	9100
10 CHARACTER FIELD :11-20:R	9200
DELTAY Y DIRECTION SPACING :21-30:R	9300
WHERE X IS HORIZONTAL AND POSITIVE TO THE RIGHT	9400
AND Y IS VERTICAL AND POSITIVE UP.	9500
DI DI SPECIFIES DUAL INLINE PIN CONFIGURATION AND PIN	9600
NUMBERING SCHEME :31-32:	9700
NP NUMBER OF PINS IN THE MODEL :33-34:I	9800
MODELNAME DELTAX DELTAY CRNXNY	9900
MODELNAME 10 CHARACTER FIELD :1-10:LJ	10000
DELTAX SAME AS ABOVE	10100
DELTAY SAME AS ABOVE	10200
CR CR DESIGNATES PIN NUMBERING INCREASING	10300

	ALONG THE COLUMN.	:31-32:	10400				
	OR RC DESIGNATES PIN NUMBERING INCREASING		10500				
	ALONG A ROW.	:31-32:	10600				
NX	NUMBER OF COLUMNS IN THE MATRIX	:33-34:1	10700				
NY	NUMBER OF ROWS	:35-36:1	10800				
MODELNAME	DELTA	DELTA	RCNXNY	DELTA	DELTA	RCNXNY	10900
	THE SECOND DELTA,DELTA,CRNXNY IS FOR REPEATED MATRIX PATTERNS						11000
	WITH CONTINUOUS PIN NUMBERS.						11100
CR 3 7	EXAMPLE	RC 7 3	EXAMPLE				11200
	1 8 15		1 2 3 4 5 6 7				11300
	2 9 16		8 9 10 11 12 13 14				11400
	3 10 17		15 16 17 18 19 20 21				11500
	4 11 18						11600
	5 12 19						11700
	6 13 20						11800
	7 14 21						11900
			DELTA WOULD BE POSITIVE AND				12000
			DELTA WOULD BE NEGATIVE IN BOTH CASES.				12100
MODELNAME							12200
PIN1NAME	X0	Y0					12300
PIN2NAME	X1	Y1					12400
.							12500
.							12600
WITH THIS OPTION, ANY MODEL CONFIGURATION MAY BE DEFINED							12700
WITH X AND Y REPRESENTING RELATIVE COORDINATES WITHIN THE MODEL.							12800
THE PINNAME IS A 10 CHARACTER FIELD :1-10:LJ							12900
X AND Y ARE 10 CHARACTER FIELDS :11-20,21-30:R							13000
THE LIST IS TERMINATED WITH ANOTHER MODEL NAME CARD OR							13100
BOARD LAYOUT CONTROL CARD.							13200
							13300
MODEL DEFINITION LIBRARY FOR AUGAT BOARDS							13400
							13500
GNDVCC	0.6	-0.8	CR0406	2.7	0.0	CR0601	13600
6PIN	0.3	-0.1	DI06				13700
8PIN	0.3	-0.1	DI08				13800
14PIN	0.3	-0.1	DI14				13900
16PIN	0.3	-0.1	DI16				14000
18PIN	0.3	-0.1	DI18				14100
							14200

20PIN	0.3	-0.1	DI20		14300
22PIN	0.3	-0.1	DI22		14400
24PIN	0.3	-0.1	DI24		14500
8PIN6	0.6	-0.1	DI08		14600
14PIN6	0.6	-0.1	DI14		14700
16PIN6	0.6	-0.1	DI16		14800
18PIN6	0.6	-0.1	DI18		14900
20PIN6	0.6	-0.1	DI20		15000
22PIN6	0.6	-0.1	DI22		15100
24PIN6	0.6	-0.1	DI24		15200
40PIN6	0.6	-0.1	DI40		15300
16PIN8	0.8	-0.1	DI16		15400
8PINGV	0.3	-0.1	DI08	*WITH GND AND VCC PINS	15410
14PINGV	0.3	-0.1	DI14	*WITH GND AND VCC PINS	15420
16PINGV	0.3	-0.1	DI16	*WITH GND AND VCC PINS	15430
28PINWDP				*HIGH DENSITY PLUG, 90 DEGS	15440
					15700

** BOARD DEFINITION - IC LOCATIONS **

BOARD LAYOUT

ICNAME	MODELNAME	X0	Y0	Z	ANGLE	GNDPIN	VCCPIN	PARTNO
ICNAME	10 CHARACTER FIELD	:1-10:LJ						16400
MODELNAME	10 CHARACTER FIELD	:11-20:LJ						16500
X0	X COORDINATE OF PIN ONE ON THE BOARD BEING DEFINED							:21-30:R 16600
Y0	Y COORDINATE OF PIN ONE ON THE BOARD BEING DEFINED							:31-40:R 16700
Z	AXIS FOR ROTATION, X,Y, OR Z							:41: 16800
ANGLE	ANGLE OF ROTATION OF THE MODEL. THE ANGLE MUST BE -90., 0., 90., 180., OR 270. FOR Z AXIS ROTATION, 180.0 FOR X OR Y AXIS							:142-50:R 16900
GNDPIN	GROUND PIN NAME OR NUMBER							:51-60:LJ 17000
	MAY BE LEFT BLANK IF CONNECTION IS NOT REQUIRED.							17100
VCCPIN	POWER SUPPLY PIN NAME							:61-70:LJ 17200
	MAY BE LEFT BLANK IF CONNECTION IS NOT REQUIRED.							17300
								17400
								17500
								17600
								17700
								17800

PARTNO	OPTIONAL USER IDENTIFICATION :71-80:FF	17900
** OPTIONAL BOARD DEFINITION **		18000
THE FOLLOWING IS FOR THE STANDARD AUGAT INPUT FORMAT OPTION.		18100
AUGAT BOARD LAYOUT		18200
ICNAME,GCNR,NSTYLE,GND,VCC,PARTNAME.		18300
FREE FORMAT AS LONG AS THE DEFINED SEQUENCE IS MAINTAINED.		18400
ICNAME LIMITED TO NO MORE THAN 10 CHARACTERS		18500
G GROUP DESIGNATION LETTER, A-F STANDARD		18600
C COLUMN DESIGNATION LETTER, ABSENT FOR EDGE CONNECTORS.		18700
NR ROW NUMBER 1-50 STANDARD		18800
NSTYLE TYPE OF IC OR SOCKET, MODEL NAME.		18900
0.3 X 0.1 INCH SPACING FOR STANDARD DUAL INLINE.		19000
14PIN, 16PIN, SPECIAL, FOR EXAMPLE		19100
THIS LIBRARY IS PROGRAM DEFINED BUT		19200
MAY BE MODIFIED UPON REQUEST.		19300
AN "*" PRECEDING THE MODEL NAME WILL CAUSE 180.0 DEGREE		19400
ROTATION. (EXCLUDING EDGE CONNECTORS		19500
GND GROUND PIN NUMBER		19600
VCC POWER SUPPLY PIN NUMBER		19700
PART PART NAME 10 CHARACTER FREE FIELD		19800
** NETWORK DEFINITION SECTION **		19900
CONNECTIONS		20000
ICNAME-PINNAME,ICNAME-PINNAME,ICNAME-PINNAME.	NETNAME	20100
THE IC OR SOCKET NAME IS SEPERATED FROM PIN NAMES WITH A "-" .		20200
EACH REFERENCE IS SEPERATED BY A " , "		20300
THE NETWORK STRING IS TERMINATED WITH A " , "		20400
NETNAME - 10 CHARACTER FIELD FOR NET OR SIGNAL NAME :71-80:FF		20500
IN THE CONNECTION SECTION, CONTINUATION OF CARDS IS POSSIBLE BY		20600
USING A COMMA INSTEAD OF A POINT ON THE CARD TO BE CONTINUED.		20700
THE LAST CARD OF A CONTINUATION STRING MUST HAVE A " , "		20800
AFTER THE LAST PIN NAME OR NUMBER.		20900
EOF		21000
EOF REPRESENTS THE LAST CARD OF THE DECK AND IS A MULTIPUNCH		21100
IN COLUMN 1 6789 .		21200
		21300
		21400
		21500
		21600
		21700
		21800
		21900

** EXAMPLE PROBLEM **
 W0131,0131-09879-32-TE6185,T100.
 BEGIN,YRRAP.
 EOR

ISSUE B
 TE6185 #1 BOARD A1 AA1
 TAPE #N
 AUGAT BOARD LAYOUT
 U1,AA1,16PIN,NC,NC,16PINCC.
 U2,AA10,14PIN,7,14,7474.
 U3,AA19,14PIN,7,14,7400.
 U4,AC1,14PIN,7,14,7402.
 U5,AC9,16PIN,8,16,3205.
 U6,AC18,16PIN,8,16,3205.
 U7,AE1,20,PIN,10,20,74273.
 U8,AE13,20,PIN,10,20,74273.
 U9,AG1,18PIN,NC,NC,8008.
 U10,AG11,24PIN6,NC,NC,PARTNAME.
 CONNECTIONS
 U1-2,U1-3,U2-4.
 U1-4,U2-10,U2-13.
 U1-5,U9-17.
 U1-6,U3-8,U4-8,U4-9.
 U1-7,U1-8,VCC.
 U1-9,U4-1,U9-16.
 U1-10,U4-4,U5-6,U9-15.
 U1-11,U3-9,U3-10,U4-13.
 U1-12,U9-10,VCC.
 U1-13,U1-14,VCC.
 U1-15,GND.
 U2-1,U3-5,U5-14.
 U2-2,U2-3,GND.
 U2-5,U9-18.
 U2-6,U7-1,U8-1.
 U2-8,U2-12,U4-6.

22000
 22100
 22200
 22300
 22400
 22500
 22600
 22700
 22800
 22900
 23000
 23100
 23200
 23300
 23400
 23500
 23600
 23700
 23800
 23900
 24000
 24100
 24200
 24300
 24400
 24500
 24600
 24700
 24800
 24900
 25000
 25100
 25200
 25300
 25400
 25500
 25600
 25700
 25800

U2-9,U4-3.	25900
U2-11,U4-2,U4-5,U4-10,U4-11,U4-12.	26000
U3-1,U3-13,U5-11,U8-11.	26100
U3-2,U3-6,U6-5.	26200
U3-3,U3-4.	26300
U3-11,U7-11.	26400
U3-12,U5-13.	26500
U5-1,U9-13.	26600
U5-2,U9-12.	26700
U5-3,U9-11.	26800
U5-4,U6-6,U9-14.	26900
U5-5,GND.	27000
U6-1,U7-12,U8-13.	27100
U6-2,U7-15,U8-14.	27200
U6-3,U7-19,U8-18.	27300
U6-4,GND.	27400
U6-15,U10-14.	27500
U7-2,U8-3.	27600
U7-3,U9-2,U10-11.	27700
U7-4,U9-5,U10-8.	27800
U7-5,U8-4.	27900
U7-6,U8-7.	28000
U7-7,U9-6,U10-7.	28100
U7-8,U9-9,U10-4.	28200
U7-9,U8-8.	28300
U7-13,U9-8,U10-5.	28400
U7-14,U9-7,U10-6.	28500
U7-16,U8-17.	28600
U7-17,U9-4,U10-9.	28700
U7-18,U9-3,U10-10.	28800
U8-2,U10-17.	28900
U8-5,U10-20.	29000
U8-6,U10-21.	29100
U8-9,U10-3.	29200
U8-12,U10-2.	29300
U8-15,U10-1.	29400
U8-16,U10-19.	29500
U8-19,U10-18.	29600
EOF	29700
	29800

								29900
								30000
								30100
								30200
								30300
								30400
								30500
								30600
								30700
								30800
								30900
								31000
								31100
								31200
								31300
								31400
								31500
								31600
								31700
								31800
								31900
								32000
								32100
								32200
								32300
								32400
								32500
								32600
								32700
								32800
								32900
								33100

** MULTI-LEVEL EXAMPLE **
 ISSUE 8
 MODEL DEFINITION
 14PIN 0.3 -0.1 DI14
 16PIN 0.3 -0.1 DI16
 MATRIX 0.3 -0.1 CR0206
 CARD DEFINITION
 1420
 11 14PIN 0.0 0.0 180.0 7 14
 12 14PIN 1.0 0.0 180.0 7 14
 13 14PIN 0.0 -1.0 0.0 1 6
 14 16PIN 1.0 -1.0 0.0 8 16
 1425
 11 14PIN 0.0 0.0 90.0 4 5
 12 16PIN 0.0 1.0 90.0 8 9
 13 MATRIX 1.0 -1.0
 CARD LAYOUT
 1AA 1620 0.0 0.0
 1BA 1620 5.0 -5.0
 2A 1425 0.0 -5.0
 BOARD LAYOUT
 XIC1 14PIN 2.5 -2.5 Z 90.0 3 10
 CONNECTIONS
 1AA11-1,1BA11-1,2A11-1,XIC1-1.
 1AA12-1,1BA12-1,2A12-1,XIC1-2.
 EOF

* * * * WWB6420 END OF LIST * * * *

06/21/78

14.41.78.

UA1840A103

ORIGIN AS-1

FLIP BOARD LEFT TO RIGHT

NORMAL STOP MODEL DEFINITION
 NORMAL STOP IC LAYOUT
 NORMAL STOP INTERCONNECT LIST

WIRE NO.	QNTY	LENGTH	
01	75	1.00	75.00
02	20	1.50	30.00
03	15	2.00	30.00
04	9	2.50	22.50
05	5	3.00	15.00
06	7	3.50	24.50
07	3	4.00	12.00
10	1	4.50	4.50
11	0	5.00	0.00
12	0	5.50	0.00
13	0	6.00	0.00
14	0	6.50	0.00
15	0	7.00	0.00
16	0	7.50	0.00
17	0	8.00	0.00
20	0	8.50	0.00
21	0	9.00	0.00
22	0	9.50	0.00
23	0	10.00	0.00
24	0	10.50	0.00
25	0	11.00	0.00
26	0	11.50	0.00
27	0	12.00	0.00
30	0	13.00	0.00
31	0	14.00	0.00
32	0	15.00	0.00
33	0	16.00	0.00
34	0	17.00	0.00
35	0	18.00	0.00
36	0	19.00	0.00
37	0	20.00	0.00
40	0	21.00	0.00
41	0	22.00	0.00
42	0	23.00	0.00
43	0	24.00	0.00
44	0	25.00	0.00
45	0	26.00	0.00
46	0	27.00	0.00
47	0	28.00	0.00
50	0	29.00	0.00
	136		219.50

SD 10008						
A5	2	0.00000	-0.10000	0.00000	99.90000	
A13	1	1.00000	-2.00000	1.00000	98.00000	
A8	3	1.00000	-1.20000	1.00000	98.80000	
SD 10009						
A5	8	0.00000	-0.70000	0.00000	99.30000	
A15	5	0.30000	-2.30000	0.30000	97.70000	
SD 10010						
A15	2	0.00000	-2.10000	0.00000	97.90000	
A19	7	0.00000	-3.60000	0.00000	96.40000	
SD 10011						
A10	7	0.00000	-1.60000	0.00000	98.40000	
A5	12	0.30000	-0.40000	0.30000	99.60000	
SD 10012						
A10	6	0.00000	-1.50000	0.00000	98.50000	
A15	6	0.30000	-2.20000	0.30000	97.80000	
A15	8	0.30000	-2.00000	0.30000	98.00000	
SD 10013						
A19	16	0.80000	-3.00000	0.80000	97.00000	
A18	4	1.00000	-3.30000	1.00000	96.70000	
SD 10014						
A19	14	0.80000	-3.20000	0.80000	96.80000	
A8	12	1.30000	-1.40000	1.30000	98.60000	
SD 10015						
A19	12	0.80000	-3.40000	0.80000	96.60000	
A18	15	1.30000	-3.10000	1.30000	96.90000	
SD 10016						
A19	10	0.80000	-1.60000	0.80000	96.40000	
VCC	11	0.80000	-3.90000	0.80000	96.10000	
SD 10017						
A15	3	0.00000	-2.20000	0.00000	97.80000	
A18	6	1.00000	-3.50000	1.00000	96.50000	
A14	5	2.00000	-3.40000	2.00000	96.60000	
SD 10018						
A10	1	1.00000	-3.00000	1.00000	97.00000	
VCC	10	0.80000	-2.90000	0.80000	97.10000	
SD 10019						
A18	8	1.00000	-3.70000	1.00000	96.30000	
GND	17	1.00000	-3.90000	1.00000	96.10000	
SD 10020						
A18	5	1.00000	-3.40000	1.00000	96.60000	
A18	7	1.00000	-3.60000	1.00000	96.40000	
A3	9	1.30000	-0.70000	1.30000	99.30000	
SD 10021						
A18	14	1.30000	-3.20000	1.30000	96.80000	
A18	11	1.30000	-3.50000	1.30000	96.50000	
A3	10	1.30000	-0.60000	1.30000	99.40000	
SD 10022						
A13	16	1.30000	-2.00000	1.30000	98.00000	
GND	21	1.50000	-1.90000	1.50000	98.10000	
SD 10023						
A8	2	1.00000	-1.10000	1.00000	98.90000	
A3	3	1.00000	-0.20000	1.00000	99.80000	

SD j0024					
AB	11	1.30000	-1.50000	1.30000	98.50000
A12	2	1.50000	-2.10000	1.50000	97.90000
A16	13	2.30000	-3.10000	2.30000	98.90000
SD j0025					
A3	13	1.30000	-1.30000	1.30000	99.70000
A12	1	1.50000	-2.00000	1.50000	98.00000
AB	5	1.00000	-1.40000	1.00000	98.60000
SD j0026					
AB	4	1.00000	-1.30000	1.00000	98.70000
AB	7	1.00000	-1.60000	1.00000	98.40000
SD j0027					
AB	6	1.00000	-1.50000	1.00000	98.50000
AB	9	1.30000	-1.70000	1.30000	98.30000
SD j0028					
AB	1	1.00000	-1.00000	1.00000	99.00000
VCC	8	.80000	-.90000	.80000	99.10000
SD j0029					
AB	8	1.00000	-1.70000	1.00000	98.30000
GND	15	1.00000	-1.90000	1.00000	98.10000
SD j0030					
A12	5	1.50000	-2.40000	1.50000	97.60000
A12	6	1.50000	-2.50000	1.50000	97.50000
A12	9	1.80000	-2.60000	1.80000	97.40000
A12	9	1.80000	-2.50000	1.80000	97.50000
A12	12	1.80000	-2.20000	1.80000	97.80000
A12	13	1.80000	-2.10000	1.80000	97.90000
GND	27	2.00000	-1.90000	2.00000	98.10000
SD j0031					
A12	7	1.50000	-2.60000	1.50000	97.40000
GND	22	1.50000	-2.90000	1.50000	97.10000
SD j0032					
A12	14	1.80000	-2.00000	1.80000	98.00000
VCC	21	1.80000	-1.90000	1.80000	98.10000
SD j0033					
A12	3	1.50000	-2.20000	1.50000	97.80000
B14	5	3.20000	-2.40000	3.20000	97.60000
SD j0034					
AB	1	3.20000	-1.00000	3.20000	99.00000
AB	5	3.20000	-1.40000	3.20000	98.60000
VCC	33	3.00000	-1.90000	3.00000	98.10000
SD j0035					
AB	3	3.20000	-1.20000	3.20000	98.80000
B14	1	3.20000	-2.00000	3.20000	98.00000
SD j0036					
B14	2	3.20000	-2.10000	3.20000	97.90000
AB	14	4.00000	-1.70000	4.00000	98.80000
AB	16	4.00000	-1.00000	4.00000	99.00000

SD 10037					
B14	14	3.52200	-2.20000	3.44000	97.80000
B8	10	4.00000	-1.60000	4.00000	98.40000
B8	12	4.00000	-1.40000	4.00000	98.60000
SD 10038					
B8	7	3.20000	-1.60000	3.20000	98.40000
B14	15	3.50000	-2.10000	3.50000	97.90000
SD 10039					
B14	4	3.20000	-2.30000	3.20000	97.70000
B14	12	3.50000	-2.40000	3.50000	97.60000
B14	16	3.50000	-2.00000	3.50000	98.00000
VCC	39	3.50000	-1.90000	3.50000	98.10000
SD 10040					
B14	8	3.20000	-2.70000	3.20000	97.30000
GND	40	3.20000	-2.90000	3.20000	97.10000
SD 10041					
B14	6	3.20000	-2.50000	3.20000	97.50000
B14	11	3.50000	-2.50000	3.50000	97.50000
SD 10042					
B14	7	3.20000	-2.60000	3.20000	97.40000
A3	7	1.00000	-0.60000	1.00000	99.40000
A16	2	2.00000	-3.10000	2.00000	96.90000
SD 10043					
B14	9	3.50000	-2.70000	3.50000	97.30000
B19	2	3.20000	-3.10000	3.20000	96.90000
SD 10044					
A8	10	1.30000	-1.60000	1.30000	98.40000
A16	9	2.30000	-3.50000	2.30000	96.50000
SD 10045					
A13	2	1.00000	-2.10000	1.00000	97.90000
A5	3	0.00000	-0.20000	0.00000	99.40000
A11	1	2.00000	-2.00000	2.00000	98.00000
SD 10046					
A5	4	0.00000	-0.30000	0.00000	99.70000
B17	14	4.50000	-3.20000	4.50000	96.80000
SD 10047					
A6	1	2.00000	-1.00000	2.00000	99.00000
B12	10	4.50000	-2.60000	4.50000	97.40000
SD 10048					
A6	2	2.00000	-1.10000	2.00000	98.90000
A18	2	1.00000	-3.10000	1.00000	96.90000
SD 10049					
A6	5	2.00000	-1.40000	2.00000	98.60000
A6	6	2.00000	-1.50000	2.00000	98.50000
A6	8	2.30000	-1.60000	2.30000	98.40000
A6	9	2.30000	-1.50000	2.30000	98.50000
A6	12	2.30000	-1.70000	2.30000	98.80000
A6	13	2.30000	-1.10000	2.30000	98.90000
GND	24	2.00000	-0.90000	2.00000	99.10000
SD 10050					
A6	7	2.00000	-1.60000	2.00000	98.40000
GND	27	2.00000	-1.90000	2.00000	98.10000

SD 10051					
A6	14	2.36000	-1.00000	2.36000	99.00000
VCC	26	2.36000	-0.90000	2.36000	99.10000
SD 10052					
A6	7	2.00000	-1.20000	2.00000	98.80000
A3	0	1.00000	-0.50000	1.00000	99.50000
SD 10053					
A16	1	2.00000	-3.00000	2.00000	97.00000
A16	11	2.30000	-3.30000	2.30000	96.70000
SD 10054					
A16	10	2.36000	-3.40000	2.36000	96.60000
A16	10	1.30000	-3.60000	1.30000	96.40000
SD 10055					
A16	3	2.00000	-3.20000	2.00000	96.80000
B12	7	4.20000	-2.60000	4.20000	97.40000
SD 10056					
A16	4	2.00000	-3.30000	2.00000	96.70000
A16	12	1.30000	-3.40000	1.30000	96.60000
SD 10057					
A16	12	2.30000	-3.20000	2.30000	96.80000
A16	14	2.30000	-3.00000	2.30000	97.00000
VCC	28	2.30000	-2.90000	2.30000	97.10000
SD 10058					
A16	7	2.00000	-3.60000	2.00000	96.40000
GND	29	2.00000	-3.90000	2.00000	96.10000
SD 10059					
A18	9	1.30000	-3.70000	1.30000	96.30000
B19	3	3.20000	-3.70000	3.20000	96.80000
B12	5	4.20000	-2.40000	4.20000	97.60000
A11	2	2.00000	-2.10000	2.00000	97.90000
SD 10060					
B19	5	3.50000	-3.30000	3.50000	96.70000
B17	5	3.70000	-3.40000	3.70000	96.60000
SD 10061					
B17	12	4.50000	-3.40000	4.50000	96.60000
B17	16	4.50000	-3.00000	4.50000	97.00000
GND	58	4.70000	-2.90000	4.70000	97.10000
SD 10062					
B17	1	3.70000	-3.00000	3.70000	97.00000
B17	3	3.70000	-3.20000	3.70000	96.80000
B19	6	3.50000	-3.20000	3.50000	96.80000
B19	7	3.50000	-3.10000	3.50000	96.90000
SD 10063					
B19	1	3.20000	-3.00000	3.20000	97.00000
GND	40	3.20000	-2.90000	3.20000	97.10000
SD 10064					
B19	8	3.50000	-3.00000	3.50000	97.00000
VCC	60	3.50000	-2.90000	3.50000	97.10000
SD 10065					
B12	1	4.20000	-2.00000	4.20000	98.00000
B6	7	4.20000	-1.60000	4.20000	98.40000

SD 10066	2	4.20000	-2.10000	4.20000	97.90000
H6	10	5.00000	-1.60000	5.00000	98.40000
H6	12	5.00000	-1.40000	5.00000	98.60000
SD 10067	6	4.20000	-2.50000	4.20000	97.50000
B12	11	4.50000	-2.50000	4.50000	97.50000
SD 10068	4	4.20000	-2.30000	4.20000	97.70000
B12	12	4.50000	-2.40000	4.50000	97.60000
B12	16	4.50000	-2.00000	4.50000	98.00000
VCC	51	4.50000	-1.90000	4.50000	98.10000
SD 10069	8	4.20000	-2.70000	4.20000	97.30000
B12	52	4.20000	-2.90000	4.20000	97.10000
GND					
SD 10070	1	4.20000	-1.00000	4.20000	99.00000
H6	5	4.20000	-1.40000	4.20000	98.60000
H6	45	4.00000	-1.90000	4.00000	98.10000
VCC					
SD 10071	14	5.00000	-1.20000	5.00000	98.80000
H6	14	5.00000	-1.00000	5.00000	99.00000
H6	14	4.50000	-2.20000	4.50000	97.60000
B12					
SD 10072	3	4.20000	-1.20000	4.20000	98.80000
H6	15	4.50000	-2.10000	4.50000	97.90000
B12					
SD 10073	9	4.50000	-2.70000	4.50000	97.30000
B12	11	1.30000	-0.50000	1.30000	99.50000
A3					
SD 10074	5	2.00000	-2.40000	2.00000	97.60000
A11	6	2.00000	-2.50000	2.00000	97.50000
A11	8	2.30000	-2.60000	2.30000	97.40000
A11	9	2.30000	-2.50000	2.30000	97.50000
A11	12	2.30000	-2.20000	2.30000	97.80000
A11	13	2.30000	-2.10000	2.30000	97.90000
A11	7	2.00000	-2.60000	2.00000	97.40000
GND	26	2.00000	-2.90000	2.00000	97.10000
SD 10075	14	2.30000	-2.00000	2.30000	98.00000
A11	27	2.30000	-1.90000	2.30000	98.10000
VCC					
SD 10076	6	1.00000	-0.70000	1.00000	99.30000
A3	15	1.30000	-0.10000	1.30000	99.90000
A3	14	1.30000	-0.20000	1.30000	99.80000
A3	19	1.50000	-0.10000	1.50000	99.90000
GND					
SD 10077	5	1.00000	-0.40000	1.00000	99.60000
A3	16	1.30000	0.00000	1.30000	0.00000
A3	13	1.30000	-0.10000	1.30000	0.10000
VCC					

RESET

A0	15	1.30000	-1.10000	1.30000	98.90000
A3	4	1.00000	-1.30000	1.00000	99.70000
B14	3	3.20000	-2.20000	3.20000	97.80000
B14	13	3.50000	-2.30000	3.50000	97.70000
A10	3	1.00000	-3.20000	1.00000	95.60000
B19	4	3.20000	-3.30000	3.20000	96.70000
B12	3	4.20000	-2.20000	4.20000	97.80000
B12	13	4.50000	-2.30000	4.50000	97.70000
A3	12	1.30000	-1.40000	1.30000	99.60000
B28	2	3.70000	-5.10000	3.70000	94.90000
B29	2	3.20000	-5.10000	3.20000	94.90000
SD 10078					
A11	3	2.00000	-2.20000	2.00000	97.80000
B28	1	3.70000	-5.00000	3.70000	95.00000
B29	1	3.20000	-5.00000	3.20000	95.00000
A5	13	1.30000	-1.30000	1.30000	99.70000

THE FOLLOWING IC PINS HAVE NO CONNECTIONS

IC	PIN	IC	PIN	IC	PIN	IC	PIN	IC	PIN
A10	3	B17	7	GND	5	GND	72	VCC	49
A10	4	B17	8	GND	6	GND	73	VCC	50
A10	5	B17	9	GND	7	GND	74	VCC	52
A10	9	B17	10	GND	8	GND	75	VCC	53
A10	10	B17	11	GND	9	GND	76	VCC	54
A10	11	B17	13	GND	10	GND	77	VCC	55
A10	12	B17	15	GND	11	GND	78	VCC	56
A10	13	B28	3	GND	12	GND	79	VCC	57
A11	4	B28	4	GND	13	GND	80	VCC	58
A11	10	B28	5	GND	14	GND	81	VCC	59
A11	11	B28	6	GND	16	GND	82	VCC	60
A12	4	B28	7	GND	18	GND	83	VCC	61
A12	10	B28	8	GND	20	GND	84	VCC	62
A12	11	B28	9	GND	23	GND	85	VCC	63
A13	4	B28	10	GND	24	GND	86	VCC	64
A13	5	B28	11	GND	25	GND	87	VCC	65
A13	6	B28	12	GND	30	GND	88	VCC	66
A13	7	B28	13	GND	31	GND	89	VCC	67
A13	8	B28	14	GND	32	GND	90	VCC	68
A13	9	B28	15	GND	33	VCC	1	VCC	69
A13	10	B28	16	GND	34	VCC	2	VCC	70
A13	11	B29	3	GND	35	VCC	3	VCC	71
A13	12	B29	4	GND	36	VCC	4	VCC	72
A13	13	B29	5	GND	37	VCC	5	VCC	73
A13	14	B29	6	GND	38	VCC	6	VCC	74
A13	15	B29	7	GND	39	VCC	7	VCC	75

A14	1	B29	8	GND	41	VCC	9	VCC	74
A14	4	B29	9	GND	42	VCC	12	VCC	77
A15	7	B29	10	GND	43	VCC	14	VCC	78
A16	6	B29	11	GND	44	VCC	15	VCC	79
A16	8	B29	12	GND	45	VCC	16	VCC	80
A18	13	B29	13	GND	46	VCC	17	VCC	81
A18	16	B29	14	GND	47	VCC	18	VCC	82
A19	2	B29	15	GND	48	VCC	19	VCC	83
A19	4	B29	16	GND	49	VCC	20	VCC	84
A19	6	B6	2	GND	50	VCC	22	VCC	85
A19	8	B6	4	GND	51	VCC	23	VCC	86
A19	9	B6	6	GND	53	VCC	24	VCC	87
A19	11	B6	8	GND	54	VCC	25	VCC	88
A19	13	B6	9	GND	55	VCC	29	VCC	89
A19	15	B6	11	GND	56	VCC	30	VCC	90
A3	1	B6	13	GND	57	VCC	31		
A3	2	B6	15	GND	59	VCC	32		
A5	14	B8	2	GND	60	VCC	34		
A5	15	B8	4	GND	61	VCC	35		
A5	16	B8	6	GND	62	VCC	36		
A6	4	B8	8	GND	63	VCC	37		
A6	10	B8	9	GND	64	VCC	38		
A6	11	B8	11	GND	65	VCC	41		
A8	13	B8	13	GND	66	VCC	42		
A8	16	B8	15	GND	67	VCC	43		
B14	10	GND	1	GND	68	VCC	44		
B17	2	GND	2	GND	69	VCC	46		
B17	4	GND	3	GND	70	VCC	47		
B17	6	GND	4	GND	71	VCC	48		

SIGNALS AT IC PINS (PINS IN CONSECUTIVE ORDER)

A10	• SD 10006, SD 10006, , SD 10005,	• SD 10012, SD 10011, SD 10004, .
A11	• SD 10045, SD 10059, SD 10078, SD 10075,	• SD 10074, SD 10074, SD 10074, SD 10074, SD 10074,
A12	• SD 10025, SD 10024, SD 10033, SD 10032,	• SD 10030, SD 10030, SD 10031, SD 10030, SD 10030,

A13	, SD 10008,	SD 10045,	SD 10001,	, ,	SD 10022,	, ,	, ,	, ,	, ,
A15	, ,	SD 10010,	SD 10017,	, ,	SD 10009,	SD 10012,	, ,	SD 10012,	, ,
A16	, SD 10053,	SD 10042,	SD 10055,	SD 10056,	SD 10017,	, ,	SD 10058,	, ,	SD 10044, SD 10046,
	SD 10053,	SD 10057,	SD 10024,	SD 10057,					
A18	, SD 10018,	SD 10048, RESET	, ,	SD 10013,	SD 10020,	SD 10017,	SD 10020,	SD 10019,	SD 10054, SD 10044,
	SD 10021,	SD 10056,	, ,	SD 10021,	SD 10015,	, ,			
A19	, SD 10007,	, ,	SD 10002,	, ,	SD 10003,	, ,	SD 10010,	, ,	SD 10014,
	, SD 10015,	, ,	SD 10014,	, ,	SD 10013,	, ,			
A3	, ,	, ,	SD 10023, RESET	, ,	SD 10077,	SD 10052,	SD 10042,	SD 10076,	SD 10020, SD 10021,
	SD 10073, RESET	, ,	SD 10025,	SD 10076,	SD 10076,	SD 10077,			
A5	, SD 10007,	SD 10008,	SD 10045,	SD 10046,	SD 10001,	SD 10002,	SD 10007,	SD 10009,	SD 10006, SD 10005,
	SD 10004,	SD 10011,	SD 10078,	, ,	, ,	, ,			
A6	, SD 10047,	SD 10048,	SD 10052,	, ,	SD 10044,	SD 10049,	SD 10050,	SD 10049,	SD 10044,
	, SD 10049,	SD 10049,	SD 10051,						
A8	, SD 10028,	SD 10023,	SD 10008,	SD 10026,	SD 10025,	SD 10027,	SD 10026,	SD 10029,	SD 10027, SD 10044,
	SD 10024,	SD 10014,	, ,	SD 10001, RESET	, ,	, ,			
B12	, SD 10065,	SD 10066, RESET	, ,	SD 10068,	SD 10059,	SD 10067,	SD 10055,	SD 10069,	SD 10071, SD 10047,
	SD 10067,	SD 10068, RESET	, ,	SD 10071,	SD 10072,	SD 10068,			
B14	, SD 10035,	SD 10036, RESET	, ,	SD 10039,	SD 10033,	SD 10041,	SD 10042,	SD 10040,	SD 10044,
	SD 10041,	SD 10039, RESET	, ,	SD 10037,	SD 10038,	SD 10039,			
B17	, SD 10062,	, ,	SD 10062,	, ,	SD 10060,	, ,	, ,	, ,	, ,
	, SD 10061,	, ,	SD 10066,	, ,	SD 10061,	, ,			
B19	, SD 10063,	SD 10043,	SD 10059, RESET	, ,	SD 10060,	SD 10062,	SD 10062,	SD 10064,	
B28	, SD 10078, RESET	, ,	, ,	, ,	, ,	, ,	, ,	, ,	, ,
	, ,	, ,	, ,	, ,	, ,	, ,			
B29	, SD 10078, RESET	, ,	, ,	, ,	, ,	, ,	, ,	, ,	, ,
	, ,	, ,	, ,	, ,	, ,	, ,			
B6	, SD 10070,	, ,	SD 10072,	, ,	SD 10070,	, ,	SD 10065,	, ,	SD 10064,
	, SD 10066,	, ,	SD 10071,	, ,	SD 10071,	, ,			
B8	, SD 10034,	, ,	SD 10039,	, ,	SD 10034,	, ,	SD 10038,	, ,	SD 10037,
	, SD 10037,	, ,	SD 10036,	, ,	SD 10036,	, ,			

GND	SD 10022	SD 10031		SD 10029	SD 10049	SD 10019	SD 10074	SD 10074	
		SD 10069				SD 10030	SD 10074	SD 10052	SD 10040
							SD 10061		
GND						SD 10050			SD 10043
VCC	SD 10016	SD 10077					SD 10028		SD 10010
	SD 10032	SD 10034			SD 10051	SD 10075	SD 10057		
				SD 10070				SD 10034	SD 10044
	SD 10068								
VCC									

X VALUES RANGE FROM -5.00 TO -0.00 X-AXIS IS HORIZONTAL
Y VALUES RANGE FROM -5.10 TO .10 Y-AXIS IS VERTICAL

NUMBERS 1-9 ON THIS GRAPH REPRESENT THE NUMBER OF POINTS AT THAT SPOT
"M" INDICATES THAT THERE ARE MORE THAN 9 IDENTICAL POINTS AT A SPOT

153 PINS WITH 1 WIRES
59 PINS WITH 2 WIRES
1 PINS WITH 5 WIRES

06/21/78 RENDIA *CYBER 174* NORMAL 07.42.00.SCOPE 3.3E
14.41.34JS131AM 06/21/78
14.41.34JS131.0131-07380-32-UA1840A103.50AMFS.T?
14.41.34.00.P3.
14.41.34.SWITCH.1.
14.41.34.SWITCH.2.
14.41.34.REGIN.YRRAP.
14.41.35.ATTACH.YRRAP.WIREWRAP.
14.41.35.CYCLE 30. WIREWRAP
14.41.35.FILE HAS BEEN ATTACHED
14.41.35.ATTACH.MLPF.ICDEFLIR.
14.41.36.CYCLE 09. ICDEFLIR
14.41.36.FILE HAS BEEN ATTACHED
14.41.36.COPY.MLPF.TAPE21.
14.41.36.REWIND.TAPE21.
14.41.36.MAP.OFF.
14.41.36.DISPOSE.TAPE12.*PR.
14.41.36.EOJ DISPOSITION SPECIFIED. KY IGNORED
14.41.36.DISPOSE.TAPE7.*PR.
14.41.37.EOJ DISPOSITION SPECIFIED. KY IGNORED
14.41.37.REQUEST.MLF.*AX30.OV.
14.41.37.YRRAP.
14.42.46.DISPOSE.PTAPE.OC=CAM. (INTERNAL)
14.42.47.STOP
14.42.47.REWIND.TAPE7.TAPE12.
14.42.47.COPY.TAPE12.OUTPUT.
14.42.49.IF.SSW.-2.1.
14.42.49.*COPYSRF.TAPE7.OUTPUT.
14.42.49.DISPOSE.TAPE12.
14.42.49.DISPOSE.TAPE7.
14.42.49.IF.SSW.-1.1.
14.42.50.*DISPOSE.OUTPUT.*PR=C.
14.42.50.REVERT.
14.42.50%CS 00000005324K CORE-SECONDS
14.42.50%CPA 004.216 SEC.
14.42.50%CPB 006.859 SEC.
14.42.50%RI 001.279 SEC.
14.42.50%RO 001.637 SEC.
14.42.50%NB 010.000 SEC.
14.42.50%PP 027.344 SEC.

* * * * JS131AM END OF LIST * * * *

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R. Caudle, DOE-MA, Washington, DC	2
V. C. Vespe, DOE-ALO	3
J. A. Freed, LASL	4
S. J. Buginas, LLL	5
H. M. Brinkmeier, Monsanto	6
D. H. Weingarten, SLA	7
J. H. Swafford, D/100, 1A44	8
D. H. Bahm, D/131, FC39	9
W. W. Davis, D/131, FC39	10-14
J. A. Dimarco, D/131, 2C39	15
R. C. King, D/131, FC39	16
W. E. Simes, D/131, FC39	17
R. E. Schmidt Jr., D/131, FC39	18
J. E. Long, D/531, 1A46	19
H. T. Barnes, D/554, BD50	20-21
L. Stratton, D/554, 2C44	22-24
C. R. Beary, D/755, 1A42	25
R. P. Frohmberg, D/800, 2A39	26
W. H. Deterding, D/814, 2C43	27
M. L. Smith D/821, 2D39	28
E. A. Kroencke, D/862, 2A47	29
R. E. Kessler, D/865, 2C40	30

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ELECTRICAL: Computer-Aided Design

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