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A PROTOTYPE CCD SYSTEM FOR THE TIME PROJECTION CHAMBER*

D. L. Fancher, K. L. Lee, J. Mallet,[§] P. Martin,
and G. Shapiro†

Abstract

A prototype sixteen channel charge-coupled device (CCD) system has been constructed for use with the prototype Time Projection Chamber (TPC) installed at the Bevalac at LBL. The system stores and digitizes analog pulse height information as a function of time from a set of proportional wires or cathode pads and provides the TPC with a true three-dimensional spatial readout. The performance of the system was found to be comparable to that of an equivalent ADC system.

I. Introduction

The Time Projection Chamber (TPC) to be installed at the Positron-Electron Project (PEP) at Stanford, California, is a new type of charged-particle detector that provides particle identification through ionization loss sampling as well as three-dimensional particle trajectory measurement. The principle of operation of the TPC is illustrated in Fig. 1. Ionization electrons left by a charged particle traversing a gaseous medium drift to the proportional wires under the influence of parallel electric and magnetic fields.¹ The magnetic field allows a measurement of the particle momentum as well as reducing transverse diffusion of the drifting electrons. Referring to Fig. 1, the coordinate Y, perpendicular to the wires but in the wire plane, is measured by the wire number. The coordinate X, along the proportional wires, is measured by cathode induction pads under the proportional wires. The performance of these pads is the subject of another paper.⁷ The third coordinate, Z, the drift direction, is measured from the drift time. The proportional wires also provide an energy loss sampling measurement for particle identification from the measurement of the pulse height on each of the wires (ionization loss or dE/dx sampling).

Fig. 1. Principle of operation of the TPC. Drifting electrons are captured by proportional wires. Induction pads measure the coordinate X. The wires give a measure of the coordinate Y as well as providing energy loss information. The drift time t gives a measure of the coordinate Z.

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To test the TPC concept, a prototype TPC system was constructed and installed at the Bevalac at LBL. The prototype had 192 sense wires (and hence 192 dE/dx samples) spaced 4 mm apart, eight rows each consisting of sixteen $7.5 \text{ mm} \times 7.5 \text{ mm}$ cathode pads, and a maximum drift distance of 10 cm. A drift electric field of $E/p = 0.2 \text{ Volts/cm/torr}$ was used along with a magnetic field of 8 kilogauss. A readout system that could preserve the pulse height information on the wires (for dE/dx ionization energy loss measurements) as well as measure the arrival time of the ionization electrons was needed. A readout system employing CCD's was developed for this purpose. The CCD acts as an analog shift register which samples input charge (i.e., pulse height) and shifts the charge along a linear array of charge storage cells, or "buckets", in response to an external clock. The clock can be fast during sampling (13 MHz) and slow during read out (110 kHz) to permit good resolution (76 nsec) and yet allow conventional ADC's to be used to digitize the data. A CCD delay line with sufficient buckets (455) can thus store the entire analog history of a single readout element for more than the time it takes the data from an event to drift the full distance of the TPC. A sixteen channel prototype CCD readout system using 455 bucket CCD's with a sampling frequency of 13.123 MHz and a readout frequency of 110 kHz was constructed which could be connected either to sixteen proportional wires or to each of sixteen induction pads in a single row. Both configurations were tested.

II. The Prototype System

The prototype system is shown in Fig. 2.

Fig. 2. Schematic of the CCD system (CCD-ADC module, clock module and buffer memory module) as installed in the TPC system.

The charge collected on the wires is amplified by low noise FET preamplifiers located at the chamber and transmitted on twisted pairs and coaxial cables to shaper-amplifiers located about three meters away. The outputs of shaper-amplifiers are sent via a twenty meter long cable to the buffered CCD module. The CCD units will be discussed in more detail later.

In operation, the readout samples the ionization waveform and stores the sampled pulse heights in the CCD. The output of the CCD is digitized by an ADC after having been transferred the length of the shift register. After a fast signal (trigger)

indicating the presence of a track, the input signal is sampled and stored at the fast rate (13.123 MHz) for a time that is greater than the maximum drift time possible for an event after a fast trigger. Then the CCD is read out at the lower frequency (110 kHz) and digitized by a low cost ADC. The digital information is stored on magnetic tape for later analysis. Figure 3 illustrates the sampling nature of the CCD. Figure 3a shows the input waveform and Figs. 3b and 3c show the sampled waveform for two different clock phases with respect to the fast track-indicating signal (trigger). The CCD samples the input waveform over a narrow period of time (about 6 nsec) on the negative-going transition of the clock.

Fig. 3. Illustration of CCD sampling of input waveform (a), and two output waveforms, (b) and (c), from two different clock phases.

The sampling of Fig. 3 is rather coarse; only three or four samples (or "buckets") of the waveform are stored. The prototype CCD system had variable width unipolar shaper-amplifiers. Data was taken with the shaper-amplifiers set for two different widths; resulting in 7 and 15 samples (on the average) per track. Figure 4 is an online picture of one event from one CCD channel located on a pad.

Fig. 4. Online picture of a single CCD sample. Each vertical line is one CCD bucket and the height of each line is proportional to the charge stored in that bucket.

The horizontal axis of Fig. 4 corresponds to time. The proportional wire gain of the chamber at the time that Fig. 4 was taken was only a few hundred. The gain of the shaper-amplifier was raised to provide the same net gain for the system as for normal data taking, which was done at a wire gain of several thousand with a correspondingly smaller amplifier gain. As a consequence, the noise in Fig. 4, as illustrated by the variation in buckets before and after the peak, is considerably worse than for normal data taking. Data were taken with both values of the wire gain. The results will be discussed later.

Referring back to Fig. 2, the CCD readout system consists of three modules; the CCD-ADC module, the clock module and the buffer memory module. The CCD's continually sample the input waveform. But only after an event trigger to the clock module does the readin process start. After shifting signals into the CCD for a predetermined number of fast clock cycles, the clock is slowed to the readout frequency and the output of the various CCD channels are multiplexed and digitized by four 8-bit ADC's. Four CCD channels are multiplexed to each ADC. The ADC outputs are transmitted serially to a CAMAC buffer memory module (BMM). The BMM demultiplexes the data and converts the serial 8-bits to a parallel 8-bit wide by 64 word long FIFO memory. Sixty-four buckets of each of the sixteen CCD channels are digitized. (For the Bevalac chamber, the maximum drift distance corresponded to about twenty buckets of sampling at the fast clock rate.) After all 64 buckets are

digitized, the FIFO's are read out onto the CAMAC dataway.

The clock module is used to generate the CCD and readout clocks, as well as provide the timing signals for the other two modules. The clock module has considerable flexibility in order to study the CCD performance under a variety of operating conditions. Scalers in the clock module can be preset via the CAMAC dataway, providing a variety of readout modes. The readout frequency can be varied from 110 kHz to 12 kHz via the read/divide counter. The time between the trigger and first bucket (sample) that is digitized (only 64 of the 455 buckets of the CCD are digitized) can be varied via the overall counter and the sample counter. The time between the trigger pulse and the switch from sampling frequency to readout frequency can be varied via the sample counter. Slowing down the clock earlier during the readout increases the dark current and permits measurement of dark current variations. Normally, the first 64 samples taken after a trigger has occurred are digitized and the first of those 64 samples is clocked through the complete 455 buckets at the high rate. This minimizes the dark current. It is possible, however, to clock the buckets through at rates as low as 12 kHz, and to start digitizing samples either before or after the trigger is received. Digitization can start up to 60 clock periods before the trigger. This allows a delayed trigger to be used.

Figure 5 is a schematic of the analog section of the CCD system as used in our system.

Fig. 5. CCD analog circuitry, showing biases and clock shape.

Each CCD channel is AC coupled. The linear region of each CCD is about ± 1 volt, but biased above ground. In Fig. 5, an input bias is set via V_2 (common to all 16 channels). An individual input bias for each chip, V_1 , can be varied to optimize and match the performance of the individual channels. An output bias, V_{os} , can be used to provide a pedestal for each channel. V_{os} is common to all 16 channels.

The gain of the CCD channels varied by 10% from channel to channel. The buffered attenuators of Fig. 2 are used to match the gain of each channel to that of the channel with the lowest gain as well as to terminate the long cable run from the shaper-amplifier in order to minimize reflections.

Figures 6 and 7 are photographs of the CCD prototype system.

Fig. 6. The CCD modules: from left to right; the buffer memory module (CAMAC); clock module (CAMAC) and the CCD-ADC module (NIM).

Fig. 7. Inside the CCD-ADC module. The ADC's are on the hinged board. The CCD chips are eight light-faced chips in a row near the bottom of the installed board.

BEVATRON DATA ACQUISITION SYSTEM

III. CCD System and Chip Performance

The chips used were Fairchild 321A's.³ Each chip contains two shift registers of 455 buckets each. The sampling frequency was 13.123 MHz and the readout frequency was 110 kHz. The input waveform width was set to give five or six samples of the input charge. The number of samples per event should be small, in order to improve the two-track resolution and to minimize the total amount of data. Even with the relatively coarse sampling (~7 samples/waveform) the measured area of the pulse (total charge) was constant to within 1% (measurement error = 1%) for any clock phase with respect to the appearance of a signal on a proportional wire or induction pad. No distortions or nonlinearities have been observed at the 1% (of full scale) level. The resulting time resolution (and hence spatial resolution) will be discussed later. Figure 9 shows the linearity of two CCD channels as measured with a pulser used to induce signals on sense elements (wires or pads).

Tests were performed on the CCD chips themselves to check the measured specifications.³ The RMS noise of the CCD's was measured to be between 1/500 and 1/700 of the maximum input signal, depending on the particular chip. This is equivalent to a dynamic range of at least 54 db. The transfer efficiency was measured to be between 93% and 94% for 455 transfers at 13 MHz yielding an individual cell transfer efficiency of 99.985% at this frequency. This agrees with other measurements done at LBL.⁴ An 8-bit ADC was used and its resolution was the limiting factor in determining the performance of the CCD system.

Another potential drawback to a CCD system is dark current. As the charge is shifted from bucket

to bucket through the CCD, the dark current is shifted and added to the noise of the subsequent buckets. Thus, the real signal appears to be superimposed on a rising background. The slope of the background is a characterization of the dark current. The dark current in the CCD was studied extensively. Measurements of the dark current were made as a function of temperature and readout frequency. It was found that by providing a pedestal on the output of the CCD (see Fig. 5), the dark current variations could be reduced considerably at the expense of slightly reduced dynamic range. For a typical CCD channel, a pedestal of 20 counts (out of 256 total for the ADC), reduced the dark current to about 2 mv/msec at 20°C while reducing the dynamic range by about 8%. For the readout speed used, this corresponded to a baseline shift of less than 1/2 a count from beginning to end of readout. Cooling the CCD below 20°C did not improve this figure appreciably, so the CCD's were run at 20°C during the Bevalac data taking.

IV. Bevatron Data-Taking

After bench tests, the CCD prototype system was installed with the TPC prototype at the Bevalac in a real data-taking environment. The CCD's were coupled either to 16 wires or 16 pads of the Bevalac TPC prototype.⁶ The chamber was tested in particle beams of 1.8 GeV/c and 0.8 GeV/c protons, pions, and positrons. The CCD's were tested with two different input amplifier shaping times (corresponding to 7 and 15 bucket sampling) and with two different chamber wire gains (~300 and 2400).

Figures 10 and 11 are online pictures of typical two-track events. For both pictures, the CCD's were coupled to proportional wires. Figure 10 shows the pulse height per bucket for the 64 buckets read out for two CCD channels. Figure 11 is another view of a two-track event, showing the pulse height (size of dots) for all 16 channels (vertical rows of dots) for all buckets (each dot is one bucket).

Fig. 10. CCD bucket amplitude vs bucket number for a two-track event.

Fig. 11. Representation of the CCD bucket amplitudes for all 16 CCD channels for a two-track event. The brightness of each dot is proportional to the charge in each bucket.

Figures 12 (CCD) and 13 (ADC) are a comparison of Fe^{55} x-ray spectra taken with the CCD and ADC systems on the same wire. The 5.9 keV main peak and the 3.0 keV escape peak are clearly seen in both figures.

Fig. 12. Fe^{55} spectra on a wire as measured by the CCD system. The abscissa is the pulse heights as measured by the CCD and the ordinate is the number of events.

Fig. 13. ^{55}Fe spectra on a wire as measured by the ADC system. The pulse height is plotted on the abscissa and the number of counts is on the ordinate. The large spike superimposed on the smaller peak (escape peak) is from a pulser used to monitor electronic drifts.

Figure 14 shows the variation in the CCD pedestal over a run. The CCD pedestal was determined by averaging over unoccupied CCD buckets.

Fig. 14. Distribution of CCD pedestals for two CCD channels.

The FWHM of the pedestal was two counts (out of 256) or less for all the CCD channels.

Finally, Fig. 15 is a scatterplot for several events of the pulse height on a cathode pad as measured by both the CCD system and the ADC system.

Fig. 15. Pulse height measured with the CCD's versus pulse height measured with the ADC's for a cathode pad in the TPC prototype chamber.

The data were analyzed and a comparison of the response of the CCD's and the ADC's to the proportional wire signals was made to see if the CCD's would degrade measurements made with the ADC readout of the prototype TPC. Three main areas were studied. With the CCD's connected to 16 proportional wires, the measurement of energy loss (dE/dx) for particle identification purposes was compared to that obtained from the ADC's. Results are given here for 1.8 GeV/c protons. The results are preliminary in that the data have only been corrected for electronic gain variations and not for such effects as wire gain variations, momentum spread in the beam, dip angle, variations in particle trajectories, etc.

With the CCD's connected to a row of induction pads, the measured position resolution obtained from the CCD's was compared with that obtained from the ADCs. This was done for 0.8 GeV/c protons.

Finally, with the CCD readout attached to the proportional wires, the time resolution (and hence spatial resolution in the drift direction) as determined by the CCD's was measured.

In all cases, the CCD's were found not to degrade the system performance measurably when compared to the signals processed by the ADC's.

a) dE/dx comparison

Since only 16 proportional wires were read out by the CCD's, full "events" of 192 samples each were simulated by adding 12 such 16 wire events together. The same signals were added together in the same way after processing by the ADC, and the two measurements compared. Single wire pulse height distributions were also compared.

Figure 16 shows the raw single wire pulse height distribution for particles for a single wire as

measured by the ADC. Figure 17 is the same quantity after processing by the CCD sytem.

Fig. 16. Single wire pulse height distribution for 1.8 GeV/c particles as measured by an ADC.

Fig. 17. Single wire pulse height distributions for 1.8 GeV/c particles as measured by a CCD.

In both cases, the FWHM of the distribution is about 75%. A single sample of ionization is insufficient to determine particle identification. For good particle identification, many samples (in our case, 192) of a single track are taken. An algorithm can then be used to optimize particle identification from these samples. The algorithm used here is a simple one. 30% of the ionization samples with the largest pulse heights are discarded and the average pulse height of the 70% remaining samples is used as an estimator of the most probable ionization. We call this the truncated mean.

The truncated means for 1.8 GeV/c protons as processed by the ADC system and the CCD system were computed. Figure 18 shows the correlation between the ADC-measured and the CCD-measured resolution. The measured resolution is 3.2% for the ADC and 3.4% for the CCD. These are equivalent for the statistics shown. The correlation between the CCD-measured and the ADC-measured values is very good, indicating that both systems are measuring the same quantity with the same effectiveness. The CCD system does not appear to degrade the particle identification capabilities of the prototype TPC compared to that obtained with an ADC system.

Fig. 18. Correlation between ADC and CCD truncated mean for 1.8 GeV/c protons.

b) Position Resolution

For the position resolution comparisons, a pad row in the center of the chamber was read out through the CCD's. Tracks from 0.8 GeV/c protons were the source of the input signals. For each track, the pulse height distribution on the pads of each row was fit, event by event, to find the avalanche position along the proportional wires above the pads. The data from the seven pad rows not instrumented with CCD readout are fit to obtain the particle trajectory. The residual distribution of the fit has an RMS of 215 μ m. The residual is computed between this trajectory and the position determined from the pad row instrumented with the CCD's. This residual can be compared to the residual obtained between the measured trajectory and the position determined from the same pad row by the ADC. From these two residuals, along with the

resolution of the fit to the trajectory, a measure of how much the CCD's degrade the position resolution measurements can be made. For such a measure, the correlation between the CCD-measured position residuals and the ADC-measured position residuals must also be known. The resolution is $190 \mu\text{m}$ from the ADC measurement and $197 \mu\text{m}$ from the CCD measurement. From these numbers, the excess contribution to the resolution from the CCD is estimated to be $54 \mu\text{m}$. It should be noted, however, that the error in this number is comparable to the number itself. In any case, the CCD does not contribute significantly to the position resolution of the cathode pads.

Figure 19 shows the correlation between the CCD-measured and ADC-measured position residuals. The strong correlation indicates that both systems are indeed measuring the same quantity. Not all pertinent corrections have been applied to the data to obtain these preliminary results. The significant point is the strong correlation between the signal processing systems on a track-to-track basis as shown by Fig. 19 (and also Figs. 15 and 18). It should be noted that with full corrections, for earlier data taken with the ADC system only, a resolution of $100 \pm 3 \mu\text{m}$ ⁸ has been obtained for the cathode induction pads.

Fig. 19. Correlation between track position measurement error for the ADC system and track position measurement error for the CCD system.

c) Time Resolution

With the CCD's measuring the signals on the proportional wires, the time resolution of the CCD's was measured in the following manner. For each CCD channel, for each event, the pulse height, P , for the three buckets with the largest pulse heights was fit to a quadratic function of time, t .

$$P(t) = a + bt + ct^2$$

The time of the event was defined to be the time, t_{max} , at the maximum of this function.

$$\frac{dP(t_{\text{max}})}{dt} = 0.$$

After t_{max} was determined for each of the CCD-measured proportional wires, a straight line (track) was fit to t_{max} versus wire number except for the data from one wire, and the difference between the fit time and the t_{max} calculated for that remaining wire was computed. The RMS of these residuals were found to be about 2.5 to 3.2 nsec for the different CCD channels which corresponds to a position resolution of 150 to 200 μm for a drift velocity of 6 cm/ μsec . This position resolution corresponds to better than 1/20th of a bucket width (76 nsec). The drift time was also measured independently by a TDC (time-to-digital converter) which measured the time between when a particle crossed the TPC and the time at which the ionization from that track reached the proportional wires. The correlation between the TDC and CCD measured drift times was found to be very good.

In conclusion, a CCD prototype system for the TPC has been constructed and tested in a particle beam. Preliminary results indicate that the CCD system performs as well as a conventional ADC system while providing very good time resolution. The CCD concept as employed by the TPC system appears to be a viable one.

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References

- (1) Proposal for a PEP Facility Based on the Time Projection Chamber, PEP-4, PUB-5012 (December 1976).
- (2) R. F. Althaus et al., "Large-Scale Digitizer System, Analog Converters", LBL-5357 (1976).
R. F. Althaus et al., "A Large-Scale Digitizer System (LSD) for Charge and Time Digitization in High-Energy Physics Experiments", LBL-5358 (1976).
- (3) CCD 321A, 455/910-Bit Analog Shift Register - Charge Coupled Device, Specifications, Fairchild, Mountain View, CA.
- (4) E. Yazgan and F. Kirsten, "Characterization of Charge-Coupled Analog Memories for Nuclear Data Acquisition", IEEE Trans. Nucl. Sci., NS-25, No. 1 (1978).
- (5) K. L. Lee, "CCD Clock Drivers With Large Amplitude, Fast-Switching and Low Power", IEEE Trans. Nucl. Sci., NS-25, No. 1 (1978).
- (6) D. Fancher, S. Loken, P. Martin, J. N. Marx, D. R. Nygren, P. Robrish, G. Shapiro, M. Urban, W. Wenzel, W. Gorn, and J. Layter, "The Dipole Time Projection Chamber", Sept. 1978, to be submitted to Nucl. Inst. and Methods.
- (7) D. L. Fancher and A. C. Schaffer, "Experimental Study of the Signals from a Segmented Cathode Drift Chamber", submitted to this conference.
- (8) G. Lynch, "A Study of Position Resolution in TPC Test Data", Oct. 1978, TPC internal report.

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