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**SEMICRYSTALLINE CASTING PROCESS DEVELOPMENT AND
VERIFICATION**

Quarterly Progress Report Number 1 for the Period June 19—September 19, 1980

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Work Performed Under Contract No. FC01-80ET23197

Semix Incorporated
Gaithersburg, Maryland

U.S. Department of Energy

Solar Energy

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SEMICRYSTALLINE CASTING PROCESS DEVELOPMENT AND VERIFICATION

Quarterly Progress Report Number 1

June 19, 1980 - September 19, 1980

A Cooperative Agreement Between the United States
Department of Energy and Semix Incorporated
Cooperative Agreement No. DE-FC01-80ET 23197

Submitted By:

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INTRODUCTION

The world-wide industrial capacity for low-cost sheet material for solar cell substrates must be developed to reduce module cost and increase availability. In this spirit, Semix Incorporated and the United States Department of Energy have entered into Cooperative Agreement DE-FC01-80ET-23197, entitled, "Semicrystalline Casting Process Development and Verification."

Unlike a contract or a grant, a cooperative agreement is a unique marriage of public and private sector interests in which substantial cost and risk sharing takes place in order to optimally meet program goals. In this case, Semix has agreed to pay 22.2% of the cost of the agreement and will reimburse the Government, starting at the end of the agreement at the rate of 1% of net sales per year. In addition, if the program is successful, Semix is committed to make semicrystalline sheet commercially available. For its part, the DOE has agreed to waive all patent and technical data rights. Proprietary information will be restricted to key technical monitors from the DOE and the Jet Propulsion Laboratory (JPL) for verification and progress accounting of the work under the agreement.

The specific objectives of this cooperative agreement are:

1. To demonstrate Commercial Readiness of semicrystalline silicon sheet technology consistent with the United States Department of Energy photovoltaic array price goal of \$2.80/Wp. (1980\$) by 1982.
2. To demonstrate Technology Readiness of semicrystalline silicon sheet technology consistent with the United States Department of Energy photovoltaic array price goal of \$0.70/Wp. (1980\$) by 1986.

A flow chart of the component processes of module assembly and process price allocations required to meet module cost goals is shown in Figure 1. Although this program encompasses only the silicon sheet manufacture step, the advantages of the Semix Ubiquitous Crystallization Process (UCP) support potential reductions in costs at each process step:

Silicon Feedstock - The Ubiquitous Crystallization Process (UCP) has a high tolerance to low-cost less pure silicon.

Sheet Manufacture - As will be demonstrated, the UCP lends itself well to automation, utilizes relatively low energy, and has overall low operating costs.

Cell Fabrication - The UCP can manufacture wafers with large areas, lowering the per watt cell fabrication costs.

Encapsulation Materials - Rectangular wafers which can be packaged with >95% packing density will lower the per watt amount of encapsulation material and cost.

Module Assembly - Again, the high packing density and large sheet area will lower the materials and labor requirements and hence, association module costs.

The technical attributes of semicrystalline sheet material produced by the Ubiquitous Crystallization Process are the result of years of in-house development, first by Solarex Corporation and later by Semix Incorporated. Initial devices fabricated in the laboratory yielded 8-9% AM1 efficiencies¹. By 1976 the

Figure 1

PROCESS FLOW AND PRICE ALLOCATION

1982¹ \$2.80/WP (MODULE)
1986² \$.70/WP (MODULE)

1. PRICE ALLOCATION GUIDELINES
J.P.L. LOW CAST SOLAR ARRAY 5101-68
R.W. ASTER, MAY 12, 1978
2. PRICE ALLOCATION GUIDELINES
J.P.L. LOW COST SOLAR ARRAY 5101-68 - REVISION A
R.W. ASTER, JANUARY 15, 1980

technology had been improved and a device with 10% AM1 conversion efficiency was reported. Two years later, in 1978, a 2 x 2 cm cell achieved 16% AM1 conversion efficiency³, independently verified by the Jet Propulsion Laboratory (JPL). In 1980, a 17% AM1 2 cm x 2 cm cell was demonstrated and at present 10 x 10 cm cells are being produced with efficiencies ranging from 10-14% at AM1.

During the early stages of this program specific technical elements will be confirmed through a thorough analysis of semicrystalline material, including cell efficiency, material and process yields, mechanical stability and crystallographic structure, which allow semicrystalline silicon to contribute to the national energy program to its maximum potential.

The primary thrust of the Semix/DOE program commences from the point of the present Semix proprietary technology with the purpose of developing low cost silicon sheet manufacturing techniques and verifying these techniques within a small scale Experimental Process System Development Unit (EPSDU). This EPSDU will be a test bed for evaluating prototype production tools and methods within the UCP, wafering and quality control process steps required to produce finished wafers from polycrystalline silicon feedstock. The EPSDU will be carefully controlled and monitored to conduct manufacturing experiments and parametric variations aimed at optimizing productivity. With its own funds, Semix will upscale existing production facilities and technology compatible with the 1982 goals, implementing the technology innovations and developments which will emanate from the Semix/DOE program.

The Semix/DOE Cooperative Agreement spans three years and is divided into three phases. Phase I will aim at designing and developing the tools needed to demonstrate, in 1980 dollars, compatibility with the \$2.80/Wp Commercial Readiness 1982 module

cost goals and \$0.70/Wp Technology Readiness 1986 module cost goals. In addition, extensive material evaluation is planned and continuing economic analyses will be performed to insure that equipment designs meet target requirements. Work being carried out under Phase I is divided into the following tasks:

- I. Proof-Of-Concept
- II. Performance Analysis
- III. High Temperature Systems Development
- IV. Wafering and Mechanical Systems Development
- V. Auxiliary Systems Development

This quarterly report is subdivided by task, with each section detailing the work performed under that particular task.

The first quarter has proceeded successfully, highlighted by organization of the Program Plan, and design, construction, and commencement of experimentation with a prototype crystallization system. Also, the design of a second prototype system was begun as well as experimentation with multi-blade slurry sawing technology.

SECTION I

PROOF-OF-CONCEPT

Semicrystalline silicon has been under development for a number of years emerging as a viable, low-cost alternative to single crystal silicon for solar cell manufacture.¹⁻³ Photovoltaic conversion efficiencies up to 17% AM1 have been reported in the literature⁴ using this material.

Semicrystalline silicon has been described⁵ as a specific state of polycrystalline silicon which is characterized by:

- o grain size of at least a few millimeters
- o high crystal order within grains, with lifetimes of many microseconds
- o non-conductive grain boundaries

Because of the polycrystalline nature of the Semix material it is evident that a much greater crystallographic variability, through the introduction of grain boundaries, crystallographic grain orientation, and internal grain order, will be present than with single crystals. It is material produced within this range of variability, experienced in normal production, that is the subject of this study.

It is the intent of part of this task to explore and place in perspective the strength and limitations of polycrystalline silicon for photovoltaic applications. Areas to be investigated will include:

- o the effects of grain size on cell efficiency
- o the effects of grain boundaries on the electrical properties of devices
- o the structural properties of semicrystalline wafers
- o the effects of random crystallographic grain orientations on cell performance

During this first quarter, a program for the Proof-of-Concept task was developed. The work outlined in this task will lead to the structural, mechanical, and electrical characterization of Semix UCP semicrystalline silicon.

In addition, this task will study the cost potential of Semix semicrystalline sheet in order to demonstrate its commercial and technology readiness to meet DOE 1982 and 1986 price goals of \$2.80 and \$0.70 per watt respectively. This program is broken down into the areas of material evaluation and economic and technical considerations.

Material Evaluation

During the early development of semicrystalline silicon there was concern that grain boundary conduction would tend to shunt a diffused junction device, affecting its fill factor by lowering the voltage at maximum power. It had been found that this is not the case⁵. This conclusion is confirmed here by Figure 1.1 which shows the spread in the light I-V curves for co-processed single and semicrystalline cells. The sets of cells are essentially the same with equivalent fill factors and maximum power voltages. The short circuit current is slightly lower for the

Figure 1.1 A typical range of variation in light I-V characteristics for co-processed lots of semicrystalline and single crystal solar cells, using a base line process developed for reproducibility.

semicrystalline material. This results in part from the lower base resistivity for this material (0.8 ohm-cm versus 2-3 ohm-cm) and in part from grain boundary recombination. However, neither one of these mechanisms affect the shunting characteristics of a cell. Thus, the state of the technology is such that under identical processing conditions both single and semicrystalline wafers will produce diffused junction devices with similar high shunt resistances.

This is not to say, however, that grain boundaries have no effect. For example, diffusants may proceed along grain boundaries. Figures 1.2a and 1.2b are photomicrographs of a semicrystalline diffused n on p junction device that has been angle lapped and stained using a copper sulfate solution to differentiate the n^+ regions. Figure 1.2a is a photomicrograph of a region in the cell containing [111] type twin boundaries. It can be seen that there is no penetration of the diffusant into the base region at this type of grain boundary. Figure 1.2b is a photomicrograph of a region in the cell containing a boundary between two crystallographically unrelated grains. In this case diffusant has penetrated about one micron into the base region. Since, however, these devices are on the order of 250-350 microns thick, there is no chance of this penetration of diffusant leading to a shunt in the device.

Another concern during the development of semicrystalline sheet material was that the grain boundaries, acting as areas of high recombination, would significantly reduce the photogenerated current. In order to predict the effect that a worst case (i.e. infinite) recombination velocity at a grain boundary would have on the short circuit current as a function of grain size, some theoretical modeling was undertaken⁶. In this model the grains

Figure 1.2a Optical Micrograph of an Angle Lapped/Stained Polysilicon Section Containing {111} Type Twin Traces

Penetration of
diffusant along
grain boundary

Figure 1.2b Optical Micrograph of an Angle Lapped/Stained Polysilicon Section Showing Junction Penetration at a Boundary Between Two Crystallographically Dissimilar Grains

were assumed to be right circular cylinders of radius R and that carriers generated closer to the grain boundaries than to the junction would recombine there and not contribute to J_{sc} , the short circuit current density. Also, it was assumed that there were no losses due either to reflection or to the existence of a dead layer in the n^+ region. Consequently, for the grain radius, R , being larger than the minority carrier diffusion length, L , the ratio of the current density collected from the grain to the current density collected when there is no grain boundary, J_L/J_L^T , is

$$1) \quad J_L/J_L^T = 1 + \frac{2}{\alpha R} \left(\frac{1}{\alpha R} - 1 \right) + \frac{e^{-\alpha L}}{1 - e^{-\alpha L}} \frac{L}{R} \left(2 - \frac{L}{R} - \frac{2}{\alpha R} \right)$$

where α is the absorption constant.

The optical generation rate of minority carriers in the bulk silicon decreases exponentially with depth from the surface ($g = F_0 e^{-\alpha z}$). Therefore, after reaching a depth of $z = \alpha^{-1}$ (commonly called the extinction length), almost two thirds of the minority carriers have already been generated within the bulk. Additionally, the majority of carriers which reach the junction come from within a distance $z = L$ of the junction. For $L > \alpha^{-1}$ most of the generated carriers will be collected at the junction, while for $L < \alpha^{-1}$ most of the carriers will never reach the junction. Thus, $L = \alpha^{-1}$ ($\alpha L = 1$) represents an effective transition point between the two regions. Figure 1.3 shows a plot of J_L/J_L^T as a function of R/L for $\alpha L = 1$ at 900 nm. The curve shows that for a grain size radius of 200 μm , J_L/J_L^T is at least 90%. For either longer diffusion lengths or larger values of the absorption constant ($\lambda < 900 \mu m$), J_L/J_L^T will

Figure 1.3 J_L/J_L^T versus R/L

be even closer to one. Therefore, grain boundaries have little influence on the collected current if the radius of the grains exceed $200\text{ }\mu\text{m}$, a dimension easily exceeded in solar cells fabricated from Semix UCP semicrystalline silicon.

In order to investigate the influence that the grain volume has upon the photogenerated response of a cell, a light spot scanning technique was employed.⁶ With this technique a light spot of approximately $60\text{ }\mu\text{m}$ in diameter is rastered across the face of a photovoltaic device and the output current of the cell is plotted as a function of the position of the light source. Figure 1.4 is such a trace for a section of a $2\text{ cm} \times 2\text{ cm}$ cell. Figure 1.5 is a sketch of the same area showing the locations of the grain boundaries. It can be seen from comparing these two figures that the two curved grain boundaries encompassing grain B are electrically active and lead to a decreased photoresponse at those locations. However, the straight line grain boundary completing the enclosure of grain B shows only a minimal change in the photoresponse. In addition it can be seen that one small area of grain A shows a rapid fluctuation in the photoresponse. Optically, no distinction can be made between different areas of the device. Thus, the technique of x-ray topography was used to investigate the structure within the grain volume. Figures 1.6a and 1.6b are Lang Transmission Topographs of grains A and B, respectively. The dark specks in grain A are inclusions and the light feathering lines are dislocations. By studying the dislocation pattern in the neighborhood of the inclusion it becomes evident that due to difference in the mechanical properties between the silicon and the inclusion, stresses have developed giving rise to the dislocation loops. By comparing Figure 1.6a with 1.4 it can be seen that the region of heaviest dislocation content is the region that has

Figure 1.4 Scanning Photoresponse Pattern of an Area of a 2cm x 2cm Cell Showing Grains A and B at $\lambda = 800 \text{ nm}$.

Figure 1.5 Sketch Showing Location of the Boundaries Between Grains A and B

Figure 1.6a $(20\bar{2})$ Lang X-ray Transmission Topograph of Grain A

Figure 1.6b $(2\bar{2}0)$ Lang X-ray Transmission Topograph of Grain B

the most significant change in photocurrent. Comparison of Figure 1.6b with 1.4 shows that the family of $\langle 111 \rangle$ type twins has no effect upon the photoresponse.

The variability of the crystallographic grain orientation across a wafer will manifest itself as a factor in determining diffusion characteristics and the attendant oxidation rate, which could potentially affect the distribution of cell parameters. Oxidation rate is primarily determined by the rate of diffusion of oxygen through the oxide to the silicon interface, and is not expected to be a strong function of orientation. This has been verified⁵ with visual and ellipsometric characterization, wherein total oxide thickness variation was found to be less than 5% for the wide range of crystallographic orientation present in the semicrystalline material, with no unusual effects noted.

To evaluate the effect of this range of crystallographic orientation upon diffusion characteristics, the sheet resistance of n^+ diffused layers has been measured for boron doped single and semicrystalline wafers. Typical results are shown in Figure 1.7.⁵ While a much greater range is present for the semicrystalline wafers, they are bracketed by values for the $[100]$ and $[111]$ single crystal wafers which were processed simultaneously and for which no anomalous behavior was noted. While the sheet resistance variability is higher than for single crystal wafers, this does not cause a significant variation in cell characteristics as can be seen from Figure 1.1.

Within this Proof-of-Concept task, more extensive analyses of the structure of Semix polycrystalline material will be carried out in order to gain a deeper understanding of the internal order within the individual grains, grain orientations, and the effects these have on device performance. A number of semicrystalline

Figure 1.7 Representative Variation in the Sheet Resistance of Semicrystalline Wafers Diffused Along With Single Crystal Controls

"bricks" are being selected for evaluation in this program with samples representing the top, middle and bottom of the "brick" being culled from each selected crystallization. Characterization techniques to be employed under these analyses include electron channelling, x-ray topography, deep level transient spectroscopy, secondary ion mass spectroscopy, angle lapping, fraction analyses and scanning electron microscopy.

Economic and Technical Considerations

Prior to the implementation of the Semix/DOE Cooperative Agreement, cost analyses by Semix and by JPL showed that the Ubiquitous Crystallization Process would provide a cost effective alternative material for solar cells. In June, 1979, JPL employed the DOE Standard Assembly-Line Manufacturing Industry Costing Standards (SAMICS) to project that using Semix material, photovoltaic modules could be produced for as low as 42.1 cents/Wp (1978\$) assuming cell efficiency of 15% AM1 in 1986. This is substantially lower than the 50 cents/ peak watt projected DOE target cost.

The basis for the JPL analysis was an upscaled version (250 MW/year capacity) of a technology currently employed by Semix. In order to be comparable to other sheet technology analyses, it was performed with all assumptions for wafering, cell processing, and panel production, exactly the same as in analyses previously run by JPL. Only those changes relating specifically to the UCP process itself were substituted.

The results of this analysis predict that panels can be built with semicrystalline material at well below the national goal in 1986:

45.6¢/Wp @ \$10/Kg Silicon (10 x 10 cm wafer size)
44.1¢/Wp @ \$ 8/Kg Silicon (10 x 10 cm wafer size)
42.1¢/Wp @ \$ 8/Kg Silicon (12 x 12 cm wafer size)*

*Much larger wafer sizes are technically feasible.

A cost breakdown of major cost elements in the 45.6¢/Wp JPL analysis is shown in Figure 1.8 illustrating the dominant role of sheet material in dictating module cost and underscoring the need to develop an inexpensive manufacturing process. The same analysis estimated that a futuristic Czochralski process could produce 60 cents/watt panels (1978\$). This is approximately a 43% increase over the 1986 estimated cost of panels made with semi-crystalline sheet material.

The major cost difference between the two processes are summarized in Table 1.1. The factors listed in the Table can be explained as follows:

- o Value Added: The simplicity of the automated UCP will result in higher productivity with less floor space, capital investment, energy, labor and direct material cost per kilogram of silicon produced;
- o Mass Yield: Semicrystalline bricks can be made into any shape required for direct wafering, with fewer grinding or other losses than those associated with Czochralski;
- o Impurity Tolerance: Natural purification takes place during crystal growth in the UCP, with impurities

FIGURE 1.8 Breakdown of Finished Module Costs,
Using UCP Semicrystalline Material*

* Based on JPL SAMIS
Analysis

TABLE 1.1 COMPARISON OF COST FACTORS RESULTING
FROM JPL SAMIS COST ANALYSIS

Cost Savings Element	Semicrystalline	Futuristic Czochralski
<u>UCP</u> 1. Value Added 2. Silicon Mass Yield 3. Impurity Tolerance	\$8/Kg 98% High	\$10/Kg. 81 - 85% Moderate
<u>WAFERING:</u> 1. Sawing Rate (SAMIS)	Flat top, constant cutting rate	Round Top, variable cutting rate
<u>CELL PROCESSING:</u> 1. Area	12x12cm = 144 cm ² * Comparable cell processing economics. Wafers have already been produced.	5.5" Dia. = 153.3 cm ²
<u>MODULE:</u> 1. Encapsulation Materials	Intrinsic square shape 96% packing density.	Round-78% packing density (Silicon mass yield drops as wafers are modified)
*Wafers of this size have already been fabricated; much larger ones are possible by 1986, resulting in further economies of scale.		

segregated out to the grain boundaries where they are inert. This should allow the use of cheaper, less refined starting material as well as recycling of silicon lost in other parts of the process*. (This is the reason for including \$8/kilogram silicon in the alternate SAMICS analyses, whereas JPL estimates that feed-stock silicon suitable for Czochralski growth will be available at \$10/kilogram at that time);

- o Sawing Rate: The consistent square cross section presented by the ingot during wafering allows a constant and much higher cutting rate per square centimeter than round Czochralski ingots, for which saw feed pressure and cutting vary considerably throughout the cut for the multi-blade slurry wafering technique;
- o Encapsulation Materials: Since the square or rectangular semicrystalline cells can be packed much tighter than round cells, much less material is required to build the module for the same cell efficiency;
- o Area Related Costs: Although not the subject of this analysis, the higher power density resulting from the tightly packed cells will result in substantial system level cost savings in such areas as array structural support, wiring, land, etc.

*The verification of this claim is not incorporated in the scope of work for this cooperative agreement.

The intent of the economic analyses to be performed within the Proof-of-Concept task, is to develop a baseline case for current technology (i.e. semiconductor grade Si feedstock) and to further substantiate the cost advantage of Semix UCP semicrystalline sheet material. This will be done through refining inputs to the SAMICS analysis as Semix's technology development moves toward meeting 1986 cost goals.

SECTION II

PERFORMANCE ANALYSIS

INTRODUCTION

It is the purpose of this task to measure the technical and economic performance of prototype systems developed during this program. To establish an electrical performance baseline for the Semix Ubiquitous Crystallization Process (UCP), single 4.2 kg semicrystalline bricks from the existing technology will be tested in order for material from new prototype systems to be measured against this standard. All material will be processed into 10 cm x 10 cm solar cells on a standard cell processing line at Solarex Corporation. In addition, basic economic and productivity measurements will be made for all new system designs to determine their cost effectiveness.

MATERIAL PERFORMANCE

The semicrystalline material to be used for this task will be produced in two of Semix's existing UCP systems. These two systems have been instrumented with platinum -6% rhodium versus platinum -30% rhodium (B-type) thermocouples which will directly monitor temperature changes within the system. Type B thermocouples were chosen since they do not require any temperature compensation at the cold junction and copper wire can be used for instrument lead-in wires. In conjunction with the B-type thermocouples, a Leeds & Northrup Optical Pyrometer will also be used to monitor temperature as an adjunct to the thermocouples. The charge which will be crystallized is semiconductor grade polycrystalline silicon and boron dopant will be added at 1.6×10^{16} atoms/cm³.

After the solidified brick has cooled to room temperature, it is removed from the UCP system. A qualitative description of the physical appearance of the brick will be made noting if any imperfections, such as cracking, have been introduced into the brick during manufacture. The brick will also be weighed in order to quantitatively measure the extent to which any physical defects have resulted in unuseable material. After this cursory physical inspection and material sizing, this brick is sliced into 10 cm x 10 cm sheets with a thickness of 300-400 microns. After the brick has been sliced, the semicrystalline wafers are removed from the saw and cleaned to remove oil and particles from them. The wafers are then inspected by Semix's Quality Control for dimensional imperfections, such as thickness, squareness, and taper and also for bulk resistivity.

The data collected by QC will be tabulated for each brick to be correlated against more detailed electrical data obtained from the solar cell characterization. In this way QC techniques will be assessed with respect to their reliability and accuracy. These considerations will be discussed in greater detail in the Auxiliary Systems section of this report.

The solar cell processing will involve an initial etch to remove surface saw damage from the wafers. The wafers will then be diffused to form an N-P junction yielding a high sheet resistance. The front patterns will be evaporated onto the surface after photolithography followed by Ag electroplating on the reverse side of the wafer. A Ta_2O_5 AR coating will also be evaporated on the front side of the wafer.

A solar simulator calibrated with a flight tested NASA-Lewis cell will be employed in evaluating the processed solar cells. The electrical tests will include the following:

- Short-Circuit Current (I_{sc})
- Open-Circuit Voltage (V_{oc})
- Conversion Efficiency
- Fill Factor (FF)
- Peak Power Current (I_{pp})
- Peak Power Voltage (V_{pp})
- Red Short-Circuit Current (I_R)
- Blue Short-Circuit Current (I_B)
- Junction Capacitance
- Conductance
- Bulk Resistivity
- Shunt Resistance

This data will then be tabulated for each run from which the initial wafers originated. Various correlations will be made to relate the above measurements to the run parameters. These correlations will be used to eventually establish a performance baseline to measure the performance of prototype UCP systems.

The work done during this quarter has focused primarily on data collection. The next quarter will discuss the characterization and data analysis of wafers now being processed into solar cells. Furthermore, a similar analysis to that outlined in this report will be made in following quarters on prototype systems to determine their technical and economical performance.

SECTION III

HIGH TEMPERATURE SYSTEMS DEVELOPMENT

Starting in the early 1970's, research at Solarex and later at Semix led to an acceptable low cost method of fabricating silicon sheet, the Ubiquitous Crystallization Process (UCP). The UCP offers many economic and technological advantages over competing silicon sheet approaches including the ability to manufacture rectangular sheet, low energy consumption, low direct materials costs, high mechanical strength, and demonstrated AM1 electrical efficiencies as high as 17%⁴ for 2 x 2 cm cells. Other advantages include the UCP's potential for automated high throughput systems with high process yields. The goals of this task are to exploit the potential of the Ubiquitous Crystallization Process to create high productivity, low-cost systems that will meet the DOE projections.

The first step on the road to automation was taken with the development of the Prototype 1 System (P1). P1 was designed to crystallize bricks greater than 17 kg, using automatic temperature controls and recording equipment. Figure 3.1 shows a size comparison of the P1 bricks and the current Semix production bricks. P1 was completed during the first part of this quarter and by July, 1980 was in operation. During the remainder of this quarter, experimental runs in the P1 system were carried out.

Gains of P1 over the preceding systems which have already become apparent include:

- o Higher throughput - over four times as much silicon is crystallized in less than twice the time.

Figure 3.1 17 Kg. Prototype 1 Semicrystalline Brick, 4.2 Kg. Semicrystalline Brick, 10 x 10cm. Wafer and Solar Cells

- o Lower energy consumption - P1 invests less than 20% of the KWh/kg of silicon that existing technology requires.
- o Lower labor costs - with the controls and increased size, 8 - 12 times as much silicon can be crystallized for the same labor input as before.
- o Higher process yield and better utilization of direct materials.

In order to optimize the P1 and set the stage for the next generation, higher productivity system, experimentation was designed to:

- o Optimize the thermal parameters to increase throughput, lower power usage, and maintain material quality.
- o Measure system reliability.
- o Determine and improve materials yield and process yield.
- o Determine and improve materials utilization.

To this end seventeen runs were made this quarter. Table 3.1 lists the experimental runs and their yields, and Figure 3.2 shows a current UCP yield distribution for the Prototype 1 System. It can be seen that of the seventeen runs, fourteen had yields of 95% or better, one had a 50% yield, and two had a 0% yield. Brick #P1-3 had a 50% yield due to a crack in the crucible, whereby, part of the molten silicon seeped out. Nevertheless, the molten silicon remaining in the crucible was usable. The two runs

TABLE 3.1
PROTOTYPE 1 YIELD AND ENERGY CONSUMPTION

	UCP YIELD*	MELTING (kWh/kg)	CRYSTALLIFICATION (kWh/kg)
1	98.1%	9.82	2.22
2	94.4%	12.4	1.78
3	52.7%	8.8	2.42
4	99.3%	12.9	3.8
5	-----POWER FAILURE-----		
6	97.9%	19.8	3.05
7	97.9%	23.3	3.17
8	98.7%	12.65	3.42
9	99.3%	12.65	3.97
10**	97.8%	---	---
11**	Not Weighed	---	---
12	97.9%	18.6	5.67
13	96.8%	9.2	4.29
14**	96.7%	---	---
15	98.4%	10.4	5.52
16	Not Weighed	6.45	3.28
17	99.1%	19.8	5.52

COMPARATIVE AVERAGE ENERGY CONSUMPTIONS

	MELT (kWh/kg)	CRYSTALLIZATION (kWh/kg)
Existing Technology Average	13.4	21.0
Prototype 1 Average	13.6	3.7

* UCP Yield = Brick Weight/Charge Weight X 100%

** Data was not obtained due to faulty instruments.

Figure 3.2
First Quarter Histogram
of Percent Runs Versus UCP Yield

having 0% yield were results of power supply failures causing the run to abort.

Also shown in Table 3.1 are measurements of kilowatt hours per kilogram of charged silicon for the 17 experimental runs and a comparison of P1 energy consumption with energy usage in the existing technology. These results show that there is a dramatic decrease in energy consumption during the crystallization stage for P1 over the existing technology.

Part of the reduction in energy usage was accomplished by modifying the insulation package which resulted in less heat loss from the system. However, the increase in energy usage during crystallization over the course of the 17 experimental runs indicates that the insulating materials being used are subject to some decay over time causing greater heat loss from the system. These observations elicit further investigation of insulating materials which may improve the thermal environment of the system even more.

Thermal environment parameters and other Prototype 1 experimental conditions are correlated to brick quality and to cell performance within the Performance Analysis task of Phase I. In addition, it is anticipated that a Prototype 2 UCP system will be put into operation during the following quarter and similar evaluations of material quality will be conducted.

Initial P1 results are encouraging and appear to indicate that the system is capable of producing semicrystalline bricks with consistently high yield. This will be verified through further reliability experimentation during the upcoming months.

SECTION IV

WAFERING AND MECHANICAL SYSTEMS DEVELOPMENT

INTRODUCTION

The Wafering and Mechanical Systems Development task of the program includes all areas of mechanical design needed to develop an advanced manufacturing line for the production of sheet silicon. Two processes which are of major importance are sizing the crystallized brick to a 10 cm x 10 cm cross section, and slicing the sized brick into wafers. During this quarter, we began investigating the machinery and techniques used in these two areas. In wafering, an experimental investigation of multi-blade slurry (MBS) sawing began. In sizing, a machine was developed to improve sizing throughput and dimensional accuracy.

MBS Experimental Slicing

We began an experimental investigation of silicon slicing on a standard MBS saw in order to increase the material yield and output of that machine. Such an investigation was part of the work done by Varian Associates under JPL Contract No. 954374.⁷ At the end of Phase I in the Varian Report, a "baseline or standard silicon cutting technique" that uses 0.15 mm (0.006 in.) thick by 6.35 mm (0.25 in.) high blades, with 0.35 mm (0.014 in.) thick spacers is described (Varian, p. 113). This is based on a single run using 300 blades, a 117 mm load length with a 10 cm round ingot, resulting in 83% yield and a 32 hour run time. We began our investigation to see if we could work down to such a spacing while cutting a full 190 mm length load of 10 cm square material, with consistently repeatable and higher yields.

A total of twenty-nine (29) experimental runs were made during the first quarter. The machine used was a standard slurry saw with blade packs 19 cm (7.5 inches) wide being used exclusively.

Wafer size was 10 cm x 10 cm and 10 x 15 cm. The slurry used was a mixture of P.C. oil and Silicon Carbide grit.

Variations in wafering parameters such as blade spacing, grit size, feed pressure, etc, were carried out during the first quarter as shown with results in Table 4.1. Runs number 1 through 20 were made on an MBS saw from Manufacturer "A" while numbers 2.1 to 2.7 were made on an MBS saw from Manufacturer "B"*. The numbers appearing under the blade pack heading represent the blade thickness, spacer thickness, blade height and number of blades respectively. Feed pressure is the force with which the workpiece is held against the cutting surface. The first number under the slurry heading is the grit size number; the second is the concentration of grit to P.C. oil in kilograms per liter. Yield is the percentage of wafers that came off the saw with no breakage or chipping. Actual material yield includes this breakage while theoretical material yield is the potential square area with no breakage. Blade travel represents the total sliding distance covered by the blades during the run and output is the area in m^2 of good wafers divided by run time. While the output represented by m^2/hr does not reflect machine downtime, it can be used for comparison of different techniques on the same machine.

By the end of September, 0.48 mm (0.019 in.) spacers and 0.20 mm (0.008 in.) with a #400 grit were being used in production on a full time basis. We are now cutting wafers in manufacturing that are on the average 76 microns (0.003 in.) thinner than those produced with the 0.56 mm (0.022 in.) spacers. This represents an 11 percent increase in material yield. Output per machine has increased accordingly because yield after breakage did not decrease and run time per load did not increase.

*We have chosen not to disclose the names of our saw manufacturers for proprietary reasons and so as not to present a manufacturer in a favorable or unfavorable light.

TABLE 4.1

VARIATIONS IN WAFERING PARAMETERS

RUN NO.	OBJECTIVE	BLADE PACK, mm	FEED PRESSURE, gm/BLADE	SLURRY, GRIT #-kg:liter	YIELD, %	MATERIAL YIELD, ACTUAL/THEOR., M ² /kg	BLADE TRAVEL, 10 ⁴ METERS	OUTPUT, M ² /hr	COMMENTS
1	Establish standard run data	.20-.56 - 6.35-250	170	400-.60	94	.53/.56	3.4	.16	Average of two runs
4	Attempt 2nd use of 7.94 mm high blades	.20-.56- 7.94-250	170	400-.60	<30	-./.56	-	-	Approximately 100 blades broke. Blades worn to 1.65 mm minimum height.
5	Use .51 mm spacers	.20-.51- 6.35-267	160	500-.60	90	.54/.60	4.5	.11	
8	Improve output with 500 grit by using higher concentration	.20-.51- 6.35-267	160	500-.75	100	.60/.60	3.5	.17	Excellent results
9	Use .46 mm spacers	.20-.46- 6.35-288	120	600-.60	20	.13/.65	4.8	.024	Extensive wafer breakage
11	Use #400 grit with .51 mm spacers	.20-.51- 6.35-267	160	400-.60	97	.58/.60	2.9	.20	
12	Improve output with higher feed pressure	.20-.51- 6.35-267	180	400-.60	95	.57/.60	2.8	.22	
16	Test "bright" steel blades	.20-.56- 6.35-250	170	400-.60	96	.54/.56	3.0	.20	

TABLE 4.1 (Continued)

VARIATIONS IN WAFERING PARAMETERS

RUN NO.	OBJECTIVE	BLADE PACK, mm	FEED PRESSURE, gm/BLADE	SLURRY, GRIT #-kg:liter	YIELD, %	MATERIAL YIELD, ACTUAL/THEOR., M ² /kg	BLADE TRAVEL, 10 ⁴ METERS	OUTPUT, M ² /hr	COMMENTS
19	Improve output with 600 grit by using higher concentration and higher pressure	.20-.51 6.35-267	160	600-.72	93	.56/.60	3.9	.13	Better yield and output than Run 9.
*	Use .46 mm spacers	.20-.46- 6.35-288	160	600-.48	76	.49/.65	-	.089	
2.1	Test new saw	.20-.51- 6.35-267	160	400-.60	95	.57/.60	2.8	.20	
2.3	Use .48 mm spacers with #400 grit	.20-.48- 6.35-277	160	400-.72	96	.60/.62	2.9	.22	Highest actual material yield to date. Equals highest output of Run 12.
2.6	Slice 10 cm x 15 cm wafers	.20-.51- 6.35-267	>170	400-.60	90	.54/.60	3.0	.24	Partial load only.
2.7	Use .46 mm spacers with #500 grit	.20-.46- 6.35-288	140	500-.72	99	.64/.65	4.9	.14	Highest yields yet.

Blade Pack : blade thickness - spacer thickness - blade height - number of blades in 7.5 inch width

Feed Pressure : force on each blade

Slurry : grit size number - concentration of grit to oil

Yield : percentage of wafers remaining after breakage and chipping during wafering

Material Yield: actual material yield/theoretical material yield if no breakage occurred

Blade Travel : total travel of blades through the work during the run

Output : actual square meters sliced divided by the run time

In run 2.6 we cut 10 cm x 15 cm wafers for the first time (Figure 4.1). Slicing 150 m² wafers in this configuration could result in a 50% increase in output per machine. Wafering costs would decrease about 33% (blade pack and run time remain unchanged, slurry cost would increase 50%). Work will be carried out under this program to determine optimal wafer configuration as it relates to cell processing and wafering economies.

In run 2.7, using 0.46 mm spacers, we cut with high yield results for the first time. This run also gave the highest material yield to date.

In the next quarter we will continue to work on reducing the spacer thickness used in slicing both 10 cm x 10 cm and 10 cm x 15 cm wafers. We also plan to begin evaluating the use of 0.15 mm thick blades in order to reduce kerf losses.

SIZING

A dicing machine was fitted with two 16 inch diamond wheels spaced 100 mm between edges. The ingot, mounted in a specially designed carriage using a mechanical clamping device, is fastened at two ends, as shown in Figure 4.2, and fed hydraulically through the blades. This results in two parallel faces being sliced exactly 10 cm apart. At the end of the cut the ingot is turned by hand 90 degrees and the other two parallel sides are sliced.

The machine consistently produces bricks in which the corners are $90^{\circ} \pm 1^{\circ}$. This means that there is no more than 2 mm taper along any one edge.

The most critical aspect of this operation is the flow of coolant over the blades. If for any reason coolant is prevented from reaching either or both sides of a blade the resulting heat buildup will cause the blade to warp rendering the ingot useless.

Figure 4.1 10cm, x 15cm, Wafer

Figure 4.2 Dual-Bladed Sizing Saw

In the next quarter work will begin on a sizing saw fitted with a 20 inch blade. The saw will be capable of sizing the next generation of 17.5 kg bricks.

SECTION V

AUXILIARY SYSTEMS DEVELOPMENT

QUALITY CONTROL AND MEASUREMENT

It has been found that both four-point probe and eddy current measurements, standard resistivity techniques for single-crystal dopant level measurement, create spurious readings for semi-crystalline material.

In single-crystal silicon the majority carrier scattering and drift transport mechanisms have been well known for decades. However, although a resistivity measurement is an excellently behaved analog of dopant concentration in single-crystal silicon, this is not the case in semicrystalline silicon. The difficulty introduced likely lies in majority carrier conduction mechanisms across grain boundaries, which are not operative in the single-crystal case.

It should be pointed out here that resistivity measurement for evaluating dopant concentration in silicon has mainly been a convenience born of the lack of a non-destructive test technique. For the photovoltaic field the value of substrate resistivity, per se, is not really of interest. Rather, the dopant concentration and consequent Fermi level position are of much greater interest in the case of a solar cell's sheet material. Especially in the case of semicrystalline silicon, as generated by Semix, the mechanisms of grain-boundary transport of majority carriers are of

little import in solar cell operation. In the cell the photocurrent flows normal to the plane of the silicon sheet and the grains continue through the sheet. Consequently, the majority carrier lateral transport mechanisms have little bearing on the final solar cell properties, and only cloud attempts to non-destructively evaluate majority carrier concentrations in the silicon by resistivity measurements.

In light of this we are beginning a program to develop techniques by which we can sample semicrystalline material effectively in order to insure consistent high quality wafers to solar cell producers.

CONCLUSION

The first quarterly period of the DOE/Semix Cooperative Agreement has ended successfully and the program has begun at a fast pace. While the concepts for equipment development are firmly in hand, a great deal of design, fabrication and experimentation of the systems are yet needed to meet the DOE Commercial and Technology Readiness goals. This quarter we organized the team, designed the experimental plans, fabricated key pieces of initial equipment, and started experimentation, and we understand the necessity of maintaining our auspicious start in order to accomplish the program objectives.

Key accomplishments during the first quarter centered around the fabrication and initiation of experimentation for the Prototype 1 crystallization system. Results showed that increased brick size, higher throughput, decreased power consumption, decreased labor and high yield were all possible. This is highly encouraging.

Experimentation in multi-blade slurry wafering showed that large 150 cm² wafers were possible at high yields with no increase in cost. In addition, high throughputs and yields were demonstrated for 10 x 10 cm wafers. Work will continue on optimizing the MBS systems.

During the next quarter it is anticipated that we will continue to experiment with the Prototype 1 Crystallization system while at the same time incorporating innovative ideas into a Prototype 2 system. As mentioned above we will continue to work with the multi-blade slurry saw wafering technology to continue to

improve throughput and yields, while at the same time, experimenting with alternate wafering technologies, most notably ID sawing. Working in conjunction with the tasks dedicated to understanding the technical and economic aspects of the material and technology, all areas of the process from the High Temperature Systems through Quality Control will continue to be better understood and confidence in our projections of a possible 42.1 cents (\$1978)/Wp will grow.

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