35
8/79

lh. 2357

DOE/JPL/954605-4

DEVELOPMENT OF LOW-COST, HIGH ENERGY-PER-UNIT-AREA SOLAR
CELL MODULES

Quarterly Report No. 4, October 1—December 31, 1977

By
Gregory T. Jones
Sanjeev Chitre

December 1977

Work Performed Under Contract No. NAS-7-100-954605

950 4579

Sensor Technology, Incorporated
Chatsworth, California

U.S. Department of Energy

MASTER

Solar Energy

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Department of Energy, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

This report has been reproduced directly from the best available copy.

Available from the National Technical Information Service, U. S. Department of Commerce, Springfield, Virginia 22161.

Price: Paper Copy \$4.50
Microfiche \$3.00

DEVELOPMENT OF LOW-COST, HIGH ENERGY-PER-UNIT-AREA
SOLAR CELL MODULESⓄ

Quarterly Report No. 4

Gregory T. Jones

Sanjeev Chitre

December 1977

JPL CONTRACT NO. 954605

Sensor Technology, Incorporated
21012 Lassen Street
Chatsworth, California 91311

This work was performed for the Jet Propulsion Laboratory California Institute of Technology, under NASA Contract NAS7-100 for the U.S. Department of Energy (DOE).

The JPL Low-Cost Silicon Solar Array Project is funded by DOE and forms part of the DOE Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays.

ABSTRACT

Production techniques and process procedures were the primary tasks emphasized during this quarter from October 1, 1977 through December 31, 1977 for the development of low-cost, high energy-per-unit area solar cell modules. Two surface macrostructure processes were written in detail, production techniques analyzed, and technical results reported. The surface macrostructure process, that produced the best solar cell electrical performance, utilized a sequential etching process procedure suitable for large scale, low-cost, production. A silicon solar cell laserscribing technique was reported in detail. While the laserscribe can cut through a p-n junction without damaging the junction, it was shown that the laser-scribing technique was important. Included in the discussion is wafer alignment, laserscribing methodology and wafer breaking technique. Electrical performance analysis was made for hexagonal solar cells processed with four grid pattern designs. It was experimentally shown that the electrical performance of solar cells with the same grid line coverage was relatively insensitive to grid pattern design. A process procedure for automatically spinning an anti-reflective coating onto a solar cell was analyzed in detail. An optimized technique suitable for production was achieved. A SAMICS analysis for all hexagonal solar cell process steps and module assembly progressed significantly this quarter. Upon completion a detailed process cost analysis will be reported.

TABLE OF CONTENTS

	<u>Page</u>
ABSTRACT	i
TABLE OF CONTENTS	ii
LIST OF FIGURES	iii
LIST OF TABLES	v
INTRODUCTION	1
TECHNICAL DISCUSSION	3
A. Surface Macrostructure Process	3
1. Preliminary Studies	
2. Surface Macrostructure Process #1	
3. Surface Macrostructure Process #2	
4. Technical Discussion and Results	
B. Silicon Wafer Laserscribing	16
C. Hexagonal Solar Cell Grid Patterns	21
D. Spin-on Anti-reflective Coating Study.	25
E. SAMICS	29
CONCLUSIONS	32
RECOMMENDATIONS	32
NEW TECHNOLOGY	34
PROGRESS SUMMARY AND PROGRAM PLAN	35
LIST OF REFERENCES	37

LIST OF FIGURES

<u>Figure</u>	<u>Page</u>
1. Surface macrostructure SEM photograph at 4000x magnification for a silicon wafer processed in a 10% NaOH by weight to deionized water solution	10
2. Surface macrostructure SEM photograph at 2000x magnification for a silicon wafer processed in a 10% NaOH by weight to deionized water followed by a water rinse and then a 1% NaOH by weight to water solution . .	11
3. Surface macrostructure SEM photograph at 20,000x magnification for a silicon wafer processed in a 10% NaOH by weight to deionized water followed by a water rinse and then a 1% NaOH by weight to water solution	17
4a. SEM photograph of laserscribed silicon material at 410x magnification	19
4b. SEM photograph of laserscribed silicon material at 1650x magnification	19
5. "Sensagon" six grid hexagonal solar cell	22
6. "Sensagon" ten grid hexagonal solar cell	22
7. "Sensagon" parallel track hexagonal solar cell	22
8. "Sensagon" pine tree hexagonal solar cell	22
9. Electrical performance curves of a "Sensagon" 6 grid hexagonal solar cell, 50.8cm ² , with and without SiO anti-reflective coating, under tungsten light at 28°C and at 100 mW/cm ²	23
10. Electrical performance curves of a "Sensagon" 10 grid hexagonal solar cell, 50.8cm ² , with and without SiO anti-reflective coating, under tungsten light at 28°C and at 100 mW/cm ²	23

FigurePage

11. Electrical performance curves of a "Sensagon" parallel track hexagonal solar cell, 50.8cm^2 , with and without SiO anti-reflective coating under tungsten light at 28°C and at 100 mW/cm^2 23
12. Electrical performance curves of a "Sensagon" pine tree hexagonal solar cell, 50.8cm^2 , with and without SiO anti-reflective coating under tungsten light at 28°C and at 100 mW/cm^2 23
13. Titaniumsilicafilm A ($\text{TiO}_2 + \text{SiO}_2$) anti-reflective coating for three groups of solar cells. The first group is surface etched with no encapsulant. The second group is texturized and encapsulated with RTV-615. The third group is texturized with no encapsulant. The solar cells are hexagonal with 50.8cm^2 active area. They are tested at 28°C , 100 mW/cm^2 under tungsten light. 30
14. Development of Low-Cost, High Energy-Per-Unit-Area Solar Cell Modules; Phase I and Phase II Program Plan 36

LIST OF TABLES

<u>Table</u>		<u>Page</u>
1.	Summary of surface macrosturcture experiments and results for the sequential etching process consisting of 10% NaOH by weight to water followed by a deionized water rinse and than a 1% NaOH by weight to water solution	13
2.	Comparison of four hexagonal solar cell grid patterns. The solar cells have the same surface area, 50.8cm^2 , were processed from the same batch of wafers, and were ₂ tested under the same conditions, 100 mW/cm^2 tungsten light at 28°C	24

INTRODUCTION

Hexagonal solar cells in a densely packed array are being utilized in the development of low-cost, high energy-per-unit-area solar cell modules. This program is being performed in two phases. The primary objectives for Phase I include hexagonal solar cell laserscribing and high density solar cell module fabrication. This work was completed last quarter with the delivery of three hexagonal solar cell modules to the Jet Propulsion Laboratory. The primary objectives for Phase II include hexagonal solar cell processing techniques to obtain high photovoltaic energy conversion efficiency and high solar cell module power output. Work toward the completion of these objectives progressed during this quarter. Investigations were completed on the surface macrostructure process procedure, silicon wafer laserscribing, and hexagonal solar cell grid patterns. Work continued on the spin-on anti-reflective coating methods and on the technical and economic cost analysis (SAMICS) of the process sequence.

During the last quarter evaluation will be made of spin-on and high pressure wafer cleaning methods and an analysis will be completed on the technical and economic cost factors involved in the hexagonal solar cell process sequence. Three hexagonal solar cell modules

will be fabricated and delivered to the Jet Propulsion
Laboratory. A final report will be published.

TECHNICAL DISCUSSION

A. Surface Macrostructure Process

Two surface macrostructure processes suitable for large scale production of silicon solar cells have been developed. Silicon wafer surface preparation and etching time, temperature, and concentration was optimized relative to surface macrostructures that trap light efficiently. The process procedure was defined for manual large scale production. The process equipment is capable of texturizing 200 ninety millimeter diameter silicon wafers in five minutes or 2400 silicon wafers in one hour. The silicon wafers have black antireflective surfaces which are uniformly etched and are batch to batch reproducible.

A significant innovation to silicon solar cell technology has been the use of orientation dependent etches to reduce reflection from the front surface of the solar cell. Various compounds like sodium hydroxide, hydrazine, ethylene diamine, and potassium hydroxide have been successfully used for anisotropic etches (Ref. 1, 2, 3, 4). Sodium hydroxide was chosen for this process. This was based on cost, safety, and ability to be used in high volume production.

1. Preliminary Studies

Experimentation was performed on 2.15 inch diameter and 90 mm diameter silicon wafers utilizing the surface macrostructure process. A 30% NaOH/water solution at 80°C was used to etch the surface of the silicon wafers. A nitrogen bubbler was used to agitate the solution. The texturized surface was black after two minutes in the solution. However, uniformity across the silicon wafer surface was difficult to achieve and reproducibility from batch to batch was hard to obtain. Similar experiments produced the same results with 10% NaOH/water solution at 80°C for 25 minutes. The nitrogen bubbler was used to agitate the solution. While uniformity across the silicon wafer surface was improved, reproducibility from batch to batch was still hard to obtain. Further experimentation was performed with a 1% NaOH/boiling water solution at 100°C for 25 minutes. The nitrogen bubbler was not utilized. Results were very good for these experiments. The solution produced black uniform wafer surfaces, and batch to batch reproducibility was good. Experimental analysis led to the following observations:

- (a) Clean silicon wafers, which are free of all organic contaminants, are required to etch uniform surface macrostructures.

- (b) The wafer jig configuration was important; it effects the flow rate and thus effects the surface uniformity and batch reproducibility.
- (c) High concentration of NaOH/water solution etches very fast. However, batch to batch reproducibility is hard to obtain.
- (d) Nitrogen agitation at a high flow rate greatly effects surface uniformity and batch to batch reproducibility.

The results of the preliminary experimentation led to two basic surface macrostructure etching solutions to be used in sample volume testing for production. The first solution consisted of 10% NaOH by weight to water. The second solution consisted of 1 % NaOH by weight to water.

Two surface macrostructure process procedures were developed. Both process procedures consisted of five steps. They are (1) wafer surface cleaning, (2) surface macrostructure etching, (3) four stage cascade rinse, (4) surface macrostructure final cleaning, and (5) final rinse/spin dry. Surface macrostructure process number one utilized, in step (2), 10% NaOH by weight to water. Surface macrostructure process number two utilized, in step (2), a sequential operation with three separate solutions, 10% NaOH by weight to water followed by a hot D.I. water rinse and then 1% NaOH by weight to water. The two surface macrostructure process procedures are discussed in detail below.

2. Surface Macrostructure Process Number One

Ninety millimeter diameter, Czochralski (100), as cut, flash etched, 20 mil thick, round silicon wafers were procured and sample inspected for experimentation. They were manually placed into jigs which hold twenty-five wafers. Four jigs or one hundred silicon wafers were processed together.

The first step in the wafer surface macrostructure process consists of a two stage wafer surface cleaning procedure. The silicon wafers are placed into a hot trichlorethylene for five minutes (preferably in an ultrasonic tank) followed by a 5 minute methanol dip. This process step cleans any organic contaminants off the wafer surfaces which might otherwise impede the surface macrostructure etching step.

The second step in the surface macrostructure process is surface macrostructure etching. The four jigs containing the silicon wafers are introduced into an ultrasonic stainless steel tank which has been filled with a 10% solution by weight of NaOH to deionized water at $85^{\circ}\text{C} \pm 2^{\circ}\text{C}$. Suspended in the tank is a nitrogen bubbler system which is designed to agitate the solution in addition to the ultrasonics. Approximately 10 liters per minute of nitrogen gas is required for the bubbler designed by Sensor Technology, Inc. It is to be noted that the design and the placement

of the bubbler with respect to the silicon wafers determines the consistency of the surface macrostructure etching process. A large amount of nitrogen bubbles which are small in diameter contribute to uniform surface macrostructures. The process time is approximately five minutes which will vary according to the amount of silicon particles and contaminants in the NaOH solution.

The jigs are manually removed from the surface macrostructure etching tank and placed into the first ultrasonic stage of a four stage cascade rinse system which make up the third step in the process. The jigs remain for five minutes in each of the four stages. Hot deionized water flows at a rate of 3.8 liters per minute from the fourth stage where the D.I. water input temperature is $80^{\circ}\text{C} \pm 5^{\circ}\text{C}$ to the first ultrasonic stage where the D.I. water output temperature is $72^{\circ}\text{C} \pm 5^{\circ}\text{C}$. The silicon wafers get progressively cleaner as they move from the first stage to the fourth stage of the cascade rinse system.

The fourth step in the surface macrostructure process is final cleaning. The wafer jigs are manually removed from the cascade rinse and introduced into a sulphuric acid/hydrogen peroxide mixture at $70^{\circ}\text{C} \pm 5^{\circ}\text{C}$ for five minutes. This solution removes any remaining deposits of sodium hydroxide that may be trapped in the wafer surface macrostructure. The wafers are rinsed off in running D.I.

water for five minutes and are now ready for the final step in this process sequence.

The fifth step in the surface macrostructure process is the final rinse/spin dry. The last remaining water surface contaminants in this five minute cycle are removed. The wafers are now ready for the junction formation process.

The surface macrostructure process demonstration equipment was used to process 100 ninety millimeter diameter silicon wafers for each carrier basket or four cassettes carrying 25 wafers each. The system capability is 200 wafers per process step assuming two layers of 100 wafers each. Therefore, the wafer surface preparation process can manually process up to 2400 wafers in one hour.

3. Surface Macrostructure Process Number Two

Ninety millimeter diameter, Czochralski (100), as cut, flash etched, 20 mil thick round silicon wafers were procured and sample inspected for experimentation. They were manually placed into jigs which hold twenty-five wafers. Four jigs or one hundred silicon wafers were processed together.

The first, third, fourth and fifth steps in the process are identical to the surface macrostructure process number one. Process step (2), surface macrostructure etching has been modified as follows: Four jigs carrying the silicon wafers are introduced into an ultrasonic stainless steel

tank which has been filled with a 10% solution by weight of NaOH to deionized water at $80^{\circ}\text{C} \pm 2^{\circ}\text{C}$. Suspended in the tank is a nitrogen bubbler system which is designed to agitate the solution in addition to the ultrasonics. Approximately 10 liters per minute of nitrogen gas is required for the bubbler designed for this step by Sensor Technology, Inc. The process time is approximately five minutes which will vary according to the amount of silicon particles and contaminants in the NaOH solution. The jigs are manually removed from the etching tank and placed into a hot D.I. water rinse tank. The jigs are then removed and placed into a second ultrasonic stainless steel tank which has been filled with a 1% solution by weight of NaOH to deionized water at $100^{\circ}\text{C} \pm 2^{\circ}\text{C}$. Suspended in the tank is a nitrogen bubbler. Approximately 10 liters per minute of nitrogen gas is required. The process time is approximately five minutes which will vary according to the amount of silicon particles and contaminants in the NaOH solution.

4. Technical Discussion and Results

A comparison was made between the two surface macrostructure processes. Figures 1 and 2 shows two SEM photographs of the surface macrostructures produced by the 10% NaOH by weight to water solution and also the same solution followed by a D.I. water rinse and then 1% NaOH by weight to water solution. Figure 1 is under 4000X and

Figure 1. Surface macrostructure SEM photograph at 4000 X magnification for a silicon wafer processed in a 10% NaOH by weight to deionized water etching solution.

Figure 2. Surface macrostructure SEM photograph at 2000 X magnification for a silicon wafer processed in a 10% NaOH by weight to deionized water followed by a water rinse and then a 1% NaOH by weight to water solution.

Figure 2 is under 2000X magnification. A comparison of the two photographs clearly shows that the surface macrostructure process number two consisting of the sequential etching solutions produces pyramidal structures that are more sharply defined than the first process. There is far less rounding of the pyramid peaks utilizing a sequential 10% NaOH to water etch followed by a water rinse and 1% NaOH to water etching solution than through a one step process that utilizes only a 10% NaOH to water solution. The surface macrostructure process number two produces consistent and uniform texturized surfaces and the process is batch to batch reproducible.

A more in-depth study was made on the surface macrostructure process number two procedure. Various parameters like temperature of the 10% NaOH by weight to water solution, nitrogen agitation, and ultrasonic agitation were varied. The wafers thus processed were measured for short circuit current, I_{sc} , open circuit voltage, V_{oc} , and efficiency, η . A summary of the experiments performed and their results is shown in Table 1.

Comparing batch Sentex -011 and 012 one can conclude that ultrasonics is needed for silicon wafer definition and uniformity. This result is probably due to an increased etching rate since the ultrasonic agitation helps to remove the hydrogen bubbles which would otherwise cling to the surface and inhibit further etching.

Table 1. Summary of surface macrostructure experiments and results for the sequential etching process consisting of 10% NaOH by weight to water followed by a deionized water rinse and then a 1% NaOH by weight to water solution.

Batch No.	No. of Wafers	Starting Material Thickness	Temp. (°C)	10% NaOH Bath Nitrogen (l/min)	Conditions Ultra-sonic	Thickness (mil)	Temp. (°C)	1% NaOH Bath Nitrogen (l/min)	Ultra-sonic	Thickness (mil)
Sentex 011	15	20.0 mil	80	0	Off 40KHZ	1.2	100	--	Off	0.3
Sentex-012	25	20.0 mil	80	0	On 40KHZ	1.5	100	--	Off	0.3
Sentex-013	25	20.0 mil	80	7	On 40KHZ	1.4	100	--	Off	0.5
Sentex 014	25	20.0 mil	80	7	On 40KHZ	1.5	100	--	On	0.55
Sentex-015	25	20.0 mil	80	10	On 40KHZ	1.4	100	--	On	0.55
Sentex-016	25	20.0 mil	80	10	On 40KHZ	1.4	100	7	On	0.4
Sentex-017	25	20.0 mil	70	10	On 40KHZ	1.1	100	--	On	0.55
Sentex-018	25	20.0 mil	60	10	On 40KHZ	0.8	100	--	On	0.55
Sentex-019	25	20.0 mil	80	10	On 40KHZ	1.4	100	--	On	0.55
Sentex-027	25	20.0 mil	80	10	On 40KHZ	1.4	100	--	On	0.55
Sentex-029	25	20.0 mil	80	10	On 40KHZ	1.4	100	--	On	0.55
Sentex-032	25	17.4 mil	80	10	On 40KHZ	1.25	100	--	On	0.55

TABLE 1. continued

No.	Batch No.	No. of Wafers	Starting Material Thickness	Total Etched Thickness	$\overline{I_{sc}}$ (Amp)	$\overline{V_{oc}}$ (Volts)	$\overline{\eta}$ (%)	η Peak (%)
1.	Sentex-011	15	20.0 mil	1.5 mil	1.455	0.580	11.12	12.21
2.	Sentex-012	25	20.0 mil	1.8 mil	1.501	0.580	11.5	12.45
3.	Sentex-013	25	20.0 mil	1.7 mil	1.457	0.577	11.41	12.52
4.	Sentex-014	25	20.0 mil	2.05 mil	1.432	0.585	11.20	12.3
5.	Sentex-015	25	20.0 mil	1.95 mil	1.630	0.575	12.75	13.75
6.	Sentex 016	25	20.0 mil	1.8 mil	1.51	0.580	11.65	12.90
7.	Sentex-017	25	20.0 mil	1.65 mil	1.414	0.580	11.06	12.40
8.	Sentex-018	25	20.0 mil	1.35 mil	1.381	0.580	10.8	12.0
9.	Sentex-019	25	20.0 mil	1.95 mil	1.104	0.580	12.55	13.3
10.	Sentex-027	25	20.0 mil	1.95 mil	1.560	0.580	12.2	13.4
11.	Sentex-029	25	20.0 mil	1.95 mil	1.687	0.580	13.2	13.55
12.	Sentex-032	25	17.4 mil	1.8 mil	1.612	0.580	12.61	13.31

The addition of nitrogen agitation, was incorporated into the process to help remove the hydrogen bubbles. The agitation flow pattern was found to be very important for silicon wafer etching uniformity. Sentex -012 in Table 1 shows the results without the use of nitrogen agitation. Sentex 013 shows the results with the use of nitrogen agitation. Increasing the nitrogen flow rate from 7 to 10 liters per minute increases the uniformity as shown by Sentex -015.

Sentex -016 indicates that the introduction of nitrogen agitation into the 1% NaOH to water solution allows one to remove the steric hindrance of sodium silicate, thus improving the pyramid definition on the silicon surface. Also, the ultrasonic agitation was retained in this process batch which helped to reduce the hydrogen bubbles and enhance the etching process.

Temperature variation results are shown in Sentex 015, 017, and 018 at 80°C, 70°C, and 60°C respectively for the 10% NaOH to water solution. Low short circuit current, I_{sc} , is found for batches, 017 and 018 processed at low temperatures which is due to degraded pyramidal structures. The best temperature for the 10% NaOH to water solution is 80°C as shown in Sentex 015. The surface macrostructure obtained with the Sentex 015 sequential process is shown in the SEM photographs in Figure 2 at 2000 times magnification and in

Figure 3 at 20,000 times magnification. The surface appears with slightly rounded peaks but with very good pyramidal definition.

The effect of ultrasonic frequency variation is shown in batches 018 and 019. Low frequencies produce undeveloped texturized regions which are probably due to the clinging of hydrogen bubbles to the surface structure. This problem is reduced at higher ultrasonic frequencies.

Sentex 032 shows the results incurred from producing surface macrostructures on surface etched wafers. Improved energy conversion efficiencies can be obtained with the addition of the surface etching process step.

Experiments which are not part of this program were performed with the results reported in Sentex 027 and 029. Higher efficiencies can be obtained with the addition of intermediate process steps. It is recommended that future work be performed on the surface macrostructure process for producing high light collection and energy conversion efficiencies.

B. Silicon Wafer Laserscribing

Laserscribing is accomplished by moving the silicon wafer through the appropriate pattern, which in this program is a hexagon, under a focused beam of laser light. The high intensity pulses are absorbed by the material rapidly heating

Figure 3. Surface macrostructure SEM photograph at 20,000 X magnification for a silicon wafer processed in a 10% NaOH by weight to deionized water followed by a water rinse and then a 1% NaOH by weight to water solution.

it to the boiling point, generating a kerf by evaporation of material. SEM photographs in Figure 4a and 4b show the effect of laserscribing silicon material. The duration of the pulses is sufficiently short (less than 0.5 nanoseconds) that negligible heat flows from the irradiated region via conduction; as a result, the temperature rise at a distance about one mil from the irradiated spot is only a few degrees and no performance degradation occurs. The depth of the kerf need only be a few mils on typical silicon wafers so that the stress enhancement when bent (Ref. 5) assures breaking along the scribe line.

It was shown in Quarterly Report No. 3 for ERDA/JPL Contract 954605 - 77/3 (Ref. 6) that the laserscribe can cut through the p-n junction without damaging the junction. The technique however, for scribing a silicon wafer is very important.

First, the silicon wafer should be aligned properly. Alignment is done manually in the laserscribe used in this program. The wafers are usually scanned prior to laserscribing to check the alignment for initial experiments. A block or stop can be made which is used to assist the operator in wafer alignment and thus eliminate the necessity of scanning each wafer prior to laserscribing.

Second, the silicon wafer can be cut by laser from the front of the cell, thus cut through the p-n junction or it can be cut by laser from the back of the cell, thus the

Figure 4a. SEM photograph of laserscribed silicon material at 410 X magnification.

Figure 4b. SEM photograph of laserscribed silicon material at 1650 X magnification.

cell is broken or cleaved through the p-n junction (Ref. 5). There is a slightly smaller current leakage produced when the cell is cut from the back and therefore this is the preferred method. It should be noted that there is no etch ring, edge grinding, or edge etching required when the solar cells are cut by the laserscribe.

Third, silicon wafers should be scribed prior to solder coating. Experience has shown that scribing solder coated solar cells by laser produces severely shorted p n junctions. This technique is not recommended. Scribing solder coated solar cells by laser through the back surface and then breaking or cleaving the p-n junction can be performed without major current leaking problems but the operator must be very careful when breaking the cell so that no solder pieces are left which might cross the p-n junction and short out the cell. This technique is not preferred for large scale production.

Fourth, the wafer breaking technique is performed manually. After a hexagon is scribed the six sides are broken by hand. This is done in the following manner. The solar cell is placed between the thumb and fingers of one hand, the scribe line is face up. The thumb and index finger of the second hand closes on the edge of the wafer just outside the midpoint of the scribed line and exerts a downward force on the segments and snaps the wafer.

C. Hexagonal Solar Cell Grid Patterns

Hexagonal solar cells with the four distinct grid patterns shown in Figures 5, 6, 7, and 8 and a comparison was made between their electrical performances, shown in Figures 9, 10, 11, and 12. The solar cells have the same surface area, 50.8cm^2 , were processed from the same batch of silicon wafers, and were tested under the same conditions, 100 mw/cm^2 tungsten light at 28°C . The grid line coverage or cell shadowing loss is the same for all four patterns. All four patterns were processed the same using Sensor Technology's standard commercial process that utilizes electroless nickel plating and no special "high efficiency" process techniques. Three grid patterns were silk screen printed and one grid pattern utilized photolithography. The results are summarized in Table 2 and are discussed below:

- (1) Solar cells processed under the same conditions that have the same grid line coverage are relatively insensitive to the grid line pattern used.
- (2) The photolithographic process was able to produce thin grid lines and produce more grid lines per unit area than the silk screen printing process but only a slight, one-half percent, increase in efficiency was achieved which was also matched by the redundant parallel track pattern that was processed with the silk screen printing method.

Figure 5. "Sensagon" six grid hexagonal solar cell.

Figure 6. "Sensagon" ten grid hexagonal solar cell.

Figure 7. "Sensagon" parallel track hexagonal solar cell.

Figure 8. "Sensagon" pine tree hexagonal solar cell.

Figure 9. Electrical performance curves of a "Sensagon" six grid hexagonal solar cell, 50.8 cm², with and without SiO anti reflective coating under tungsten light at 28°C and at 100 mw/cm².

Figure 10. Electrical performance curves of a "Sensagon" ten grid hexagonal solar cell, 50.8 cm², with and without SiO anti-reflective coating under tungsten light at 28°C and at 100 mw/cm².

Figure 11. Electrical performance curves of a "Sensagon" Parallel Track hexagonal solar cell, 50.8 cm², with and without SiO anti-reflective coating under tungsten light at 28°C and at 100 mw/cm².

Figure 12. Electrical performance curves of a "Sensagon" Pine tree hexagonal solar cell, 50.8 cm², with and without SiO anti-reflective coating under tungsten light at 28°C and at 100 mw/cm².

Table 2. Comparison of four hexagonal solar cell grid patterns. The solar cells have the same surface area, 50.8 cm^2 , were processed from the same batch of wafers, and were tested under the same conditions, 100 mw/cm^2 tungsten light at 28°C .

PATTERN	SURFACE	PROCESS	A. R. COATING	ISC (amp)	VOC (volts)	η (%)	η (%)
Pine Tree	Texturized	Photoresist	---	1.47	.56	10.7	10.9
			SiO	1.57	.56	11.3	11.6
Parallel Track	Texturized	Silkscreen Resist	---	1.38	.56	10.5	10.8
			SiO	1.47	.56	11.2	11.7
10 Grid Hex	Texturized	Silkscreen Resist	---	1.44	.56	10.1	10.8
			SiO	1.50	.56	10.8	11.5
6 Grid Hex	Texturized	Silkscreen Resist	---	1.43	.55	10.0	10.9
			SiO	1.52	.55	10.7	11.4

- (3) A single contact point or a redundant contact point produces very nearly the same electrical performance. While a half percent increase in efficiency was observed in the parallel track pattern over the 6 grid and 10 grid hexagon patterns, it was matched by the pine tree pattern that utilized a single contact point.

The electrical performance analysis of the hexagonal solar cell grid patterns was made to check the sensitivity to the grid pattern designs. An exhaustive study was not made. No large advantage was found for utilizing one pattern over another. Therefore, modules will be fabricated utilizing each of the four grid pattern designs produced.

D. Spin-On Anti-Reflective Coating Study

The primary function of anti-reflective coatings is to increase the photovoltaic energy conversion efficiency of solar cells. There are presently several diverse varieties of anti-reflective coatings in common usage ranging from single to multi-layer. The standard method for depositing single layer A.R. coatings such as silicon monoxides, silicon nitride and titanium oxide to an approximate thickness of 800°A is by means of vacuum desposition. The technological level of the equipment currently available in today's market precludes the method of vacuum deposition from being cost-effective and is thus a significant deterrent towards the attainment of a high volume low-cost throughput. With this drawback in mind,

Sensor Technology has proposed the alternative procedure of spin-on anti-reflective coatings.

The solutions used in this study are titaniumsilica-film A, B and C from Emulsitone Company, Whippany, New Jersey. Titaniumsilicafilm is a spin-on formulation which yields glassy films containing TiO_2 and SiO_2 . The indices of refraction for titaniumsilicafilm A, B and C are respectively 1.80, 1.90 and 1.96.

The Titaniumsilicafilms A, B and C were spun on textured and chemically etched wafers which were subsequently encapsulated with RTV encapsulants. Studies of spin speed vs. thickness for a given viscosity, uniformity of wafer coatings, and batch to batch reproducibility have been conducted. Spin-on equipment currently available in today's market were investigated. Automatic handling equipment made by Headway Research Inc., Macronetics and Solitec Inc., were studied for cost versus performance. The Model C-1000 wafer coating system with single track, load/unload facilities was purchased from Macronetics in Sunnyvale, California.

The Model C-1000 coater utilizes a single plane transport mechanism to convey silicon wafers through an electronically controlled process station. Push button switches control the application of power, select an operating mode (manual, semi-automatic or automatic) and control the start, stop and emergency stop, reset and carousel functions.

A three digit L.E.D. indicator provides an accurate ($\pm$ 150 R.P.M.) indication of spin motor speed. Two tanks of 5 gallon capacity feed the dispense nozzles; one contains isopropyl alcohol and the other contains the A.R. film.

Each wafer is individually processed during the process sequence. In a typical coating operation a wafer is removed from the input carrier and placed on a vacuum chuck for processing. Nitrogen is initially blown against the wafer surface to remove dust and foreign material. An A.R. film is dispensed onto the wafer which is then spun at low speed to disperse the solution. The wafer is next spun at high speed to remove any excess coating solution which results in a completely uniform A.R. coating film. At the completion of the process cycle, the wafer is removed from the vacuum chuck and loaded into the output carrier.

The model C-1000 coater used for this contract has been specifically designed to process 90mm or 3.54 inch diameter silicon wafers. The system also has the capability of processing 1.5 to 5.0 inch diameter wafers. The maximum rated throughput from this equipment is 300 wafers per hour. The mechanical yield was found to be 98%.

The experimental studies which have been formulated to investigate the viability of the spin-on anti-reflective coating technique utilized by the Model C-1000 coater were performed on batches consisting of approximately twenty-five

90mm diameter wafers. The experimental results obtained for any batch signify the average experimental value of its constituents.

The initial experiments were designed to study the effect of isopropyl alcohol as a solvent to reduce the A.R. solution viscosity. Various percentages of isopropyl alcohol, typically 10%, 25% or 50% by volume were mixed with the A.R. solution. The spinning speed of the Model C-1000 coater was maintained at 2000 RPM for 30 seconds and 5 cc of A.R. solution was dispensed on each wafer. It was found that by increasing the percentage of isopropyl alcohol in titanium-silicafilm A (viscosity 30cp), the film developed drying cracks and circles. It was therefore concluded that the addition of isopropyl alcohol to titaniumsilicafilm A did not lead to admissible results. It was found experimentally however, that the adherence quality of the film was greatly enhanced by spinning the isopropyl alcohol prior to dispensing the A.R. film and consequently all subsequent experiments were performed with an alcohol-wetted surface.

The remaining experiments performed this quarter focused on establishing the electrical characteristics and adherence quality of titaniumsilicafilm A. Titaniumsilicafilm A was spun on a surface etched batch and a texturized batch. The thickness of the A.R. coating was mathematically estimated to be 7.5 μm . This choice was based upon the height of the

pyramidal surface structure engendered during the texturizing process. Under high magnification it was observed that the pyramidal surface structure was not uniformly coated with the A.R. film. In order to correct this situation, the spin speed was reduced from 2000 RPM to 1000 RPM, whereas the total spin time was maintained at 30 seconds. The representative I-V curves which portray the electrical characteristics of a cell with and without the titaniumsilicafilm A A.R. coating is shown in Figure 13 in order accentuate the effect of the silica film. The I-V curves indicate that the solar cell which has a titaniumsilicafilm A anti-reflective coating maintains a higher energy conversion efficiency relative to the cell without an A.R. coating.

Next quarter effort will be directed towards performing similar experiments on titaniumsilicafilm B and C and then comparing the resulting electrical characteristics and adherence qualities with those of silicon monoxide and silicon nitride anti-reflective coatings.

E. SAMICS

The Solar Array Manufacturing Industry Cost Standard (SAMICS) is being applied for all hexagonal solar cell process steps and module assembly in this program. It was decided that while the time required to complete this program would be increased, the value of the SAMICS analysis would be very significant. All Format A material has been completed and

Figure 13. Titaniumsilicafilm A ($\text{TiO}_2 + \text{SiO}_2$) anti-reflective coating for three groups of solar cells. The first group is surface etched with no encapsulant. The second group is texturized and encapsulated with RTV-615. The third group is texturized with no encapsulant. The solar cells are hexagonal with 50.8cm^2 active area. They are tested at 28°C , $100\text{mW}/\text{cm}^2$ under tungsten light.

cost calculations have begun. A detailed SAMICS Final Report will be delivered to the Jet Propulsion Laboratory next quarter. The Final Report for this program will contain a summary of the SAMICS results.

CONCLUSIONS & RECOMMENDATIONS

The work performed on the development of low-cost, high energy-per-unit-area solar cell modules has led to a number of conclusions and recommendations.

Two surface macrostructure processes suitable for large scale production of solar cells were developed. The process equipment is capable of texturizing 200 ninety millimeter diameter silicon wafers in five minutes or up to 2400 wafers in one hour. The silicon wafer surface preparation and etching time, temperature, and concentration was optimized relative to surface macrostructures that trap light efficiently. The silicon wafers have black anti-reflective surfaces which are uniformly etched and are batch to batch reproducible. Intermediate steps in the surface macrostructure have indicated that higher photovoltaic efficiencies can be obtained. It is recommended that future investigative work be performed on the surface macrostructure process for producing photovoltaic energy conversion efficiencies.

A silicon solar cell laserscribing technique was studied in detail. While the laserscribe can cut through a p-n junction without damaging the junction, it was shown that the laserscribing technique was important. The laserscribing technique includes wafer alignment, laser-scribing methodology, and wafer breaking.

The laserscribing technique requires manual loading, aligning, automated laserscribing, manual unloading, and manual breaking. Development of a fully automated laserscribing system is recommended for high throughput at lower costs.

Electrical performance analysis was made for hexagonal solar cells processed with four grid pattern designs. It was experimentally shown that the electrical performance of solar cells with the same grid coverage was relatively insensitive to grid pattern coverage.

NEW TECHNOLOGY

A surface macrostructure process capable of manually processing 2400 wafers per hour was developed. The new low-cost texturizing system produces silicon wafers that have a black anti-reflective surface consisting of a sharply defined pyramidal structure; they are uniformly etched and are batch to batch reproducible. This process sequence is suitable for large scale production.

A wafer shaping process was developed which allows one to scribe a silicon wafer by laser and break the wafer to form a hexagonal solar cell. A laserscribing technique was defined which allows one to cut through a solar cell p-n junction without damaging the junction.

PROGRESS SUMMARY AND PROGRAM PLAN

The progress summary and program plan for Phase I and Phase II of the development of low-cost, high energy-per-unit-area solar cell modules is shown in Figure 14.

Figure 14. Development of Low-Cost, High Energy-Per-Unit-Area Solar Cell Modules; Phase I and Phase II Program Plan

△ Planned Goals
▲ Completed Goals

LIST OF REFERENCES

1. J. W. Thornhill, Automated Fabrication of Back Surface field Silicon Solar Cells, Spectralab Inc., NASA/Lewis Contract NAS3-20029, Final Report (August 1977), NASA-CR-135202.
2. D. B. Lee, Journal of Applied Physics, Vol. 40 No. 11 by 4569, 1969.
3. A. E. Stoller, RCA Review, Vol. 31, No. 2. pg. 271, 1970.
4. Spectralab report on "High Efficiency Solar Panel", AF APL-77-36.
5. R. A. Kaplan, "Breaking Characteristics of Laserscribed Wafers". Circuits Manufacturing, September, 1973, p. 58.
6. G. T. Jones and S. Chitre, ERDA/JPL-954605-77/3, "Development of Low-Cost, High Energy-Per-Unit-Area Solar Cell Modules," Quarterly Report No. 3, September 1977.