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SEMI-CUSTOM INTEGRATED CIRCUIT AMPLIFIER AND LEVEL DISCRIMINATOR FOR NUCLEAR AND SPACE INSTRUMENTS

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Abstract

An extra fast current feedback amplifier and a level discriminator are developed employing a dielectrically-isolated bipolar, semi-custom Application Specific Integrated Circuit (ASIC) process. These devices are specifically designed for instruments aboard spacecrafts or in portable packages requiring low power and weight. The amplifier adopts current feedback for a unity-gain bandwidth of 90 MHz while consuming 50 mW. The level discriminator uses a complementary output driver for balanced positive and negative response times. The power consumption of these devices can be programmed by external resistors for optimal speed and power trade-off.

I. INTRODUCTION

Nuclear instruments for detecting energetic particles and photons aboard spacecraft or in a portable package has to meet demanding operational requirements such as light weight, low power consumption and small volume. In addition, the components and material used in the instruments need to be radiation-hard for total dose and, for some applications, should be latch-up free for transient dose rates.

Such requirements severely limit the component types available to the instrument designers and, as a consequence, some high-speed, low-noise circuit designs had to be carried out with discrete components either on printed circuit board or in hybrid forms resulting in inefficient use of weight and power. Monolithic, rad-hard integrated circuits for such applications should greatly simplify the design and implementation. Thus, the two most frequently needed function blocks in our instruments were identified for monolithic integration; a low-noise, wide-band amplifier and a level discriminator. The following chapters describe the selection of a wafer fabrication process, the design and performance data of the two integrated circuit devices.

II. SELECTION OF A FABRICATION PROCESS

Various wafer process technologies were examined from the points of view of fabrication cost, circuit speed, noise and radiation-hardness. Since the production quantities of

the devices were moderate, less than one thousand units per order, a semicustom tile-array process presented the most cost effective alternative. In a tile array process, transistors of various geometries are prearranged in tile-like patterns on a die, and the customer specifies interconnections using up to two layers of metalization to suit the design.

The electrical performance, especially the speed and noise of the amplifier and the response time of the level discriminator, was another major consideration in the design of the two circuits. The bipolar process was selected for its low $1/f$ noise and better frequency responses of the available transistors over MOS process. In addition, dielectric isolation technology was chosen for its virtually latch-up free operation as well as the availability of vertical geometry PNP transistors which are complementary to NPNs in frequency responses. In dielectric isolation process, each transistor is completely isolated from the substrate in a silicon-dioxide tub. Bipolar transistors also avoid radiation-induced threshold shift of MOS gate oxides. MOS process would also require extra process steps such as trench isolation and silicon-on-insulator processes for latch-up free operations.

In the end, SP1104 tile array of 20V process (V_{cb0} , $V_{ce0} = 20V$) by DataLinear, Milpitas, CA, was chosen for the implementation. The tile array also carries NiCr resistors which can be laser-trimmed if required. The device model library for spice simulation was obtained from the vendor for design and analysis. The cutoff frequencies of the available transistors are relatively high; up to 900 MHz for NPN and 600 MHz for PNP single geometry transistors.

III. CURRENT FEEDBACK AMPLIFIER

A. Design

The main design goals of the amplifier were to provide the supply current adjustability and to exploit the most of the available transistor capabilities. The rise and fall times and the slew rate of the amplifier should be about an order better than conventional operational amplifiers at similar power consumption levels. In addition, the circuit should be protected from any photocurrent burn-out caused by strong transient radiation. Thus, no short-circuit path is allowed between any terminal leads when the bulk semiconductor changes to conductors during transient radiation. This required small value NiCr resistors distributed throughout the circuit branches as current limiters.

Since the amplifier was to handle mostly low duty cycle pulses, the offset specifications were of secondary importance, and the input bias current of a few μA was considered acceptable since the source impedance would usually be small, 1k ohms at most. A Current Feedback Amplifier (CFA) with complementary topology meets these requirements very well. The operational principles and designs of current feedback amplifier can be found in many publications [1,2].

The CFA has four distinct stages of complementary NPN and PNP transistors as shown in Figure 1. The first stage including transistors Q1 through Q8 makes up the current sources which set amplifier bias currents and provide voltage translation for the non-inverting input signal into the next stage. The two complementary current sources can be adjusted by two external resistors, which also provide DC output offset control at the same time. The emitter degeneration resistors at Q1 and Q4 help to stabilize the temperature effect of the current sources. This stage draws currents of about 0.4mA for nominal operation.

The second stage consists of transistors Q9, Q10, Q17 and Q18, and is the major gain stage of the amplifier. Double-base geometry transistors were opted for the input transistors for lower base spread resistance and thus lower input voltage noise density. R4 and R5 limit the transient photo-current between inverting and non-inverting input terminals. Mirroring the first stage current, this stage also is run at 0.4 mA for nominal operation.

Transistors Q11 through Q14 comprises the third stage, and work as the current mirror with gain. It also provides bias setting of the output voltage follower. Due to the 4X geometry of the double-base transistors (Q11 and Q14) mirroring the single-geometry transistors (Q17 and Q18), there is a current gain of about four. The current gain of the double-base transistors helps to increase the slew rate of the amplifier as it drives the high-impedance node which exists at the collectors of Q11 and Q14. The amplifier open loop gain and the dominant pole location are determined by the behavior of these nodes. The input impedance of the emitter follower output stage and the combined output capacitances of Q11 and Q14 as well as distributed capacitances of the node place the dominant pole at about 1 MHz and DC gain of approximately 1000 for a 500 ohm load.

The emitter degeneration resistors at the current mirrors reduce the effect of the transistor miss-match and limits transient photocurrents induced by radiation bursts. The degeneration resistors are of NiCr type for excellent temperature and radiation stability. This stage draws approximately four times the current of the previous stage at about 1.6 mA nominal. The straight-forward current mirror design was selected over more elaborate ones such as Wilson type [3] to obtain larger output voltage swing amplitude. At $\pm 6\text{ V}$ supply voltages, output swing is better than 9 Vp-p. Wilson mirror circuit would have helped to improve the phase margin somewhat at the expense of

Fig. 1 Current Feedback Amplifier schematic

the output swing of about 1.4 V_{p-p}. More conventional approach of two-stage output buffering was not followed to save power.

The output drive stage is a conventional complementary emitter followers of multiple-geometry (two base and collector connections each) transistors for high current drive capability. The amplifier can drive 100 ohm load with some degradation in performance as compared to that of recommended 500 ohm load. The output stage is current limited by monitoring the collector currents of the Q15 and Q16 and driving inverting input towards reducing the output voltage. The amplifier is thus output short-circuit protected. Both straight output terminal and one with 33 ohm series resistance are provided for convenience. The terminal with series resistance is useful for isolating capacitive load from the straight output terminal, which is used for feedback connection.

Two identical amplifiers sharing a common die but laid out in a mirror image of each other are housed in a 16-pin, side-brazed, dual-in-line (DIP) package for higher circuit density. The two amplifiers are completely independent of each other, down to the power supply connections, for flexibility and isolation. An 1.8k ohm internal feedback resistor is provided for narrow bandwidth (<10 MHz) and large gain applications. However, for most high speed operations, a 2k ohm external resistor in parallel with the 1.8k (for an effective resistance of about 950 ohms) is recommended.

Breadboarding of the amplifier designs using manufacturer-supplied evaluation kit transistors was useful only to the extent of determining bias conditions. Otherwise, the amplifier design relied heavily on SPICE simulations, which agreed well with the actual measurements as shown in the following section.

Table I
CFA performance summary

SPECIFIED FOR:		SUPPLY CURRENT	
+/-V _{cc} =6V R _f = 930 Gain=5		2.0 mA	4.2 mA
Temperature = 25°C		R _L = 1000	R _L = 500
PARAMETER	CONDITIONS		
Frequency Response (MHz)			
-3dB bandwidth V _{out} = 250mV _{pp}		60	85
V _{out} = 2.5V _{pp}		39	60
Rise & Fall times (tr, tf) (ns)			
V _{out} = 250mV _{pp} tr		5.1	3.9
if		5.0	3.9
V _{out} = 2.5V _{pp} tr		7.0	4.2
tf		8.4	5.6
Slew Rate (V/us) +SR		380	700
5.0V _{pp} output swing -SR		300	440
Equiv. input noise voltage density nV/(Hz) ^{1/2} @ >100kHz			2.8
Input Bias Current (uA) non-inverting input			<10

B. Performance

Table I summarizes the major performance data of the amplifier at two different supply current settings as determined by the set resistors. The rise and fall times are less than 4 nS at a gain of 5 while consuming 50 mW at +/- 6 V. A scope picture of an output waveform of the amplifier at a gain of five (5) is shown in Figure 2. The amplifier is recommended for non-inverting gains between 5 and 25. For inverting operations, the recommended gain ranges from -1 to -20.

Exhibiting the typical characteristics of current feedback amplifier, the amplifier bandwidth does not decrease as rapidly as conventional voltage-feedback amplifiers as can be seen in Figure 3. For gains between -1 and -20, the bandwidth changed from 90 MHz to 45 MHz.

While the amplifier is characterized for +/-6 V operation at various current settings, the supply voltage can be increased to +/-12 V without any danger of breakdown. The noise performance of the amplifier is better than most of the commercial devices of comparable speed, lower than 2.8 nV/(Hz)^{1/2} above 100 kHz.

Fig. 2 Scope trace of a CFA output
(Gain=5, +/-I_{cc}=4.2 mA, R_f=950 ohm)

Fig. 3 Frequency responses of CFA at various gains

IV. COMPLEMENTARY LEVEL DISCRIMINATOR

A. Design

Many of the design goals of the current feedback amplifier still apply to the complementary level discriminator (CLD) design as well. These include the supply current programmability, protection from photocurrent burnout and the best possible response time from the available transistors. It was also desired that the output voltage swing matches that of the input requirements of various CMOS logic devices operating at $V_{CC}=5\text{ V}$ when $\pm 6\text{ V}$ supply is used for the discriminator. Figure 4 shows the schematic of the level discriminator as fabricated.

The bias current of the entire circuit is controlled by a current setting branch consisting of Q7, Q8 and Q9. A current programming resistor between Q9 emitter and Q7 collector determines the branch current, which in turn is reflected throughout the rest of the circuits.

The circuit has the usual differential input stage of transistors Q1 and Q2 with resistive collector loads driving a second differential stage of Q3 and Q4. The input stage is conventional without bias current cancellation circuit, as the source impedance driving the input terminal is usually quite low, tens of ohms presented by the series resistance in the case of the current feedback amplifier described in previous chapter.

The collectors of the second differential amplifier stage drive complementary current mirror-multipliers to the

output terminal using the multiple-base and collector geometry transistors Q6 and Q19 as mirrors. The transistors Q23 and Q26 are to shunt the excess collector currents from Q6 and Q21, respectively, back to the current sources for self balance. Thus in the case of no DC load at the output terminal, the diode currents through Q23 and Q26 will supply four-fifths of the collector currents of Q16 and Q3, respectively. The use of emitter degeneration resistors not only compensates the mismatch of the mirror transistors, but also limits the transient photocurrents as well.

Transistors Q20, Q21, Q24 and Q25 forces the output "Low" state to very near 0 volt by maintaining the Q21 base voltage at two diode drops below ground level. This circuit is activated only when the output is at low state. Transistor Q22 is to reduce the output swing below 5 V (to be compatible with the more common logic input levels) when $\pm 6\text{ V}$ supplies are used for the device.

Since the output terminal is driven essentially by complementary current sources, the device cannot be damaged even when the output terminal is shorted. The complementary nature of the output circuit also makes it possible to achieve balanced response times between positive and negative input pulses. It also eliminates the need for external pull-up or pull-down load for the output terminal.

The gain of the CLD is about 5000 with a load of 10k ohms, so the device responds to a differential signal as small as a millivolt for a full output voltage.

Fig. 4 Complementary Level Discriminator schematic

As in current feedback amplifier, two identical discriminators sharing a common die but laid out in a mirror image of each other are housed in a 16-pin, side-brazed, dual-in-line (DIP) package. The two devices are completely independent of each other, down to the power supply connections, for flexibility and isolation. Again, the breadboarding of the development circuit of evaluation kit transistors could not predict the performance of the final circuit other than bias conditions and supply currents.

B. Performance

Figure 5 sums up the performance of the discriminator for various overdrive voltages at several power settings. The measured positive and negative response times were 34 nS and 40 nS, respectively, for an overdrive voltage of 10 mV while consuming 24 mW at ± 6 V. A scope trace of the response time is shown in Figure 6.

Over the temperature range of -55 to $+125$ $^{\circ}\text{C}$, the positive response time changed less than 5 nS, while the negative response time increased by up to 25 nS at $+125$ $^{\circ}\text{C}$. The input bias current over the same temperature range remained less than 5 μA .

The output swing using supply voltages of ± 6 V and a load resistance of 10k ohms is 0.1 V to 4.5 V. A load resistor is not required for operation and in this case the output increases to 4.6 V. The output swing for ± 5 V supplies was from 0.1 V to 3.6 V. This is sufficient to drive the inputs of CMOS logic devices using 4.5 V supplies.

Fig. 5 CLD response times vs. overdrive at various power levels

Fig. 6 Scope trace of a CLD output (10 mV overdrive, 24 mW)

V. RADIATION TEST RESULTS

Both CFA and CLD devices have been tested for total-dose radiation hardness in a cobalt-60 Gamma-Cell (model 220) at Los Alamos National Laboratory. The CFA test parameters measured against accumulated dose levels include supply currents, non-inverting input bias current, output offset voltage and the rise and fall times. All were measured with the amplifier gain of five and power consumption of 50 mW. The CLD test parameters measured were; input bias current, input offset voltage and the supply currents which were set initially for 24 mW power consumption. ± 6 V supplies were used throughout the measurements.

Two devices each of CFA and CLD were exposed to the radiation while powered on continuously. Additional two devices each were irradiated with the power off. Two more devices each were tested as control samples. The dose rate of the Gamma-Cell was calibrated at approximately 650 Rads/min on the average. Except for the duration of 12-minute test period, the test circuits were continuously exposed to the radiation inside the cell. The circuits accumulated approximately 5 MRad of dose in approximately five(5) days of exposure.

No significant change in any of the CFA parameters was observed. The non-inverting input bias current fluctuated by as much as 30% of the pre-irradiation values, but all devices ended the test with slightly less bias currents than those of starting values. Since the input bias current is mainly created by the mismatch of the two balanced current sources, the fluctuation was apparently caused by the difference in gain changes of the two transistors used as current sources.

CLD test results show a more predictable behavior than that of CFA as shown in Figure 7. The input bias currents (as measured on one of the two input base terminals of the differential pair while the other transistor is turned off) increased monotonically up to the dose level of 1 MRad.

Fig. 7 CLD bias currents vs. total dose ('on' for normally-on devices, 'off' for normally-off devices)

At or near 1M Rad, however, the input bias currents, either started decreasing in the case of normally powered-on units, or reached a plateau for the normally powered-off units. The difference in behavior between the two groups of devices is clearly seen in the graph.

Transient dose-rate test was performed with a Scandi-Flash X-ray burst generator which is capable of dose rates

of up to 2×10^8 Rad/S at 10 cm from the anode electrode. After two shots each of the X-ray bursts, no change in circuit behavior was observed.

VI. CONCLUSION

Semicustom, bipolar ASICs with dielectric-isolation process for developing special purpose circuits to be used in a radiation environment such as in space or in nuclear power plant proved to be a cost effective and practical alternative to either discrete or hybrid designs. The circuit behaved satisfactorily in speed for radiation doses up to 5M Rads.

The design of the ASICs can be performed easily on an IBM-PC compatible computers using SPICE with manufacturer-supplied device libraries for various transistor geometries. The SPICE simulation agreed quite well with the measured data except for the saturation recovery behavior, for which the simulation results were generally more severe than the actual. The speed of the circuits were generally close to the predicted values.

VII. REFERENCES

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