2
5-1-79
SAND79-0329

MULTIPLE APPLICATION CODED SWITCH DEVELOPMENT REPORT

E. L. BERNAL AND J. D. KESTLY

Prepared by Sandia Laboratories, Albuquerque, New Mexico 87115
and Livermore, California 94550 for the United States Energy Research
and Development Administration under Contract AT (29-1) 789

MARCH 1979

Sandia Laboratories

SF 2900 Q(7-73)

MASTER

SAND79-0329

Printed March 1979

MULTIPLE APPLICATION CODED SWITCH DEVELOPMENT REPORT

E. L. Bernal and J. D. Kestly
Command and Control Division 2335
Sandia Laboratories
Albuquerque, New Mexico 87185

Abstract

The development of the Multiple Application Coded Switch (MACS) and its related controller are documented; the functional and electrical characteristics are described; the interface requirements defined, and a troubleshooting guide provided.

ABSTRACT
The Multiple Application Coded Switch (MACS) is a
programmable logic device which can be configured
to perform a wide variety of switching functions.
The MACS is designed to be used in a variety of
applications, including data processing, control
systems, and communications. The MACS is a
highly flexible device which can be configured
to perform a wide variety of switching functions.
The MACS is designed to be used in a variety of
applications, including data processing, control
systems, and communications. The MACS is a
highly flexible device which can be configured
to perform a wide variety of switching functions.

Acknowledgment

The authors wish to acknowledge C. C. Bates and D. J. Grab for switch, display and relay selection and evaluation. C. H. Purdue provided test equipment design and program development for the PT used for final acceptance testing. D. R. Leonard provided drafting support and mechanical inputs. C. L. Sparks provided systems interface definition and R. L. Nagel provided the core memory design. W. G. Merritt assisted in Sparton Southwest production activities. R. E. Bair and T. L. Workman provided the initial concepts of the M.A.C.S.

TABLE OF CONTENTS

	<u>Page</u>
I. Overview	
Introduction	7
System Description	7
Interface Characteristics	8
Monitor Indications	12
II. The MACS Controller, TC811A	
General	12
Functional Operation	14
Electrical Operation	15
Troubleshooting	17
III. The Coded Switch, TC810	
General	24
Functional Operation	24
Electrical Operation	26
Troubleshooting	27

LIST OF FIGURES

FIGURE

1	MACS System	9
2	Interface Cable Definition	10
3	TC811A Mechanical Compatibility Drawing (SB-S16261)	13
4	Block Diagram, TC811A	16
5	Timing Diagram for TC811A	16
6	Printed Wiring Assembly, MACS Controller (S16944)	20
7	Mechanical Compatibility, MACS Switch (SB-S11755)	25
8	Block Diagram, TC810	26
9	Printed Wiring Assembly, MACS Switch (S16941)	40
10	Printed Wiring Assembly (2), MACS Switch (S18459)	41
11	Schematic, MACS Switch (CK-S11755)	42
12	Schematic, MACS Controller (CK-S16261)	43
13	Multiple Application Coded Switch and Controller	44

MULTIPLE APPLICATION CODED SWITCH DEVELOPMENT REPORT

I. OVERVIEW

Introduction

The Multiple Application Coded Switch System is comprised of two units, a Multiple Application Coded Switch (MACS) TC810 and a MACS Controller TC811A. The system was designed to be a universal, inexpensive, unclassified coded switch system which would be used for a number of military and civilian applications to control access to a secured area where sensitive material would be stored. In particular, the system was designed for the Safe Secure Trailer System used for secure transportation of nuclear material.

System Description

The MACS is a single code coded switch with a remotely recodable permanently stored 16-bit code word. There are 65,536 possible code words which can be stored in the 16-bit magnetic core memory of the coded switch. The coded switch has four sets of 5 amp form C output contacts which are controlled by the coded switch logic.

In order to operate the output relays to the "accessed" state, one must enter a code word in 4 hexadecimal digits into the MACS controller which then communicates the trial code in a specified format over a user supplied interface cable to the coded switch. The coded switch interprets the trial code, compares it to its stored code word and, if the words are the same, it operates the output relays contacts into the "accessed" state. In addition, two other relay contacts are transferred; a monitor contact and another switch contact which enables recoding of the coded switch. If an attempt is made to access a MACS with a wrong trial code, a 30 ±10 second time delay is required before the coded switch can be interrogated again. Any interrogation made in the interim is ignored. This requires a minimum 40 second delay between bad tries to guarantee that the coded switch will respond to the next attempt. This allows 90 bad tries in an hour for the individual attempting to determine the code. A minimum delay of 20 seconds would allow a maximum of 180 tries per hour. The worst case

bypass time, based on 20 second delays and 180 bad tries per hour with random guesses of the stored code, is calculated to be 3 hours 39 minutes for a one percent chance of determining the stored code.

In the "accessed" state the operator can change the code in the system by performing a recode operation. This operation is performed by putting the desired new code into the controller and operating the already accessed coded switch with the controller. Inadvertent recoding of the coded switch is prevented by an arrangement on the function select switch which requires a positive action to transfer the contacts and a recode enabling switch located in the secure volume which requires two-man action for a recoding operation.

The coded switch can be changed from its accessed state to its secured state by using the secure function of the controller. This function requires that the code entry switches in the controller be returned to a code of all zeros, thus removing any evidence of what codes were stored in the system. The controller then operates the coded switch and the contacts of the output relays are transferred back to the secured position. In this state, the monitor contacts are in the secured monitor position and the recoding capability is disabled.

The coded switch system has been studied for its ability to withstand a countermeasures threat represented by a small group of technically competent individuals having access to all unclassified drawings of the coded switch system as it is installed in a safe secure trailer but without knowledge of the code stored in the coded switch. The coded switch was determined to be well enough shielded and protected that emanations from the coded switch would not reveal code information with the defined threat. In addition, bypass of the coded switch by overvolutaging and grounding combinations of input lines was studied. As a result of these studies, STS system grounding and diode protection requirements have been established and no practical bypass means have been found.

The coded switch system is designed to meet a nominal set of military environments as specified in Sandia Drawing: PS-S16261 for the controller and PS-S11755 for the coded switch.

Interface Characteristics

The MACS system drawn in Figure 1 shows the minimum set of elements required for a working MACS system. The external 28 volts power supply

provides power to the controller and to the input side of the opto-isolators in the coded switch. The internal 28 volt power supply is isolated except for a single point common ground from external power and supplies logic power and output relay drive power to the coded switch. This isolation is critical to the security of the stored codes.

FIGURE 1. MACS SYSTEM

The system interface cable, schematically described in Figure 2, shows the nine lines comprising the command and control interface between the controller and the coded switch.

FIGURE 2. INTERFACE CABLE DEFINITION

The power control line has an active high signal at the beginning of a Recode or Access operation to power up the MACS and initialize logic in preparation for controller commands. The clock is a 50 percent duty cycle square wave with a period of approximately 6 milliseconds and is active low. It commences with a negative going leading edge approximately 10 milliseconds after the power control signal appears. It is synchronous with the data transfer on the data line and is the logic clock for the coded switch sequencer. The 16-bit trail code data is an active low, negative logic signal. Bits change on the negative going edge of the controller clock pulse and are interpreted by the MACS on the positive going edge of the same clock pulse. Data transfer occurs during the third through eighteenth controller clock pulse and the bit sequence is defined in PS-S16261. Approximately 5 milliseconds after a complete 16-bit data transfer has occurred in an "access" operation, the contacts of the output relay will transfer and the monitor status of the active low negative logic ACCESS monitor line will go low and the active low negative logic SECURE monitor line will go high.

For recoding to occur the Recode Enable line is active low. It is active at the MACS only if the Recode Enabling switch is closed. This switch acts as an administrative control and does not allow the coded switch to be recoded by unauthorized personnel. Authorization is provided by closure of the Recode Enable switch from inside the SST making one man or unintentional recoding less likely to occur since one man inside the secure volume controls the Recode Enabling switch (S1) and another man controls the function select switch on the controller. After a recode operation, the contacts of the output relay will remain in the accessed state. The access line, which does not come out of the secured volume, enables the coded switch to be directly accessed with ground applied to the ACCESS line (J1 pin L) in conjunction with 28 volts on MACS power control and power in lines. (See Figure 1) This is useful for accessing the coded switch without taking it apart when the coded switch contains an unknown code and physical access to the coded switch is not precluded.

With the code wheels of the controller returned to an all zeros code and the operate switch depressed, the power control line goes to 28 volts simultaneous with the secure line going to ground. This actuates the output magnetic latching relays to their secured state. The clock, data, and recode enable lines are inactive during this operation.

Within 5 milliseconds of the application of the power control and

secure signals, the output relay contacts will transfer to the secure state, the secure monitor line will become active, and the access line inactive.

Monitor Indications

Access Monitor Indication - The Access monitor indicator, located on the front panel of the MACS controller, is actuated by a closed relay contact to ground in the MACS switch when the coded switch is in the Accessed state. The signal is assigned to J1-Pin E of the system interface cable. (See Figure 2) The Access monitor indication is displayed on the MACS controller whenever the MACS switch is accessed even though the MACS controller function switch may be turned off. This is done because the SST, while in transport, should always be secured; and if it is not, the Access state should be immediately obvious to operating personnel.

Secure Monitor Indication - The Secure monitor indicator, located on the front panel of the MACS controller, is actuated by a closed relay contact to ground in the MACS switch when the coded switch is in the Secured state. The signal is assigned to J1-Pin F of the system interface cable. The monitor is only displayed when the function selection switch of the MACS controller is in a position other than the off position.

Tamper Monitor Indication - This circuit is not used in the SST application but is provided as part of the design to latch a relay on at some remote monitor location to warn of an attempt to tamper with the system. The tamper monitor indication is an active low signal with a 600 Ω series current limiting resistor and is active low when power is applied to the MACS, the power control line is active, and when the 20 - 40 second inhibit timer is active.

II. THE MACS CONTROLLER, TC811A

General

Figure 3, extracted from the interface compatibility drawing SB-S16261, shows the outline of the MACS controller. The front panel has four Dzus fasteners for attachment to the next assembly and an edge lit front panel which is illuminated by two lamps on each side of the function select switch

in the center of the panel. The lamps are lit if the function select switch is not off and power is applied to the controller. Two monitor lamps are located on the upper right side of the front panel, the secure lamp lens is clear, the access lamp lens is amber.

All front panel lamps are GE327 type lamps. In addition, four more lamps are used in the thumbwheel switch assembly located in the upper left side of the panel. These lamps are T1 bulbs and the rear cover of the controller must be removed to replace them. The thumbwheel switch assembly is a 4-deck hexadecimal digit switch with character format 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, E, J, L, M, P, R in increasing hexadecimal order. The digits are covered by two security covers: the "A" cover covering the two left-hand digits, the "B" cover covering the two right-hand digits. The lockwiring device on each cover provides code security for half the code at a time and enables split code operation whereby two operators, each knowing two digits of code information, can operate the coded switch system only as a team. The controller dust cover is removable by removing seven screws around the edge of the cover and four more at the back of the unit. The controller unit has an inner electronic assembly which is connected to the front panel by a cable bundle. Great care must be exercised so that damage to the internal connections of the controller will not occur by overflexing or otherwise overstressing the cable.

The LJT 07-15-155 connector mounted on the back of the unit connects to the grounded shielded cable of the next assembly which interfaces with the coded switch and external power source of the next assembly.

The inner electronic assembly is packaged in its own moisture sealed and EMI sealed box. It is intended that repair of the electronics in the inner box be done only at Sparten Southwest, Albuquerque.

Functional Operation

There are four functions which the controller can perform on the system: Access; Secure; Recode; and Code Check. These functions are comprised of three basic operations.

Access - The Access operation is performed with the function select switch in the access position. The operator who knows the "A" half of the code enters his two digits into the thumbwheel under the "A" cover and lockwires the covers down, the other operator who knows the "B" half of the code enters his half under the "B" cover and lockwires his cover down.

If a bad try was previously executed, the operator must wait 40 seconds to guarantee that the bad try timer in the coded switch has timed out, and then pushes the operate toggle momentarily up. The controller should respond with an access monitor condition within a second. If not, a bad try was performed and another operation or other appropriate action on the system will have to be performed.

Secure - With the function select switch in the secure position and with all four code entry switches returned to their zero positions, the operator must push the toggle switch momentarily. The controller monitor lights should transfer immediately to indicate a secured state. If not, a system fault has occurred and repair will be necessary.

Recode - With the system in the accessed state, the new code is entered into the controller as was done in the access operation. The operator must pull out and rotate the function select switch to the recode position, close the recode enable switch in the secure volume, and push the operate toggle switch momentarily and the recode function will be performed.

Code Check - The code check operation is performed on the MACS system before the trailer system doors are irrevocably locked with the coded switch. It is comprised of a secure function to operate the locking system to lock with the doors to the secured volume still open, followed by an attempt to access. If the access is successful, the locking system will return from lock and the code check is complete. The system can then be secured with the new stored code information inserted and verified.

Electrical Operation

Figure 4 is a simplified block diagram of the MACS controller and Figure 5 illustrates the timing of the electrical interface signals.

Logic Power - The TC 11A derives its internal logic power from a 100 milliamp 12 volt $\pm 10\%$ μ a 723 power supply. The power supply has a .27 μ F filter capacitor located near the power supply. This capacitor stabilizes the circuit oscillations as well as provides current surge capacity to the power source during CMOS switching.

FIGURE 4. BLOCK DIAGRAM, TC811A

FIGURE 5. TIMING DIAGRAM FOR TC811A

Data - The basic logic system is comprised of a 15-bit shift register. The shift register, two CD4021 8-bit parallel-in/serial-out shift registers, has an asynchronous data load with a negative logic clock with data transfer on the positive leading edge.

Clock - The clock circuit consists of a CD4047 Astable multivibrator. The clock has a 6 millisecond 50 percent duty cycle period. The clock is gated on a 10 millisecond timer to assure proper operation. It is held on for a period of 365 milliseconds upon release of the operate switch.

Power Control - Power control consists of a 30 volt signal switched on through a PNP (SA10311) transistor and associated discrete circuitry. Power control is begun as soon as the operate switch is pushed and is held on for as long as the operate switch is plus 365 milliseconds $\pm$ 50 milliseconds.

Secure - The secure circuit consists of a ground signal being applied to pin D and power control going high. Power control will be inhibited if the sense circuit (Q100) senses a non-zero on any of the thumbwheel switches.

Troubleshooting

All nomenclature is referenced to CK-516261. Place +28V dc on pin N of J1 and common to pin G and H. Place the five position switch to ACCESS position. On pin J place a 34 ohm 50 watt resistor to ground. Place the scope lead to pin J and push the operate switch to the operate position. The voltage on pin J should rise from 0 volts to +28V dc $\pm$ 4 volts.

Place a 125 ohm 10 watt resistor on pin B of J1 to +28V dc. Place the scope lead on pin B and trigger on pin J. Push the operate switch to the operate position. The clock line should start out high and remain high (+28V dc) for $10\text{ms} \pm 2\text{ms}$ then go to ground for 3ms and then return high for 3ms. This should continue for as long as the operate switch is pushed up. Upon release of the operate switch, the clock should remain running for $350\text{ms} \pm 25\text{ms}$.

Place a 125 ohm 10 watt resistor between pin C and +28V dc. Place a code of 5555 into thumbwheel switches. Trigger OFF of pin B (clock). Push operate switch up and the following wave forms should be observed.

Place a 125 ohm 10 watt resistor on pin D. Rotate the five position switch to secure position. Place the scope lead on pin D and push the operate switch up. The voltage on pin D should go from +28V dc to ground.

1. Power Control Test

Refer to Figure 6, Controller Board Printed Wiring Assembly, for location of referenced components. Place the scope lead on the collector of Q103. Push operate switch up. The collector should go to within a few tenths of a volt of ground.

Place a scope lead on pin 12 of U103. With the operate switch in the on position, the voltage should be at 12 volts.

Place a scope lead on pin 13 of U103 and push the operate switch. Pin 13 should go from +12V dc to ground.

2. Clock Test

Place a scope lead on pin 4 of U102. Push the operate switch to the operate position. Clock pulses should be present.

Place a scope lead on pin 5 of U102. Clock pulses should be present.

Move the scope lead on pin 9 to U105. Clock pulses should be present. If not, check U105 circuits.

NOTE: Clock pulses are generated by U105 only when pin 5 is at +12V dc. This is accomplished when the operate switch is pushed to the operate position.

3. Data Test

Place a code of 5555 into thumbwheel switches. Place the scope lead on the base of Q101 and operate the controller. Data pulses should be present.

Place the scope lead on pin 2 of U102. Data pulses should be present

Data bits are generated by U100 and U101 (parallel IN/Serial OUT) shift registers. If no data is being generated, then these two circuits should be checked.

4. Secure Test

The secure operation causes pin D of J1 to be at ground potential and pin J of J1 to be at +28 volts. This operation results when S100 is placed in the secure position and S101 is pushed to the operate position.

III. THE CODED SWITCH, TC810

General

Figure 7 (extracted from the MACS interface compatibility drawing SB-S11755), shows the external configuration of the MACS. The coded switch container is moisture sealed and is designed to be rugged enough so that normal handling of the unit during installation and maintenance will not degrade its performance. The unit was subjected to special tests to assure that normal vibration, normal and abnormal shocks, external magnetic fields, overvoltages on interface cable lines as well as electrostatic discharges transmitted to the MACS from the trailer assembly with the MACS mounted to the trailer would not alter the state of the MACS output relays, alter its stored memory or degrade its performance. The MACS was not required to meet an EMR environment, and it was left to the next assembly to provide cable shielding, external shielding, and interface cable filtering as required to meet an EMR requirement. The MACS, however, was tested to both incident and direct coupled radiation tests and the report for both the MACS and the MACS controller is in Division 2335 files.

Functional Operation

There are three coded switch responses which the controller can evoke: Access; Secure; and Recode.

Access - The Access operation can be performed by applying a proper code to the TC810. The Access operation checks the code being entered with the contents in memory. If this is properly performed, then the output relay is transferred to the Access position.

Secure - The Secure operation can be performed by applying power and a ground signal from the TC811A. This operation only transfers the output relay from the Access state to the Secure state.

Recode - With the system in the Access state, a Recode of the memory can be accomplished. During a Recode operation, the memory is charged to the code that is being presented to it.

Electrical Operation

Figure 8 is a simplified block diagram of the coded switch.

FIGURE 8. BLOCK DIAGRAM, TC810

Sequencer - The Sequencer is a CD4017 divide-by-ten Johnson counter with decoded outputs. The Sequencer is run by a divide-by-two clock. States one through eight address the memory and state nine provides the output pulse for the output drive circuit.

Memory - The Memory consists of: 16 magnetic cores; read generator; write generator; and sense amp. When the Memory is addressed, the read generator develops a 10 μ s write pulse which reads the contents out of the bit being addressed. The sense amp senses the contents in the memory and allows the write generator to write the contents back into that bit. This sequence is repeated until all 16 bits are addressed.

Read Generator - The Read Generator consists of a PNP transistor and associated discrete circuitry. Read pulses (20 μ s) are generated on the negative going edge of the clock pulse. A minimum of 16 read pulses are generated.

Write Generator - The Write Generator consists of an NPN transistor and associated discrete circuitry. Write pulses (20 μ s) are generated on the positive going edge of a clock pulse. The write pulses are ANDed, together with data pulses during a recode operation or during an attempted access.

Data Compare - Data Compare is done only during an Access attempt. The Data Compare circuit consists of an EXCLUSIVE-OR gate. Data at this gate is compared with what is read out of memory during a memory address. When a wrong bit is compared, then the limited try counter is invoked.

Try Counter - The Try Counter is invoked when a bad data compare is made and the ninth state of the sequencer is present. The Try Counter consists of an RC which is charged to +12 volts when invoked and will discharge to 50 percent of that level before the inhibit is taken off. The limited try counter prevents the memory from being addressed.

Troubleshooting

In order to perform the following trouble shooting procedure, a known good TC811A must be connected to the TC810 under test. All nomenclature is referred to the coded switch schematic, CK-S11755.

Place TC811A in Recode Enable position. Access light should be on.

1. Operational Check

Set code of (RRRR) into thumbwheel switches. Push operate switch to operate. Place code of (0000) into thumbwheel switch and go to Secure position. Push operate switch to operation position. The monitor lights should indicate the secure status.

Place TC811 in Access position and put a code of (RRRR) into thumbwheel switches. Push operate switch to operate position; the monitor lights should indicate the access status.

2. Voltage Regulator Power

To have +12 volt logic present, the following signals must be present at J1.

- a) +28 volts on pin J
- b) +28 volts on pin N
- c) Common at G and H

Place a scope lead on U109, pin 10. With power (+28V dc) applied to J1, pins J and N, the scope should indicate +12V dc $\pm$ 0.5V.

Place scope lead on U109, pin 11 or 12. Twenty-eight volts should be present at this point.

Place scope lead on K101, pin X2 which should be at ground potential. If not at ground, place scope lead on base of Q113. This point should be at approximately 12 volts.

CHECK Q201 circuit.

3. Clock

In order to receive a clock signal, the following signals must be present at J1.

- a) +28 volts on pins J and N
- b) Ground on pins G and H
- c) A clock signal being generated on pin B.

Place the scope lead on point pin 6 of U103. A clock signal should be observed as in the diagram below.

Place scope lead on pin 5. Clock signal present?

Place scope lead on pin 2 of Q202. Clock signal present?

Check Recode Enable circuit pin 2 of U104.

4. Memory

In order to troubleshoot the memory properly, the following steps should be done to the TC810.

- a) Connect a TC811A to the TC810.
- b) Set controller to Recode/Enable position and set a code of all R's into thumbwheel switches. Complete a recode operation, then secure the coded switch.
- c) Place controller in the Access position; then set in a code of all zeros (Ref.: CK-S1755).

Place a scope lead on pin 4 of U105. Push the operate switch on the controller. Observe write pulses on the scope (maximum of 16).

Check to see if 16 write pulses are being generated.

5. Sense Amp Test

Place a test lead on pin 11 of U104. With all one's in the memory, 16 one's should be read out of memory.

Reset for the RS flip-flop is accomplished by the clock signal on pin 13 of U104.

Sixteen low pulses should be present on pin 11.

Is failure a total memory failure?

Determine which bits are missing by the following chart.

Bit No.

1
2
3
4
5
6
7
8

Core No.

L104	—	R100
L105	—	
L103	—	R101
L106	—	
L102	—	R102
L107	—	
L101	—	R103
L108	—	

<u>Bit No.</u>	<u>Core No.</u>
9	L116
10	L109
11	L115
12	L110
13	L114
14	L111
15	L113
16	L112

The preceding chart will help determine which bit is missing and which point to next place the scope lead

Typical wave form. If it is

- a) Read pulse → Go to Section 6 - Read Test.
- b) Write pulse → Go to Section 7 - Write Test.
- c) No output → Check U107 and U108 outputs.

6. Read Test

Read pulses are generated on the negative going edge of the clock pulse. The read generator consists of Q111 and associated circuitry.

Place a scope lead on pin 6 of U100 and a second lead on pin 3. The following wave forms should be observed.

Total pulses present?

Place a scope lead on pin 2 of U100. A minimum of 16 read pulses should be present.

Place a scope lead on pin 1 of U100. A divide-by-two clock should be present.

7. Write Test

Write pulses are generated on the positive going edge of the clock pulse. The write generator consists of Q110 and associated circuitry.

Place a scope lead on pin 11 of U100 and a second lead on pin 8. The following wave form should be observed.

Total pulses present?

Place a scope lead on pin 12 of U100. A total of 16 write pulses should be present.

Place a scope lead on pin 13 of U100. A divide-by-two clock should be present.

Check U100.

8. Inhibit Circuit

The Inhibit Circuit is initiated only when a bad code is detected during an ACCESS attempt. The Inhibit Circuit consists of an exclusive OR gate and a dealy timer. Detection of a wrong code causes pin 4 of U106 to go high which in turn changes pin 2 to go a high state. When this happens and the nine state of U107 goes high, pin 6 of U111 goes high causing C115 to be charged to +12 volts.

To check the circuit place a wrong code into the TC811A. Place the scope lead on pin 15 of U112 and operate the controller. Pin 15 should start out high, then go low when the wrong bit is sensed by the exclusive OR gate.

9. Output Driver

The output driver circuit consists of: K100; K102; Q109; and associated circuitry. Relays K100 and K102 are transferred only when a proper code is received by the TC810.

Place a scope lead on the base of Q109. Operate TC811A with proper code. A high signal should be seen.

Go to pin 3 of U103. When state nine of U107 and a good code is compared, pin 3 should go high.

Check U107 and check U106.

10. Secure Test

The secure circuit consists of K100 and K102. Securing the unit consists of transferring the relays.

Place scope lead on anode of CR142. CR142 anode should be at ground potential.

Place the TC811 in secure position and set thumbwheels to (0000).
Push operate switch to operate position.

Place scope lead at cathode of CR133. Point should be +28 volts $\pm$ 4 volts.

Check K100 and K102.

FIGURE 9. PRINTED WIRING ASSEMBLY, MACS SWITCH

[illegible]

FIGURE 13. MULTIPLE APPLICATION CODED SWITCH AND CONTROLLER