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**Assembly Test Chip Version 01
Description and Users Manual**

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Abstract

This report describes the features and use of the Sandia National Laboratories Assembly Test Chip Ver. 01 (ATC01). This chip contains a variety of Al conductor features which are intended for use in corrosion testing. These include triple tracks with a variety of line and gap widths, ladder structures, straight line structures, and van der Pauw sheet resistance structures. The chip is square, approximately 0.250 in. on a side, with a minimum Al feature size of 1.25 μm . The various test structures on the die are described in detail and bonding layout data are given. Finally, we give an example of measurements made on ATC01 when packaged in a 40 lead Cerdip.

MASTER

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I. Introduction

Assembly Test Chip, Version 01(ATC01) is a first generation chip intended for use in monitoring integrated circuit degradation or damage during assembly and subsequent lifetime. This chip is devoted primarily to detection and measurement of the corrosion of Al conductors. In addition, the chip contains structures for detecting high voltages at bondpads which might produce electrostatic damage (ESD) and an edge damage sensor for detecting chipping and cracking produced during assembly. There are also several test structures for studying electromigration effects and a structure for monitoring the Al sheet resistance. This report is principally devoted to a description of the structures intended for use in corrosion testing. The other die structures will be discussed only briefly, as their testing and evaluation are incomplete at this time.

Development of ATC01 was initiated because test chips for corrosion testing are generally unavailable from commercial suppliers. Although many test structures have been described briefly in the literature, usually by large semiconductor manufacturers, none have been made generally available to other experimenters. A test vehicle was needed for use in qualifying non-hermetic IC packaging for use in DOE weapons applications. As a result, after a survey of the available literature, we developed a number of structures which are useful for studying the effects of corrosion in both experimental and actual lifetest studies.

A brief outline of this guide is as follows. In Section II, we review the basic details of chip fabrication. The corrosion test structures are described in detail in Section III. Other test structures are discussed briefly in Section IV. Details of the bondpad layout and test configuration information are given in Section V.

II. ATC01 Layout & Fabrication

A. Fabrication

ATC01 contains only patterned Al features on an oxide coated Si substrate. We have fabricated wafers both passivated with P-glass and unpassivated. In the fabrication process, we start with 6 in. [100] Si wafers doped with Sb. A thermal oxide(SiO_2) layer $\approx 0.5 \mu\text{m}$ thick is grown on the wafer surface, and the Al film is then deposited on the wafer.

An MTI (Machine Technologies Incorporated) sputtering system is utilized for the deposition of the Al/Si(.75%)/Cu(.5%) alloy used in Sandia's Microelectronics Development Laboratory (MDL). This system is a single wafer, cassette-loaded, cryopumped system equipped with a vacuum load-lock. Aluminum alloy is sputtered using a dc discharge with an rf bias at elevated temperatures on a rotating wafer platen. Typically, a 12 nm boron-doped silicon anti-reflection layer is then deposited to aid in photolithographic resolution and to prevent corrosion during the subsequent etch processes. The structure of the film as shown by TEM is columnar, with grains approximately 200 nm wide and 1000 nm high. Small precipitates, composed primarily of silicon, are also seen in the film.

Following Al deposition and patterning, a CAP oxide($\approx 3\%$ P doped SiO_2) $\approx 1.2 \mu\text{m}$ thick is deposited by low pressure chemical vapor deposition. This is the standard passivation or capping layer used in the MDL CMOS-V radiation hardened process.

In some cases, the wafer backside is metallized with Ti-Au for subsequent eutectic die attach. In other cases, the wafer is left uncoated for epoxy die attachment.

B. Chip Layout

A layout of the chip is shown in Fig. 1. The large black squares are all corrosion test structures with closely packed Al conductor lines of various feature size, with a minimum of $1.25 \mu\text{m}$. The structures with interior bondpads are electromigration test structures. Two parallel Al conductor lines run around the perimeter of the chip. An open circuit in either line or a line-to-line short indicates the occurrence of edge damage. The structure marked VP is a van der Pauw sheet resistance and linewidth measurement feature, while SL1 and SL2 are short straight-line corrosion detectors which utilize four terminal measurements to accurately monitor the resistance of the lines.

Fig. 1 Overall layout of ATC01. The structures with interior bondpads are for electromigration measurements. The large black structures are triple track (TT) and ladder (L) corrosion test structures with densely packed fine Al conductor lines. Starting in the lower lefthand corner and going clockwise, these structures are; TT8, TT6, TT2, TT1, L1, L2, L3, TT4, TT5, and TT3. The TT and L structures are defined in Tables I and II, respectively.

ATC01 is a square die, 0.254 in. on a side, with 0.004 in. bondpads at 0.008 in. centers. There are 88 external bondpads on the die connected to the various test structures. The connections are discussed in Section V.

III. Corrosion Test Structures

A. Triple Tracks

These are sets of three displaced serpentine Al conductors with bond pads at either end. The outer tracks can be biased at $\pm V_b$ or $+V_b$ relative to the center track, where $V_b = 10-40$ V, to accelerate corrosion. The fundamental design variables are the Al line width, w_{Al} , and the gap width, w_g . A track resistance, $R_t \geq 1$ k Ω , is used for ease in making resistance measurements. The properties which are usually measured are the line resistance and the line-to-line leakage current. The leakage current is very sensitive to the presence of ionic species, and its measurement can indicate the initiation of corrosion long before the line resistance changes appreciably. There are eight triple tracks on the die, with design parameters as listed in Table I.

Table I

Parameters used for the eight triple tracks on ATC01. The geometric parameters are defined at the bottom of the Table or in Fig. 1.

Triple Track Corrosion Test Structure Design Guide - Structures on ATC01										
* = Input Variable				Rs = 0.050 Ohm/sq.						
Design Number	w/Al (mu-m)	w/g (mu-m)	w/t (mu-m)	L (mu-m)	Z1 (mil)	Z1 (mil)	Rt (Ohm)	Area (mil^2)	Lt (mil)	N/p
1	1.25	1.25	6.25	15.00	40.00	39.51	4000.0	1162.50	29.4	50
2	2.00	2.00	10.00	24.00	40.00	39.21	4000.0	2976.01	75.9	80
3	2.00	4.00	14.00	36.00	40.00	38.90	3000.0	3348.01	86.1	61
4	4.00	4.00	20.00	48.00	70.00	68.43	2000.0	5952.01	87.0	46
5	4.00	6.00	24.00	60.00	90.00	88.11	1500.0	5580.01	63.3	27
6	6.00	4.00	26.00	60.00	90.00	87.95	1000.0	5580.01	63.4	27
8	1.25	2.00	7.75	19.50	40.00	39.39	4000.0	1511.25	38.4	50
<p>Notes-- This program is for laying out corrosion triple track test structures. The variables are:</p> <div style="display: flex; justify-content: space-between;"> <div> <p>w/Al = Aluminum line width(microns)</p> <p>w/g = Gap width(microns)</p> <p>w/t = Total width of horizontal runs, $3 \cdot w/Al + 2 \cdot w/g$(microns)</p> <p>L = Period of horizontal runs, $6 \cdot w/Al + 6 \cdot w/g$(microns)</p> <p>Z1 = Total height of triple track(mils)</p> </div> <div> <p>Z1 = height between horizontal runs, $Z1 = Z1 - 6 \cdot w/Al - 4 \cdot w/g$(mil)</p> <p>Rt = Total desired resistance(ohms)</p> <p>Area = $Z1 \cdot Lt = 3 \cdot (Rt/Rs) \cdot w/Al \cdot (w/Al + w/g)$(mil^2)</p> <p>Rs = Aluminum sheet resistance(ohm/square)</p> <p>Lt = Total track horizontal length, $Lt = (N/p) \cdot L$, where N/p = # of periods</p> <p>N/p = Number of periods in horizontal direction</p> </div> </div> <p>Resistances are nominal values based on assumed Rs value</p>										

The various geometric parameters are illustrated in Fig. 2.

Fig. 2 Schematic of triple track structure showing various geometric parameters used in the design (see Table I).

A variety of interdigitated corrosion test structures have been discussed in the literature. Edwards, Heinen, Bednarz, and Schroen[1] describe a structure with one track and a comb structure. A structure described by various authors from AT&T[2 ,3] utilizes a center track and two outer comb patterns. This structure facilitates the measurement of leakage currents but provides only one track for a continuity measurement.

Sbar and Kozakiewicz[2] also describe a triple track structure, similar to that shown in Fig. 2., which they used to make a corrosion test structure with Ti-Pd-Au thin film conductors on a hybrid circuit. Since the triple track enabled both leakage current measurements and three continuity measurements, it has evolved as the *standard* corrosion test structure over a ten-year period. However, other types of meander patterns and structures continue to be used. Fan and McPherson[4] used a two-track structure in a recent study. A similar structure was used by Padmanabhan[5] in a study of corrosion in TAB test parts.

ATC01 contains triple tracks with a number of different line and gap widths, as listed in Table I. These features facilitate the study on the dependence of corrosion rate on w_{Al} and w_g . Recent studies by Wada, Sugimoto, and Ajiki[6,7] showed a significant effect of line and gap size on corrosion rate.

The triple-track structures on ATC01 were designed with a simple Lotus 1-2-3[8] spreadsheet calculation. The * columns, or cells, in Table I represent data entry variables, while the remainder of the variables are calculated. The inputs are: aluminum linewidth, w_{Al} ; gap spacing, w_g ; Al sheet resistance, R_s ; total height of the track structure, Z_t ; and total track resistance, R_t . The spreadsheet then calculates the width of the structure, L_t , the track area, and the number of periods, N_p . For the calculations in Table I, a sheet resistance, $R_s = 0.05 \Omega/\text{sq.}$, was assumed. In our facility, the $1.0 \mu\text{m}$ Al used for *second level metal* has a nominal sheet resistance $\approx 0.035 \Omega/\text{sq.}$, while the $0.5 \mu\text{m}$ *first level metal* Al has a sheet resistance $\approx 0.07 \Omega/\text{sq.}$

B. Ladders

The ladder structure is intended for use in studying the corrosion failure time distribution function. A ladder consists of a number of Al conductor tracks connected in parallel, as shown schematically in Fig. 3. As the individual tracks open or corrode through, the ladder resistance increases in a stepwise fashion. The experimental cumulative failure distribution function can then be used to test or fit failure models.

Fig. 3 Schematic of ladder structure showing various geometric design parameters (see Table II)

ATC01 has three ladder structures with design parameters given in Table II. The initial starting resistance, R_t , is $\approx 30 \Omega$. Each ladder bus is connected to two bondpads to enable four terminal resistance measurements if high accuracy is desired. Table II shows that the number of resistors in parallel, N_R , is 20 for ladder # 1 and 10 for ladders # 2 and 3. N_R represents the resolution which can be obtained in mapping the cumulative failure distribution function. The ladder structures were also designed with a spreadsheet, and the * marked variables in Table II were used as inputs to calculate the other variables.

Table II

Ladder design parameters used for the three ladders on ATC01. The geometric parameters are defined in Fig. 2.

Ladder Test Structure Design Guide - Structures on ATC01										
* = Input Variable				Rs =	0.050	Ohm/sq.	Bus-Bar W Width =			
							20.0			
							micro-m			
Design Number	w/Al (mu-m)	w/g (mu-m)	Delta (mu-m)	N/R	L/R (mil)	Rt (Ohm)	Area (mil^2)	N/p	H/R (mil)	H/T (mil)
1	1.25	1.25	3.00	20.00	20.00	25.0	1023.6	12.0	2.5	51.2
2	2.00	2.00	4.00	10.00	40.00	50.0	1385.8	10.0	3.3	34.6
3	2.00	4.00	4.00	10.00	40.00	30.0	1259.8	6.0	3.0	31.5
<p>Notes-- This program is for laying out corrosion ladder test structures. The variables are:</p> <p>w/Al = Aluminum line width(microns) w/g = Gap width(microns) Delta = Vertical spacing between resistors N/R = Number of resistors in ladder</p> <p>L/R = Width of resistor between buss-bars Rt = Total resistance of N/R parallel resistors Area = L/R * H/T N/p = # vertical periods/resistor H/R = Vertical Height/resistor H/T = Total height of ladder</p> <p>Resistances are nominal values based on assumed Rs value Rt does not include line resist. from ladder to bondpad</p>										

C. Straight Line Corrosion Detectors

These structures are similar in concept to triple tracks but use only two straight parallel Al conductor lines. A schematic of a straight line detector is shown in Fig. 4.

There are two straight line detectors on ATC01, with parameters shown in Table III.

Fig. 4 Schematic of straight line corrosion detector showing geometric design parameters(see Table III).

Table III.

Parameters for the two straight line corrosion detectors shown in Fig. 4.

SL#	$w_{A1}(\mu m)$	$w_g(\mu m)$	$L_v(\mu m)$
1	2	2	250
2	2	4	250

The resistance of each line can be measured by a four-terminal method, and the two tracks can be biased relative to each other, if desired. The nominal line resistance of each conductor is given by,

$$R_1 = R_s L_v / w_{A1}. \quad (1)$$

With $L_v = 250 \mu m$ and $w_{A1} = 2 \mu m$, $R_1 \sim 125 R_s$. For $R_s = 0.05 \Omega/sq.$, $R_1 = 6.25 \Omega$.

The use of straight line detectors for corrosion measurements has been discussed by a number of authors. Comizzoli et al.[9] measured the change in line resistance as a function of time for parts exposed to corrosive agents in a special test cell. The restricted size of the straight line detector facilitates rapid determination of the location of a failure and aids in post-failure microscopic analysis. Bhide and Eldridge[10] used a structure similar to the ATC01 straight line detector to measure the effect of P₂O₅ concentration on the surface conductivity of phosphosilicate glass (PSG) by leakage current measurement. They also measured the track resistance as a function of time-to-study corrosion rates. Oldberg and Bozarth[11] have also used straight line structures to study Al corrosion in realistic packaging environments. Since triple tracks can be used for both leakage and resistance measurements, while simultaneously allowing positive and negative biasing, they have largely replaced the straight line detector in modern corrosion testing. The large triple tracks are also more likely to be located under a passivation pinhole, which may be a site for corrosion initiation.

IV. Other Test Structures

A. Van der Pauw & Linewidth Structure

The van der Pauw & linewidth structure, shown in Fig. 5, has two purposes. The first purpose is a measurement of the Al sheet resistance, R_s (Ω /square). This measurement aids in determining if corrosion is attacking the Al conductor surface uniformly or just acting locally at a discrete number of points in a conductor structure. Surface corrosion should produce a decrease in Al thickness, leading to an increase in R_s .

Referring to Fig. 5, the Al connections numbered 81-84 are used for the sheet resistance measurement. These numbers are the same as the corresponding pad numbers for the chip (Fig.1). The Al sheet resistance R_s , resistivity ρ , and thickness t are related by the equation,

$$R_s = \rho/t \quad (2)$$

Fig. 6 General van der Pauw sheet resistance structure.

$f(x)$ in Eq.(3) is a function of the resistance ratio, $x = R_{AB,CD}/R_{BC,DA}$, where the R functions are calculated with Eq.(4). For a symmetrical pattern, $x = 1$ and it can be shown[12] that $f(1) = 1$. This is the case for our pattern, so the sheet resistance is given by the relation,

$$R_s = 4.532 \left[\frac{V_{81} - V_{82}}{I_{84,83}} \right] . \quad (5)$$

In Eq.(5), the index numbers correspond to the pad numbers in Fig. 5 or Table IV. If desired, a possibly more accurate R_s value may be obtained by averaging the result obtained from Eq.(5) with the result obtained by interchanging current and voltage leads,

$$R_s = 4.532 \left(\frac{1}{2} \right) \left[\frac{V_{81} - V_{82}}{I_{84,83}} + \frac{V_{84} - V_{83}}{I_{81,82}} \right] . \quad (6)$$

The linewidth portion of the structure is used to evaluate how accurately the conductor patterns have been defined. The nominal linewidth is $2.0\ \mu\text{m}$ and the length of the Al line between pads 80 and 81 is $250\ \mu\text{m}$, so the linewidth resistance, R_{LW} , as defined by,

$$R_{\text{LW}} = \frac{V_{80} - V_{81}}{I_{79,83}} \quad (7)$$

can be used with the relation, $R_{\text{LW}} = (250/w_{\text{AL}})R_{\text{S}}$, to yield an experimental value for w_{AL}

$$w_{\text{AL}}(\mu\text{m}) = 250(R_{\text{S}}/R_{\text{LW}}) \quad (8)$$

B. Edge Damage Sensor

The edge damage sensor consists of two perimeter conductor lines, $5\ \mu\text{m}$ wide with a $5\ \mu\text{m}$ spacing located about $10\ \mu\text{m}$ from the chip edge. A short between the lines or an open in either line indicates the presence of edge damage. The nominal line resistance is $\approx 200R_{\text{S}}$.

C. ESD Detectors

Many ICs are sensitive to electrostatic damage. The electrostatic threat can come from the assembly operators or machinery. In measuring the ESD threat of either a complete facility or a process, it is important to have sensor structures that can indicate both the frequency and the severity of the threat. Since Electrostatic damage is most often manifest as gate oxide rupture of an MOS device, one natural detector for the threat is unprotected gate oxide, where both MOS capacitor electrodes (gate and channel) connect directly to bond pads. Such structures are designed in our third generation assembly test chip. However, the first two ATC designs did not allow for gate oxide, thus an "all aluminum" ESD detector was needed. Micro "spark gaps" have been talked about in the literature since at least 1973[13,14]. A micro spark gap is two metal spans approaching within a fraction of a mil of each other in one local area. For voltage pulses above several hundred V peak, a gap discharge occurs which usually disturbs the metal edges[15].

The design chosen for the first generation test chips consists of running metal from bond pads on adjacent chip edges. The metallizations approach each other, exposing adjacent sharp points of variable spacing, as shown in Fig. 7.

Fig. 7 Mask design for electrostatic discharge structures on ATC01. The gap widths for ESD-1 are 5, 10, and 20 μm , while for ESD-2 they are 1.0, 1.5, and 2.0 μm .

In Fig. 7, ESD-1 has gap widths of 20, 10, and 5 μm , while ESD-2 has design gap widths of 2, 1.5, and 1.0 μm . The particular spacing (as long as it is below 10 μm) does not influence the breakdown voltage, but does seem to determine the extent of tip damage achieved in a discharge. The closer spacing results in more damage. Similarly, repeated pulses result in cumulative damage. Since such damage often occurs to only about 1% of parts through a line, it is necessary to inspect many sensors for damage.

Triple tracks and ladder metallizations can also act as ESD monitors; however, the larger resistance and capacitance of these structures can supply an ameliorating time constant, as well as distribute the damage in a non-critical fashion.

V. Test Configuration

A list of all ATC01 connections is given in Table IV.

Table IV

Bondpad layout chart for ATC01. Pads are numbered clockwise, starting in the lower left hand corner, when the chip is viewed so that the writing is in the correct viewing position.

SNL Assembly Test Chip - Ver. 01
Bondpad Chart
—Pads numbered CW, start in Lower Left Corner
Chip writing upright in correct viewing position

Chip Side	Pad Number	Device	Pad Description
LHS	1	TT8	TT8 Outer Track #1
LHS	2	TT8	TT8 Center Track #1
LHS	3	TT8	TT8 Inner Track #1
LHS	4	TT8	TT8 Inner Track #2
LHS	5	TT8	TT8 Center Track #2
LHS	6	TT8	TT8 Outer Track #2
LHS	7	TT6	TT6 Outer Track #1
LHS	8	TT6	TT6 Center Track #1
LHS	9	TT6	TT6 Inner Track #1
LHS	10	TT6	TT6 Inner Track #2
LHS	11	TT6	TT6 Center Track #2
LHS	12	TT6	TT6 Outer Track #2
LHS	13	TT2	TT2 Outer Track #1
LHS	14	TT2	TT2 Center Track #1
LHS	15	TT2	TT2 Inner Track #1
LHS	16	TT2	TT2 Inner Track #2
LHS	17	TT2	TT2 Center Track #2
LHS	18	TT2	TT2 Outer Track #2
LHS	19	TT1	TT1 Outer Track #1
LHS	20	TT1	TT1 Center Track #1
LHS	21	TT1	TT1 Inner Track #1
LHS	22	TT1	TT1 Inner Track #2
LHS	23	TT1	TT1 Center Track #2
LHS	24	TT1	TT1 Outer Track #2
TOP	25	L1	L1 Current +
TOP	26	L1	L1 Voltage +
TOP	27	L1	L1 Voltage -
TOP	28	L1	L1 Current -
TOP	29	L2	L2 Current +
TOP	30	L2	L2 Voltage +
TOP	31	L2	L2 Voltage -
TOP	32	L2	L2 Current -
TOP	33	L3	L3 Current +
TOP	34	L3	L3 Voltage +
TOP	35	L3	L3 Voltage -
TOP	36	L3	L3 Current -
TOP	37	ESD-1	ESD1 +
TOP	38	ESD-2	ESD2 +
TOP	39	ESD-2	ESD2 -
TOP	40	ESD-2'	ESD2' +
TOP	41	ESD-2'	ESD2' -
TOP	42	SL-1	SL1 Track #1 Current -
TOP	43	SL-1	SL1 Track #1 Voltage -
TOP	44	SL-1	SL1 Track #1 Voltage +

Chip Side	Pad Number	Device	Pad Description
TCP	45	SL-1	SL1 Track #1 Current +
RHS	47	SL-1	SL1 Track #2 Voltage +
RHS	48	SL-1	SL1 Track #2 Voltage -
RHS	49	SL-1	SL1 Track #2 Current -
RHS	50	ESD -1'	ESD1' +
RHS	51	ESD -1'	ESD1' -
RHS	52	ESD-1	ESD1 -
RHS	53	TT4	TT4 Outer Track #1
RHS	54	TT4	TT4 Center Track #1
RHS	55	TT4	TT4 Inner Track #1
RHS	56	TT4	TT4 Inner Track #2
RHS	57	TT4	TT4 Center Track #2
RHS	58	TT4	TT4 Outer Track #2
RHS	59	TT5	TT5 Outer Track #1
RHS	60	TT5	TT5 Center Track #1
RHS	61	TT5	TT5 Inner Track #1
RHS	62	TT5	TT5 Inner Track #2
RHS	63	TT5	TT5 Center Track #2
RHS	64	TT5	TT5 Outer Track #2
RHS	65	SL-2	SL2 Track #1 Current -
RHS	66	SL-2	SL2 Track #1 Voltage -
RHS	67	SL-2	SL2 Track #1 Voltage +
RHS	68	SL-2	SL2 Track #1 Current +
RHS	69	SL-2	SL2 Track #2 Current +
BOT	70	SL-2	SL1 Track #2 Voltage +
BOT	71	SL-2	SL1 Track #2 Voltage -
BOT	72	SL-2	SL1 Track #2 Current -
BOT	73	TT3	TT3 Outer Track #1
BOT	74	TT3	TT3 Center Track #1
BOT	75	TT3	TT3 Inner Track #1
BOT	76	TT3	TT3 Inner Track #2
BOT	77	TT3	TT3 Center Track #2
BOT	78	TT3	TT3 Outer Track #2
BOT	79	VP	van der Pauw LW Cur. +
BOT	80	VP	van der Pauw LW Volt. +
BOT	81	VP	van der Pauw SR Volt. +, LW Volt. -
BOT	82	VP	van der Pauw SR Volt. -
BOT	83	VP	van der Pauw SR & LW Cur. -
BOT	84	VP	van der Pauw SR Cur. +
BOT	85	ED-In.	R+
BOT	86	Ed-Out	R+
BOT	87	ED-Out	R-
BOT	88	ED-In	R-

The bondpads are numbered clockwise, starting in the lower left corner, when the chip is viewed with the writing upright (TT2 in lower left-hand corner). In most cases, the device code corresponds to the label engraved on the chip near the associated feature. We use this table to prepare bonding instructions for package assembly. In most cases, only a few of the test structures are bonded for a particular experiment.

Table V. shows an example for a case in which the chip was packaged in a 40 lead Cerdip.

Table V

Bonding layout for tests conducted using a 40 pin Cerdip.

SNL Package Test Chip - Ver. 01	10/10/89
Bondpad Chart-40 Pin Cerdip	
—Pads numbered CW, start in Lower Left Corner	
Chip writing upright in correct viewing position	

Chip Side	Pad Number	Device	Pad Description	Bond	Pack No.	Package Instructions
LHS	1	TT8	TT8 Outer Track #1			Package 40 DIP
LHS	2	TT8	TT8 Center Track #1			
LHS	3	TT8	TT8 Inner Track #1			
LHS	4	TT8	TT8 Inner Track #2			
LHS	5	TT8	TT8 Center Track #2			Water #. 9-12
LHS	6	TT8	TT8 Outer Track #2			#Die/Pack.
LHS	7	TT6	TT6 Outer Track #1		6	
LHS	8	TT6	TT6 Center Track #1		5	
LHS	9	TT6	TT6 Inner Track #1		4	
LHS	10	TT6	TT6 Inner Track #2		3	
LHS	11	TT6	TT6 Center Track #2		2	
LHS	12	TT6	TT6 Outer Track #2		1	
LHS	13	TT2	TT2 Outer Track #1		40	
LHS	14	TT2	TT2 Center Track #1		39	
LHS	15	TT2	TT2 Inner Track #1		38	
LHS	16	TT2	TT2 Inner Track #2		37	
LHS	17	TT2	TT2 Center Track #2		36	
LHS	18	TT2	TT2 Outer Track #2		35	
LHS	19	TT1	TT1 Outer Track #1			
LHS	20	TT1	TT1 Center Track #1			
LHS	21	TT1	TT1 Inner Track #1			
LHS	22	TT1	TT1 Inner Track #2			
LHS	23	TT1	TT1 Center Track #2			
LHS	24	TT1	TT1 Outer Track #2			
TOP	25	L1	L1 Current +			
TOP	26	L1	L1 Voltage +			
TOP	27	L1	L1 Voltage -			
TOP	28	L1	L1 Current -			
TOP	29	L2	L2 Current +		34	
TOP	30	L2	L2 Voltage +		33	
TOP	31	L2	L2 Voltage -		32	
TOP	32	L2	L2 Current -		31	
TOP	33	L3	L3 Current +		30	
TOP	34	L3	L3 Voltage +		29	
TOP	35	L3	L3 Voltage -		28	
TOP	36	L3	L3 Current -		27	
TOP	37	ESD-1	ESD1 +			
TOP	38	ESD-2	ESD2 +			
TOP	39	ESD-2	ESD2 -			
TOP	40	ESD-2'	ESD2' +			
TOP	41	ESD-2'	ESD2' -			
TOP	42	SL-1	SL1 Track #1 Current -			
TOP	43	SL-1	SL1 Track #1 Voltage -			
TOP	44	SL-1	SL1 Track #1 Voltage +			

Chip Side	Pad Number	Device	Pad Description	Bond	Pack No.
TOP	45	SL-1	SL1 Track #1 Current +		
RHS	47	SL-1	SL1 Track #2 Voltage +		
RHS	48	SL-1	SL1 Track #2 Voltage -		
RHS	49	SL-1	SL1 Track #2 Current -		
RHS	50	ESD-1'	ESD1' +		
RHS	51	ESD-1'	ESD1' -		
RHS	52	ESD-1	ESD1 -		
RHS	53	TT4	TT4 Outer Track #1		26
RHS	54	TT4	TT4 Center Track #1		25
RHS	55	TT4	TT4 Inner Track #1		24
RHS	56	TT4	TT4 Inner Track #2		23
RHS	57	TT4	TT4 Center Track #2		22
RHS	58	TT4	TT4 Outer Track #2		21
RHS	59	TT5	TT5 Outer Track #1		20
RHS	60	TT5	TT5 Center Track #1		19
RHS	61	TT5	TT5 Inner Track #1		18
RHS	62	TT5	TT5 Inner Track #2		17
RHS	63	TT5	TT5 Center Track #2		16
RHS	64	TT5	TT5 Outer Track #2		15
RHS	65	SL-2	SL2 Track #1 Current -		
RHS	66	SL-2	SL2 Track #1 Voltage -		
RHS	67	SL-2	SL2 Track #1 Voltage +		
RHS	68	SL-2	SL2 Track #1 Current +		
RHS	69	SL-2	SL2 Track #2 Current +		
BOT	70	SL-2	SL1 Track #2 Voltage +		
BOT	71	SL-2	SL1 Track #2 Voltage -		
BOT	72	SL-2	SL1 Track #2 Current -		
BOT	73	TT3	TT3 Outer Track #1		
BOT	74	TT3	TT3 Center Track #1		
BOT	75	TT3	TT3 Inner Track #1		
BOT	76	TT3	TT3 Inner Track #2		
BOT	77	TT3	TT3 Center Track #2		
BOT	78	TT3	TT3 Outer Track #2		
BOT	79	VP	van der Pauw LW Cur. +		12
BOT	80	VP	van der Pauw LW Volt. +		11
BOT	81	VP	van der Pauw SR Volt. + (W V-)		10
BOT	82	VP	van der Pauw SR Volt. -		9
BOT	83	VP	van der Pauw SR & LW Cur. -		8
BOT	84	VP	van der Pauw SR Cur. +		7
BOT	85	ED-In.	R+		
BOT	86	ED-Out	R+		
BOT	87	ED-Out	R-		
BOT	88	ED-In	R-		

The structures bonded for our test were TT2, TT4, TT5, TT6, L2, L3, and VP. Table VI shows a Test & Measurement sheet prepared for this wiring arrangement.

Table VI

Measurement & test layout for the 40 pin Cerdip tests.

ATC01 - Test & Measurement					12/8/89			
40 Pin CERPDP								
Device	Chip P1	Pad #s P2	Package P1	Pad #s P2	Measurement	Input	Calculation	Description
TT6	7	12	6	1	R6->1			Outer track resistance(Ohms)
TT6	8	11	5	2	R5->2			Center track resistance(Ohms)
TT6	3	10	4	3	R4->3			Inner track resistance(Ohms)
TT6	7	8	6	5	I6->5			Outer -> center track leakage current(Amps)
TT6	8	9	5	4	I5->4			Center -> inner track leakage current(Amps)
TT2	13	18	40	35	R40->35			Outer track resistance(Ohms)
TT2	14	17	39	36	R39->36			Center track resistance(Ohms)
TT2	15	16	38	37	R38->37			Inner track resistance(Ohms)
TT2	13	14	40	39	I40->39			Outer -> center track leakage current(Amps)
TT2	14	15	39	38	I39->38			Center -> inner track leakage current(Amps)
TT4	53	58	26	21	R26->21			Outer track resistance(Ohms)
TT4	54	57	25	22	R25->22			Center track resistance(Ohms)
TT4	55	56	24	23	R24->23			Inner track resistance(Ohms)
TT4	53	54	26	25	I26->25			Outer -> center track leakage current(Amps)
TT4	54	55	25	24	I25->24			Center -> inner track leakage current(Amps)
TT5	60	64	20	15	R20->15			Outer track resistance(Ohms)
TT5	60	63	19	16	R19->16			Center track resistance(Ohms)
TT5	61	62	18	17	R61->62			Inner track resistance(Ohms)
TT5	59	60	20	19	I20->19			Outer -> center track leakage current(Amps)
TT5	60	61	19	18	I19->18			Center -> inner track leakage current(Amps)
L2	29	32	34	31	I34->31	*		Applied current(Amp)
L2	30	31	33	32	V33-V32		$(V33-V32)/(I34->31)$	Ladder resistance(Ohms)
L3	33	36	30	27	I30->27	*		Applied current(Amp)
L3	34	35	29	28	V29-V28		$(V29-V28)/(I30->27)$	Ladder resistance(Ohms)
VP	79	83	12	9	I12->9	*		LW applied current(Amp)
VP	80	81	11	10	V11-V10		$(V11-V10)/(I12->9)$	LW Resistance(Ohms)
VP	84	83	7	8	I7->8	*		SR applied current(Amp)
VP	81	82	10	9	V10-V9		$4.532 * (V10-V9)/(I7->8)$	Sh. Res.(Ohm/Sq.)

$LW(VP) = 250 * R_s(VP)/R(LW)$
 $LWVP - Nominal = 2 \mu - m$

$$LW(VP) = 250 * R_s(VP) / R(LW)$$

$$LW(VP - Nominal) = 2 \mu m$$

The measurements are currently made on a PC based system, which is still in the development stage. Some typical results from a package measurement are shown in Table VII.

Table VII.

Typical Output Data From a 40 Pin CERDIP and ATC01
Chip Prior to Environmental Testing

<u>Structure</u>	<u>Pins</u>	<u>Resistance(Ω)</u>
TT2 (outer)	40-35	2700
TT2 (center)	39-36	2699
TT2 (inner)	38-37	2698
TT4 (outer)	26-21	1295
TT4 (center)	25-22	1296
TT4 (inner)	24-23	1296
TT5 (outer)	20-15	975
TT5 (center)	19-16	975
TT5 (inner)	18-17	975
TT6 (outer)	6-1	639
TT6 (center)	5-2	640
TT6 (inner)	4-3	641
L2	force 34-31 read 33-32	34.5
L3	force 30-27 read 29-28	23.6
VPSR	force 7-8 read 10-9	0.0057
VPLW	force 12-8 read 11-10	3.39

The sheet resistance found from Eq.(5) is, $R_s = 4.532 \cdot \text{VPSR} = 0.026 \text{ } \Omega/\text{sq}$, while the line width from Eq.(8) is, $w_{A1} = 250 \cdot R_s / \text{VPLW} = 1.90 \text{ } \mu\text{m}$, which can be compared to the design linewidth of $2.00 \text{ } \mu\text{m}$.

VI. Summary

We have described a recently fabricated assembly test chip which is useful for testing encapsulants and coatings in corrosion resistance experiments. The chip employs a variety of structures, together with a selection of Al linewidths and spaces. This document is intended to serve primarily as a user's guide. We shall describe actual experimental results obtained with these chips in coatings evaluations in a future report.

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