RECEIVED J. H. MAY 20 1981

DEVELOPMENT OF PASSIVE ELECTRONIC COMPONENTS
FOR INSTRUMENTATION OF IMPROVED GEOTHERMAL
LOGGING TOOLS AND COMPONENTS

MASTER

DOE Contract No. EY-76-S-02-⁵³⁸⁶~~4881~~
A504-76 ET 28355

Final Report

to

UNITED STATES DEPARTMENT OF ENERGY
Division of Geothermal Energy

October 1978

Report No. COO/4081-4

UA Reference No.: 76-EE-65

Principal Investigator: L. S. Raymond
Co-Investigators: D. J. Hamilton
W. J. Kerwin

DISCLAIMER

This book was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

Solid State Engineering Laboratory
Department of Electrical Engineering
College of Engineering
The University of Arizona
Tucson, Arizona 85721

48B
DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

INTRODUCTION

Instrumentation of geothermal wells requires development of electronic circuits for well-logging tools; such circuits must be able to withstand environmental conditions much more severe than are encountered by conventional or military electronics. Short term objectives for well-logging instrumentation are circuits which can operate at temperatures in the range 275°C to 350°C; the medium term goal is operation up to 500°C, and the long term goal is to achieve operation at 1000°C.

The two-year project discussed in this report is generally directed toward the development of passive components for electronic circuits for geothermal well-logging tools; specifically, this involves resistors, capacitors, metallization and passivation.

It is apparent that useful electronic circuits will require the combination of both passive components and active devices. This means that the components developed in this project must be compatible with active devices both in fabrication processing and in circuit performance. Active devices under development in other projects include MOS silicon devices for short term temperatures and integrated thermionic devices for medium and long term temperatures. In order to meet the compatibility requirements, the basic technology which has been selected in this project is the chemical vapor deposition (CVD) of metal interconnections, resistor material, dielectric material and passivating material. It is to be emphasized that this is a thin-film, not thick-film, technology which is compatible with the processing methods used in fabricating either semiconductor or integrated thermionic devices, and produces components which are electrically compatible with those

devices. The investigation in this project is primarily directed toward tungsten metallization, tungsten-silicon resistors, and capacitors with silicon nitride dielectric and passivation. Since CVD can be done at temperatures in the range 500°C to 1200°C, the resulting components are capable of operating at least at short and medium term temperatures, and possibly at long term temperatures.

The devices investigated in this project are deposited on their own substrate, either sapphire or oxidized silicon. Since they are compatible with both semiconductor and integrated thermionic devices, future development (beyond the scope of this two-year project) would see them deposited on the same substrate as these devices, probably as the final steps in the fabrication process. The result would then be a monolithic integrated functional electronic block containing both active and passive components.

REACTOR MODIFICATION AND PROCESS PREPARATION

The first task in the program was the modification of the CVD reactor and the preparation of the processes for deposition of tungsten, tungsten-silicon, and silicon nitride. These modifications were completed in December 1976, and sample wafers were delivered to DOE in Washington in January 1977.

The success of fabricating high temperature passive components depends on the materials used in the various components as well as the method of deposition. Both the materials and the method of deposition used for the high temperature components are significant departures from those used in commercial thin-film components.

Chemical vapor deposition (CVD) was chosen over the standard methods of sputtering or thermal evaporation for a number of reasons. Chemical vapor deposition is a high temperature process, and allows the materials to be

Fig. 1 General Deposition System for Chemical Vapor Deposition

The reactant gases, along with a carrier gas, are introduced into a quartz reaction chamber where they react on the heated substrate surfaces to form the desired materials.

deposited at temperatures which exceed the component operating temperatures. Greater control over the process variables can be realized and material properties can be readily modified.

The general deposition process (CVD) is shown in Fig. 1 where the substrates are placed on a graphite susceptor. The susceptor is then loaded into a quartz reaction chamber and heated inductively by the RF coil that is placed around the outside of the quartz tube. A carrier gas such as hydrogen or helium is introduced into the reaction tube where it replaces all of the atmospheric gases. The susceptor is then heated until the correct deposition temperature is reached, typically 500°C to over 1000°C. One or more reactant gases are then added to the flow stream of the carrier gas. Upon reaching the heated substrate surface the gases react on the surface depositing the desired thin film of material and rejecting the by-products of the reaction back into the gas stream.

In general, the flowrate of the carrier gas is 100 to 10,000 times greater than the flowrates of the other gases. The carrier gas serves to provide correct gas environment for the reaction and also to keep the gas velocity at a reasonable rate through the reactor.

The materials selected for use in the components must be high temperature materials and stable in themselves in order to fabricate stable compounds. Film thicknesses range from 0.01 μm to >1.0 μm . The initial materials used in fabricating the resistors, capacitors, interconnects, and passivation are:

1. Tungsten
2. Tungsten-Silicon
3. Silicon Nitride

These materials are formed by the following reactions:

Tungsten

Carrier Gas: H_2

Tungsten-Silicon

Carrier Gas: H_2 or H_2 and He

Silicon Nitride

Carrier Gas: H_2 or He

The reactor was designed to be extremely flexible in terms of the process parameters and the materials that can be deposited.

The gas control panel has a total of ten rotometer type flowmeters for use with the carrier gases as well as the reactant gases. The controls for the tungsten hexafluoride (WF_6) and silane (SiH_4) are separated from the main controls for safety reasons. The flowrates of both WF_6 and SiH_4 are measured with electronic mass flowmeters. The flowrates are displayed on the front panel.

The main reaction tube is nominally 4" in diameter and the graphite susceptor is 2-1/2" x 6" which allows us to process two 2" diameter substrates at a time. The temperature range of the reactor is 400°C to >1200°C.

The majority of the reactor modifications in one way or another resulted from the use of WF_6 in the system. The reactions using WF_6 are carried out at pressures less than 200 torr. The reaction chamber and all associated lines must operate at pressures of 1×10^{-4} torr without leaking. Tungsten hexafluoride gas is extremely corrosive and toxic. The source and gas controls for the system are designed with a minimum of internal volume and only acceptable materials come into intimate contact with the gas for any extended period of time.

The major components of the system are shown in Fig. 2. The carrier along with the various reactant gases are injected into the main reaction chamber where they pass over the RF heated graphite susceptor. The carrier gas, unspent reactant gases, and by-product gases are pumped out of the main reaction chamber. The gas then enters a secondary reaction chamber which is designed with a large high temperature surface area to insure that all of the WF_6 has been reacted. The gas is cooled and passed through a large column of potassium hydroxide to remove hydrofluoric gas, which is a by-product of the reaction of WF_6 and H_2 . The final stage is a vacuum pump that provides system vacuum and exhausts the remaining gases out of the building.

Materials and Component Development

The fabrication of thin-film components requires the sequential deposition of several thin-film layers depending on the circuit and components to be fabricated. After the deposition of each layer, the substrate is removed from the reactor and a pattern is delineated into the deposited thin film by transferring a photographic image into a layer of photoresist. The film is then chemically etched.

Fig. 2 Major Internal System Components in the Modified Reactor

All of the materials used in the components must be compatible with each other at elevated temperatures, 750°C to 950°C. The diffusion of one layer into another over a long period of time at high operating temperatures is also very undesirable for high stability components. The materials originally selected for this work have the required compatibilities. These materials are typically characterized by their electrical parameters; the following section will cover materials and components together.

Substrates

The substrate on which the thin films are deposited serves strictly as a mechanical support but it must be inert to deposited materials and high temperature deposition conditions. Another important parameter is the polish of the substrate since scratches and surface deviations could cause component instability and failure.

The two substrates used to date are oxidized silicon wafers which are used in standard integrated circuits, and polished sapphire wafers. Deposition on both substrates has been successful with no apparent difference. Oxidized silicon wafers are used in current component development work.

For convenient analysis, modeling, and understanding properties of deposited tungsten, the tungsten interconnect can be considered as a low value resistor. Tungsten interconnects can also be considered as a limiting case for the W-Si resistors in which silicon concentration is reduced to zero. This is important since characteristics of tungsten metallization predictably follow our assumptions and theory for developing high temperature resistors using grain growth control. The deposition parameters that provided the initial results were carried out at pressure of ~55 Torr with a tungsten hexafluoride, WF_6 , flowrate at 2.5 cc/min in a carrier gas of hydrogen.

Films were uniform and specular after a minimum of parameter adjustment. Deposition temperature was 750°C; initial conductivity measured 7.76×10^6 ohm-cm on a sample 1250A thick. The bulk value given for tungsten is 5.5×10^{-6} ohm-cm, and the measured value was about 40% higher than bulk value. This is a very reasonable value for a film thickness of 1250A.

Additional tungsten depositions were made in order to verify the repeatability of the tungsten and to determine the temperature coefficient of resistance of tungsten. The first series of depositions was made using tungsten hexafluoride in a carrier gas of hydrogen along with a secondary carrier gas of helium to improve the uniformity of the deposition. The helium was added strictly as an inert carrier gas; however, it produced a significant increase in the resistivity of the tungsten. The temperature coefficient of the material was also modified by the utilization of helium. The second series of depositions was run with hydrogen as the only carrier gas. The total flowrate and reactor pressure were held constant for both groups.

The resistivity of the samples grown in the presence of helium ranged from 9.9×10^{-6} to 42×10^{-6} Ω -cm with the majority of the samples having a resistivity 3 to 8 times the bulk resistivity of tungsten. The temperature coefficients of resistance of bulk tungsten is ~ 4700 ppm/°C. The TCR of the samples grown in the presence of helium ranged from 1,090 to 2977 ppm/°C and the samples grown in hydrogen only ranged from 2320 to 2781 ppm/°C. It was also noted that the sample with a resistivity of 42×10^{-6} Ω -cm also had the lowest temperature coefficient of 1090 ppm/°C.

The lower temperature coefficients can be attributed to the grain size. The bulk resistivity of tungsten would be measured on a high purity tungsten sample with a relatively large grain size. The grain size of the films is severely limited by the thickness of the film which accounts for

the higher resistivities. The grain size is also varied by the deposition parameters. The utilization of helium reduces the grain size; however, this has not been analytically verified. This same phenomenon has been observed with the growth of silicon in helium in one of our previous programs. The temperature of the deposition also affects the grain size; the higher the deposition temperature, the larger the grain size will tend to be. This is demonstrated by the fact that the lowest resistivity measured, 6.47×10^{-6} , was grown in hydrogen at a temperature of 880°C. Figure 3 shows several Resistance versus Temperature plots for tungsten grown under different conditions.

RESISTOR DEVELOPMENT

The basic resistor material is grown from two gases, tungsten hexafluoride and silane. The basic reaction is

The W-Si material should be considered as a family of materials as opposed to a single compound. This is the reason for writing it as W-Si (tungsten-silicon) and not as a standard compound. The composition is variable over the complete range from 0 - 100% of either tungsten or silicon. As noted in the previous section, a resistor composed completely of tungsten (the interconnects) represents a limiting case in the W-Si family of materials.

The very large range of material composition along with being able to control the deposition parameters somewhat independently is what gives the tremendous advantage in using CVD to produce the high temperature materials.

The processing variables are much more readily available to the designer

Fig. 3 Resistivity of Tungsten as a Function of the Deposition Carrier Gas

than with either sputtering or thermal evaporation. However, with a large range of controllable variables we have an equally large task of sorting out their interdependence and how they affect the device parameters.

A matrix approach is used in mapping out the deposition parameters and the material characteristics of the tungsten-silicon family of materials.

The initial deposition conditions were as follows:

Deposition Temperature: 750°C to 780°C;

Pressure: 5.5 Torr;

Approximately a one-to-one gas concentration
ratio of WF_6 to SiH_4 .

The tungsten-silicon film was delineated with the resistor test pattern shown in Fig. 4. The temperature coefficient of resistance, TCR, was less than 100 ppm for all of the films grown under these conditions. The Resistance versus Temperature curves for three resistors are shown in Fig. 5. The best temperature coefficient was +6.1 ppm/°C. Both positive and negative TCR's were produced along with near zero TCR's.

In order to evaluate resistors with higher sheet resistance, a deposition was made with a higher silicon concentration. This yielded a sheet resistance of approximately 5000 ohms per square, approximately an order of magnitude higher than our previous depositions, and about five times higher than normal thin-film resistors exhibit. It was felt that this material would provide an opportunity to evaluate temperature cycling effects. The wafer was subjected to the temperature tests summarized in Table 1; a complete temperature cycle plot is shown in Fig. 6.

As was expected, the temperature coefficient of -533 ppm/°C for this material is larger than that obtained with lower values of sheet

Fig. 4 Resistor Test Chip with Platinum Contacts

Fig. 5 Resistance versus Temperature for Three Tungsten-Silicon Resistors. Temperature Range of Measurement: 25 to 550°C.

Table 1. TEMPERATURE CYCLING RESULTS

RESISTOR WAFER
SHEET RESISTANCE: ~5000 OHMS PER SQUARE

INITIAL RESISTANCE	1565.9 K OHMS
AFTER 10 HOURS IN AIR AT 400°C	1573.4 K OHMS
AFTER 50 CYCLES, 25°C TO 400°C, AIR	1569.0 K OHMS

1-MIL LINE WIDTH, 300 SQUARES

WAFER NUMBER : 1
RESISTOR NUMBER : 23
PATTERN : V-S1

MAXIMUM RESISTANCE = 1549500.00 OHMS
MINIMUM RESISTANCE = 1157220.00 OHMS

Fig. 6 Resistance versus Temperature Measured
After Temperature Cycling

resistance. However, it should be noted that no adverse effects were observed during and following the life testing. Life testing was also conducted on resistors, bonding pads, and ultrasonically bonded platinum wire. The test temperatures were 350°C, 425°C, and 500°C.

After 1000 hours, the ultrasonically bonded wire held up well at all three temperatures. Some of the bonds were destructively tested during the testing period. The failures generally occurred as a lifting of the bonding pad or as a break in the 0.001 inch platinum wire. From the current data it seems that the bond between the platinum wire and the platinum bonding pads will survive at temperatures up to 500°C over a long period of time.

There is, however, a problem related to the interface between the silicon dioxide passivation and the tungsten-silicon that is under the platinum bonding pads. We feel that degradation in the adherence of the W-Si to the silicon dioxide is a result of oxidation of the W-Si layer.

The degradation in the bonding pad adherences has also resulted in difficulty in the life testing of both the resistors and capacitors. On the resistors tested at 350°C and 500°C we had bonding pad failure; however, the resistors tested at 425°C showed no evidence of bonding pad failure. At 650 hours, the resistors were typically within 1% of their initial values.

Power/Temperature tests were conducted on resistors with extremely good results. In the first part of the test, the resistors were held at 20, 100, 200, 300, 400, and 500°C for a period of one hour with 0.1 watts of power being dissipated across a resistor 1.6 mils x 96 mils. There was no failure during this test. The second test consisted of holding the resistors at 500°C and then increasing the dissipated power across the resistor every hour. The dissipation levels used were 0.1, 0.2, 0.5, 0.75, 1.0, 1.5, and 2.0 watts. Failure occurred after 20 minutes at a dissipation level of

2.0 watts. The current density at this level was $\sim 3.5 \times 10^5$ amp/cm² and a power density of 2,018 watts/cm². These numbers would be considered extremely high for thin film resistors even at room temperatures.

Measurements

During 1978, additional funding was provided by DOE for the purchase of a Hewlett-Packard Data Acquisition system with 9825A calculator and plotter. A heated probe station was constructed in order to enable measurements at elevated temperatures for devices at the wafer stage. Programs have been written to automate the taking of data for resistors. Figure 6 is an example of data plotted by this system.

CAPACITOR DEVELOPMENT

High temperature capacitors were formed using CVD deposited tungsten as the plate material and CVD deposited silicon nitride as the dielectric. The capacitance, C, of a capacitor is given by

$$C = \epsilon_r \epsilon_o \frac{A}{d}$$

where ϵ_r is the relative dielectric constant, $\epsilon_o = 8.85 \times 10^{-12}$ F/m, A is the plate area, and d is the dielectric thickness.

The relative dielectric constant, ϵ_r , is a parameter of the dielectric material and is also dependent on the method of deposition. The measured relative dielectric constant is 8.6 for silicon nitride grown in a carrier gas of helium at 750°C. Figure 7 shows the capacitance as a function of temperature for three separate thicknesses. The test pattern is shown in Fig. 8. The temperature coefficient of capacitance is in a small range around -70 ppm/°C. The test area of the capacitors is 1.0 mm². There was no problem with pin holes

Fig. 7 Capacitance versus Temperature Curves for Three High Temperature Capacitors

Fig. 8. Capacitor Test Chip with Platinum Contacts

or defects in the dielectric material. The capacitors were not cycled above 350°C due to the rapid oxidation of unpassivated tungsten above 400°C.

A series of capacitors was run using hydrogen as the carrier gas; the results were extremely poor. The capacitors were very leaky, and there was a significant amount of mobile charge in the dielectric. All work on silicon nitride using hydrogen as the gas stream has been discontinued.

Two major areas of concern in the design and use of high temperature capacitors are the leakage current and the dielectric breakdown voltage. It is possible to have leakage currents through the capacitors of the same order of magnitude as the signal or larger. The leakage could affect the biasing of active devices or degrade the circuit function of a passive network.

We can model the capacitor by the following circuit:

where C is an ideal capacitor and R is the resistance through the dielectric between the two plates. A typical plot of the leakage current density and the applied voltage at constant temperatures is shown in Fig. 9. The conductivity of the silicon nitride is dependent on the temperature, the applied field, and the dielectric thickness. Figure 10 illustrates the affect of these parameters on the conductivity of Si_3N_4 .

Fig. 9 Capacitor Leakage Current as a Function of Applied Voltage and Temperature

Dielectric: Si_3N_4

Thickness: 5140 Å

WDW - 52A

Fig. 10 Conductivity versus Inverse Temperature of the Silicon Nitride Dielectric Layer

For comparison we also show in Fig. 10 a curve representing the values of σ as a function of temperature taken from Introduction to Ceramics by W. D. Kingery. Kingery did not provide further information on the dielectric thickness, applied field, or on the method of material preparation. It should be noted that our data follows the general shape of the Kingery curve. The dependence of σ on the applied field is also illustrated by the shift in the curve for low field and high field conditions.

It is to be emphasized that high leakage currents resulting from the increasing conductivity of the dielectric at high temperature will be encountered well below the field strength at which dielectric breakdown occurs. Published values for breakdown of silicon nitride at room temperature are approximately 10^7 V/cm. To avoid catastrophic failure at high temperatures, the applied field should be kept well below this value. An example will be used to illustrate how the conductivity variation affects capacitor design.

Suppose we impose the design rule that the applied field should not exceed 1×10^6 V/cm. At 600°K , the conductivity of the nitride is approximately 10^{-11} (ohm-cm) $^{-1}$, and the dielectric relaxation time ϵ/σ is 0.76 megohm-microfarads. If a capacitor is designed with 1 cm^2 area and $5000\text{\AA}$ dielectric thickness, it will have the following parameters:

$$C = 15 \times 10^{-9} \text{ F}$$

$$\text{Leakage resistance } R = 5 \times 10^6 \text{ ohms at } 600^\circ\text{K}$$

$$\text{Maximum voltage } V = 50 \text{ volts for } E = 10^6 \text{ V/cm}$$

$$\text{Leakage current at 50 volts, } 600^\circ\text{K: } I = 8 \times 10^{-6} \text{ amp.}$$

The determining factor in the design is the maximum field. For example, in a low-voltage digital circuit where the voltage will not exceed

10 V, the dielectric thickness could be reduced to 1000Å for the maximum field of 10^6 V/cm. The capacitance would then be 75×10^{-9} F, but the leakage resistance would decrease by a factor of 500 due to the dependence of σ on thickness. Moreover, from a reliability standpoint, it is desirable to keep the dielectric thickness above 2000Å.

Pinholes

In the fabrication of large-area capacitors, pinholes may become a problem, if they are produced in the dielectric material. Experience has shown that pinholes are usually attributable to defects in the photoresist, and thus occur when the dielectric pattern is delineated. If pinholes are produced during this delineation, subsequent deposition of the top electrode will cause a short in the capacitor. We have therefore developed a process modification which does not require delineation of the dielectric material. The process is implemented as follows:

1. Bottom tungsten electrodes are deposited and delineated.
2. Silicon nitride dielectric is deposited. Without removing the wafer from the reactor, tungsten is deposited. The dielectric under the top tungsten electrode is free from exposure to ambient environment, and has had no photoresist.
3. The top electrode pattern is delineated and etched. If pinholes occur at this step, they do not degrade the capacitor.
4. Silicon nitride passivation is deposited followed by silicon dioxide. The oxide layer is used as an etch mask for the nitride, as well as the passivation.
5. Contact windows are opened in the oxide.
6. The same contact windows are etched in the nitride.
7. Contacts are deposited and delineated.

This process has been used successfully to fabricate capacitors with areas as large as 1 cm^2 .

Life Tests

A major concern in the development of high-temperature passives is the device reliability. Numerous devices have been cycled from 25°C to 550°C in air without obvious degradation in performance or appearance. The short-term cycling provides immediate information for process development, but it does not show long-term failure modes and rates.

The capacitors are the most vulnerable to failure. They cover the largest amount of area, and the tungsten electrodes are readily oxidized at temperatures over 400°C .

To test the mechanical reliability of the materials at high temperatures, a series of capacitors was fabricated. The capacitors were constructed with a continuous bottom electrode across the wafer. Normally, the bottom electrode is delineated into individual electrodes for each capacitor. These capacitors were run at 350°C and 500°C in the Marshall furnace; the atmosphere in the furnace was room air.

The capacitors tested at 500°C showed a relatively high infant mortality rate during the first 48 hours; after the initial 48 hours, the failure rate decreased significantly for the remainder of the 1,000 hour life-test. The defect causing the failures has been identified, and it is related to the oxidation of the bottom electrode. The oxidation of the tungsten propagated radially outward from small defects in the passivation layer. Since the bottom electrode was continuous across the entire wafer, there was nothing to inhibit the spreading of the oxidation failure.

Figure 11 illustrates the lifting of the bottom electrode under a capacitor.

Fig. 11 Capacitor failure due to oxidation of the bottom tungsten electrode. Test temperature was 500°C.

Fifty percent of the capacitors on the wafer tested at 500°C were lost due to failure. There were no failures in the capacitors tested at 350°C for 1000 hours.

The mean time to failure for the capacitors tested at 500°C was calculated to be 1,440 hours; and by extrapolation of the high temperature data to 350°C, a mean time to failure was calculated to be 54,000 hours. It is worth noting that the MTF for the 500°C test would have been much greater if we had not included the infant failures that occurred within the first 48 hours.

INTEGRATION OF PASSIVE COMPONENTS

The processes for the fabrication of resistors, capacitors, metallization and passivation are all compatible. Figure 12 shows schematically in cross-section how integration would be accomplished. To demonstrate process compatibility, we have fabricated a third-order Butterworth low-pass active-RC filter. Figure 13 shows the circuit, and a photomicrograph of the completed 100 x 100 mil chip. Note that only passive components were integrated on the chip; the active device is not included.

While all processing was compatible, the circuit did not perform satisfactorily at high temperature due to large leakage currents in the capacitors. However, both resistors and capacitors were obtained on the same chip.

In RC active filters in general, capacitor leakage resistance variations with temperature can be expected to cause problems in performance at elevated temperatures. Accordingly, we have developed a synthesis procedure which permits degradation caused by leakage resistance to be avoided. Basically, this is a pre-distortion method in which the capacitor is shunted by

PASSIVE COMPONENT STRUCTURE
(CROSS-SECTION)

Fig. 12 Cross-Sectional View Illustrating the Integration of Components

Fig. 13 Third-Order Butterworth RC-Active Filter

a low-TCR resistor whose resistance is much lower than the lowest leakage resistance at the maximum temperature. The shunt resistance is included in the synthesis of the filter, with the result that the response characteristic is the same as would be obtained with no leakage resistance, except for a constant attenuation of several dB. The method is described in the Appendix.

Appendix

PRE-DISTORTION OF ACTIVE RC FILTERS

PRE-DISTORTION OF ACTIVE RC FILTERS

William J. Kerwin
Manoon Aramrattana
Douglas J. Hamilton

Electrical Engineering Department
The University of Arizona
Tucson, Arizona 85721

Abstract

The use of active RC networks at high temperature requires that the dissipation factor of the capacitors be taken into account. This paper presents the design procedure for various types of functions as well as specific results for single amplifier active RC structures realizing 2nd, 3rd, and 4th order Butterworth low-pass filters for various values of the capacitor dissipation factor.

Introduction

The use of active RC circuits at high temperatures increases the capacitor dissipation, thus degrading the circuit performance. Typical high temperature applications are in geothermal well logging, oil or gas well logging, nuclear reactor or turbojet engine instrumentation, etc. Of course, the active devices must also be designed for high temperature operation. Existing metal ceramic tubes (such as GE 7552) can be used up to 350-400°C, but beyond that temperature, integrated thermionic circuits must be used.¹

Pre-Distortion of the Characteristic Equation

In this work we will consider the single amplifier active RC multi-feedback equal resistor ladder structure.² Pre-distortion of an active RC structure requires the introduction of a pole displacement toward the $j\omega$ axis in an amount equal to the capacitor dissipation (which has the effect of introducing a $p + D$ term moving the poles directly away from the $j\omega$ axis by an amount equal to the dissipation factor D). This pre-distortion can thus be accomplished by substituting $p-D$ in the particular transfer function to be realized.

Since the capacitors developed for the particular applications discussed earlier are of the thin film type in which all have the same dielectric material, the ratio of capacitance to conductance is fixed, that is, they all have the same dissipation factor D .

We will consider first the Butterworth 2nd order filter shown in ideal form in Fig. 1(a) and including capacitor dissipation in Fig. 1(b). The denominator of the transfer function is $p^2 + \sqrt{2}p + 1$ and substituting $p-D$, we get

$$(p-D)^2 + \sqrt{2}(p-D) + 1 = p^2 + (\sqrt{2} - 2D)p + 1 - \sqrt{2}D + D^2 \quad (1)$$

As an example, consider $D = 0.1$, then we obtain

$$p^2 + 1.2142p + 0.8686 \quad (2)$$

If we use an amplifier gain of +2 (this has been shown to be optimum for most single amplifier positive gain structures²), we then obtain for Fig. 1(a)

$$\frac{v_o}{v_i} = T(p) = \frac{\frac{2}{C_1 C_2}}{p^2 + \frac{(2C_2 - C_1)}{C_1 C_2} p + \frac{1}{C_1 C_2}} \quad (3)$$

and equating the denominator of (3) to Eq. (2), we obtain

$$\frac{1}{C_1 C_2} = 0.8686 \quad (4)$$

$$\frac{2C_2 - C_1}{C_1 C_2} = 1.2142 \quad (5)$$

whose real and positive solutions are

$$C_1 = 0.9717F$$

$$C_2 = 1.1848F$$

Now adding a dissipation of $D = 0.1$, we obtain

$G_1 = DC_1 = 0.0972\Omega$, $G_2 = DC_2 = 0.1185\Omega$, thus $R_1 = 10.29\Omega$, and $R_2 = 8.44\Omega$ for the network of Fig. 1(b). We can, of course, verify this result by direct analysis of Fig. 1(b). This result is

*Work supported by Office of Geothermal Energy, Department of Energy, Contract #EY-76-S-02-4081.

$$\frac{v_o}{v_i} = T(p) =$$

$$\frac{2}{C_1 C_2 p^2 + (2C_2 - C_1 + 2DC_1 C_2)p + 1 - C_1 D + 2C_2 D + C_1 C_2 D^2} \quad (6)$$

where

$$D = \frac{1}{R_1 C_1} = \frac{1}{R_2 C_2}$$

and substituting $C_1 = 0.9717$, $C_2 = 1.1848$, $D = 0.1$, we obtain

$$\begin{aligned} \frac{v_o}{v_i} &= \frac{2}{1.1513p^2 + 1.6282p + 1.1513} \\ &= \frac{1.7372}{p^2 + 1.414p + 1} \end{aligned} \quad (7)$$

Of course, Eq. (6) could have been solved directly for C_1 and C_2 for various D values, but this method becomes much more difficult as we go to more complex networks.

Similarly for the 3rd order Butterworth, we use the networks shown in Fig. 2. Here we have (substituting $p-D$ for p) in the Butterworth polynomial

$$(p-D)^3 + 2(p-D)^2 + 2(p-D) + 1 \quad (8)$$

which is

$$p^3 + (2-3D)p^2 + (2-4D+3D^2)p + 1-2D+2D^2-D^3 \quad (9)$$

If, for example, the capacitor dissipation $D = 0.1$ then we obtain by substituting in Eq. (9)

$$p^3 + 1.700p^2 + 1.630p + 0.819 \quad (10)$$

The transfer function of the circuit in Fig. 2(a) is

$$\frac{v_o}{v_i} = T(p) =$$

$$\frac{\frac{K}{C_1 C_2 C_3}}{p^3 + \frac{(2C_2 C_3 + 2C_1 C_3 - C_1 C_2)p^2}{C_1 C_2 C_3} + \frac{(3C_3 - 2C_2 + C_1)p}{C_1 C_2 C_3} + \frac{1}{C_1 C_2 C_3}} \quad (11)$$

Thus equating the denominator of Eq. (11) to Eq. (10), we obtain

$$\frac{1}{C_1 C_2 C_3} = 0.819 \quad (12)$$

$$\frac{3C_3 - 2C_2 + C_1}{C_1 C_2 C_3} = 1.630 \quad (13)$$

$$\frac{2C_2 C_3 + 2C_1 C_3 - C_1 C_2}{C_1 C_2 C_3} = 1.700 \quad (14)$$

Solving the above equations and recalling that $G_1 = DC_1$, $G_2 = DC_2$, $G_3 = DC_3$, and $D = 0.1$, we obtain for the element values (R, F) of the circuit in Fig. 2(b):

$$\begin{aligned} C_1 &= 1.8562 & R_1 &= 5.39 \\ C_2 &= 0.9604 & R_2 &= 10.41 \\ C_3 &= 0.6850 & R_3 &= 14.60 \end{aligned}$$

Table 1 gives the 3rd order Butterworth results for a few values of D (values in R, F).

Table 1

D	C_1	C_2	C_3	R_1	R_2	R_3
0	1.706	0.8671	0.6761	-	-	-
0.005	1.713	0.8715	0.6767	116.75	229.49	295.55
0.010	1.720	0.8760	0.6770	58.15	114.17	147.64
0.020	1.734	0.8850	0.6780	28.84	56.51	73.70
0.050	1.778	0.9123	0.6814	11.25	21.92	29.35
0.100	1.856	0.9604	0.6850	5.39	10.41	14.60
0.200	2.038	1.0650	0.6854	2.45	4.69	7.30

Similar results can be obtained for various values of D starting with the Thomson or Chebyshev polynomials, if desired.

Lastly, we will consider the 4th order network shown in Fig. 3(a) and 3(b). Analysis of Fig. 3(a) gives the transfer function below

$$\frac{v_o}{v_i} = \frac{K/C_1 C_2 C_3 C_4}{p^4 + \frac{[2(C_1 C_2 C_4 + C_1 C_3 C_4 + C_2 C_3 C_4) - C_1 C_2 C_3] p^3}{C_1 C_2 C_3 C_4} + \frac{(C_1 C_2 - 2C_1 C_3 + 3C_1 C_4 - 2C_2 C_3 + 6C_2 C_4 + 3C_3 C_4) p^2}{C_1 C_2 C_3 C_4} + \frac{(4C_4 - 3C_3 + 2C_2 - C_1) p}{C_1 C_2 C_3 C_4} + \frac{1}{C_1 C_2 C_3 C_4}} \quad (15)$$

The pre-distorted 4th order Butterworth polynomial is

$$(p-D)^4 + 2.6131(p-D)^3 + 3.4142(p-D)^2 + 2.6131(p-D) + 1 \quad (16)$$

which is

$$p^4 + (2.6131 - 4D)p^3 + (3.4143 - 7.8393D + 6D^2)p^2 + (2.6131 - 6.8284D + 7.8393D^2 - 4D^3)p + 1 - 2.6131D + 3.4142D^2 - 2.6131D^3 + D^4 \quad (17)$$

Choosing for example, $D = 0.1$, we obtain

$$p^4 + 2.2131p^3 + 2.6983p^2 + 2.0047p + 0.7703 \quad (18)$$

Equating this polynomial to the transfer function (Eq. 15), we obtain

$$\frac{1}{C_1 C_2 C_3 C_4} = 0.7703 \quad (19)$$

$$\frac{4C_4 + 2C_2 - 3C_3 - C_1}{C_1 C_2 C_3 C_4} = 2.0047 \quad (20)$$

$$\frac{1}{C_3 C_4} + \frac{3}{C_2 C_3} + \frac{4}{C_1 C_3} + \frac{3}{C_1 C_2} - \frac{2}{C_2 C_4} - \frac{2}{C_1 C_4} = 2.6903 \quad (21)$$

$$\frac{2}{C_3} + \frac{2}{C_2} + \frac{2}{C_1} - \frac{1}{C_4} = 2.2131 \quad (22)$$

Solving these equations, we obtain (values in Ω , F)

$$\begin{aligned} C_1 &= 1.3108 & R_1 &= 7.63 \\ C_2 &= 2.4668 & R_2 &= 4.05 \\ C_3 &= 0.9212 & R_3 &= 10.86 \\ C_4 &= 0.4358 & R_4 &= 22.95 \end{aligned}$$

Analysis of Theoretical Results

These resulting 2nd, 3rd, and 4th order networks were analyzed using the SPICE program and the results are shown in Fig. 4 for $D = 0.1$. These results agree with the expected Butterworth frequency response. Note that the DC gain values are reduced as a result of the capacitor dissipation. The DC gain of the ideal network ($D=0$) is 6.02 dB.

Experimental Results

Scaling the 3rd order result for $D = 0.1$ to a cut-off frequency of 10 kHz and scaling the series resistors to values of 10k each, we obtain the circuit shown in Fig. 8. This circuit was built and tested. The measured data are shown in Fig. 6; in comparison with the SPICE program result.

Conclusions

The application of pre-distortion techniques to active RC filters allows accurate performance of the filters even though the capacitor dissipation factor may be quite high. The method is applicable to various types of functions including inverse Chebyshev and elliptic for various values of dissipation factor as well as to other active RC realizations.

If the circuit is to be used over a range of temperatures where there is a considerable variation in D over this temperature range, it may be appropriate to include fixed resistors in parallel with the capacitors to produce a D value that swamps out the internal D variations of the capacitors so as to obtain a relatively constant filter performance from, say 0°C to 500°C . If even better performance is required, the external resistor temperature coefficient might be chosen to be highly positive so as to maintain a more nearly constant D as the temperature increases.

References

1. Rowley, J. C. "Geothermal Energy Development," Physics Today, January 1977.
2. Aikens, R., and W. J. Karwin. "Single Amplifier Minimal RC, Butterworth, Thomson and Chebyshev Filters to the 6th Order," International Filter Symposium, Santa Monica, Calif., April 1972.

(a)

(b)

Fig. 1 Second Order Butterworth Circuits

(a)

(b)

Fig. 2 Third Order Butterworth Circuits

(a)

(b)

Fig. 3 Fourth Order Butterworth Circuits

Fig. 4 Frequency Response of Pre-Distorted Filters

Fig. 5 Experimental Results for Pre-Distorted Third Order Filter

SUMMARY

Both resistors and capacitors have been successful fabricated. Table 2 summarizes the parameter ranges which can be obtained. Table 3 gives the complete process sequence for resistors, Table 4 for capacitors, and Table 5 for integration of resistors and capacitors. Contact deposition and delineation for all processes is described in Table 6.

Table 2. PASSIVE COMPONENT PARAMETERS

COMPONENT	MATERIAL	RESISTIVITY OHM CM	DIELECTRIC CONSTANT	SHEET RESISTANCE OHMS/	TEMPERATURE COEFFICIENT PPM/ C
RESISTOR	TUNGSTEN- SILICON	1000×10^{-6} TO 2000×10^{-6}		50 TO 1000	$< \pm 100$
CAPACITOR	SILICON NITRIDE		8.6		$< \pm 100$
INTER- CONNECTS	TUNGSTEN	6×10^{-6}		< 1	2900
PASSI- VATION	SILICON NITRIDE OR SILICON DIOXIDE	10^8 AT 500°C	8.6 3.9		

Table 3. RESISTOR PROCESS

-
1. Clean substrates.
 2. Deposit W-Si resistive material:

Temp:	720°C
Gas Flow:	WF ₆ - 3 cc/min
	SiH ₄ - 3 cc/min
	H ₂ - 1 l/min
	He - 1 l/min
Time:	3 min
 3. Delineate resistor pattern by photoresist and etch.
 4. Strip photoresist and clean.
 5. Deposit Si₃N₄ followed by SiO₂:

Temp:	760°C
Gas Flow:	Si ₃ H ₄ - 3 cc/min
	NH ₃ - 100 cc/min
	He - 2 l/min
Time:	2 min
Rate:	300A/min
Temp:	760°C
Gas Flow:	Si ₃ H ₄ - 3 cc/min
	N ₂ O - 100 cc/min
	He - 2 l/min
Time:	5 min
Rate:	300A/min
 6. Delineate contact windows by photoresist, etch through SiO₂.
 7. Strip photoresist.
 8. Etch through Si₃N₄.
 9. Clean.
 10. Deposit and delineate contact pads.
-

Table 4. CAPACITOR PROCESS

1. Clean substrates.
2. Deposit tungsten bottom electrode:

Temp:	720°C
Gas Flow:	WF ₆ - 3 cc/min
	H ₂ - 2 l/min
Time:	4 min
Sheet Resistance:	< 1 ohm per square
3. Delineate bottom electrode with photoresist; etch.
4. Strip photoresist and clean.
5. Deposit Si₃N₄ and tungsten top electrode without removing from reactor:

<u>Dielectric</u>	
Temp:	760°C
Gas Flow:	Si ₃ N ₄ - 3 cc/min
	NH ₃ - 100 cc/min
	He - 2 l/min
Time:	15 min
Rate:	300A/min
<u>Tungsten</u>	
Same as (2) above.	
6. Delineate top electrode by photoresist and etch.
7. Strip photoresist and clean.
8. Deposit Si₃N₄ followed by SiO₂:

Temp:	760°C
Gas Flow:	Si ₃ N ₄ - 3 cc/min
	NH ₃ - 100 cc/min
	He - 2 l/min
Time:	3 min
Rate:	300A/min
Gas Flow:	SiH ₄ - 3 cc/min
	N ₂ O - 100 cc/min
	He - 2 l/min
Time:	5 min

Table 4. (Continued)

-
9. Delineate contact window by photoresist and etch SiO_2 .
 10. Strip photoresist.
 11. Etch contact window in Si_3N_4 .
 12. Deposit and delineate contacts.
-

Table 5. INTEGRATION PROCESS

-
1. Clean substrates.
 2. Deposit tungsten for bottom capacitor electrodes:

Temp:	720°C
Gas Flow:	WF ₆ - 3 cc/min
	H ₂ - 2 l/min
Time:	4 min
 3. Delineate bottom electrode pattern by photoresist and etch.
 4. Strip photoresist and clean.
 5. Deposit W-Si resistor material:

Temp:	720°C
Gas Flow:	WF ₆ - 3 cc/min
	SiH ₄ - 3 cc/min
	H ₂ - 1 l/min
	He - 1 l/min
Time:	3 min
 6. Delineate resistor pattern by photoresist and etch.
 7. Strip photoresist and clean.
 8. Deposit Si₃N₄ dielectric followed by W top electrode:

<u>Dielectric</u>	
Temp:	760°C
Gas Flow:	Si ₃ N ₄ - 3 cc/min
	NH ₃ - 100 cc/min
	He - 2 l/min
Time:	15 min
Rate:	300A/min
<u>Tungsten</u>	
Same as (2) above.	
 9. Delineate top electrode by photoresist and etch.
 10. Strip photoresist and clean.

Table 5. (Continued)

11. Deposit Si_3N_4 followed by SiO_2 :

Temp: 760°C

Gas Flow: Si_3N_4 - 3 cc/min

NH_3 - 100 cc/min

He - 2 l/min

Time: 3 min

Rate: 300Å/min

Gas Flow: SiH_4 - 3 cc/min

N_2O - 100 cc/min

He - 2 l/min

Time: 5 min

12. Delineate contact windows with photoresist and etch SiO_2 .

13. Strip photoresist.

14. Etch contact windows in Si_3N_4 .

15. Clean.

16. Deposit and delineate contacts and interconnections.

Table 6. CONTACT PROCESS

I. Platinum

1. Deposit W-Si as in resistor process.
2. Remove from reactor and immediately sputter 5000A platinum.
3. Delineate contact areas and interconnections with KTI photoresist.
4. Etch in hot aqua regia.
5. Etch W-Si.
6. Strip photoresist.

II. Aluminum

1. Evaporate aluminum.
 2. Delineate contact areas and interconnections with photoresist.
 3. Etch in phosphoric acid aluminum etch.
 4. Strip photoresist.
-