A PIPELINED IC ARCHITECTURE FOR RADON TRANSFORM COMPUTATIONS IN A MULTIPROCESSOR ARRAY

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A PIPELINED IC ARCHITECTURE FOR RADON TRANSFORM COMPUTATIONS IN A MULTIPROCESSOR ARRAY

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INTRODUCTION

The amount of data generated by CT scanners is enormous, making the reconstruction operation slow, especially for 3-D and limited-data scans requiring iterative algorithms. The Radon transform and its inverse, commonly used for CT image reconstruction from projections, are computationally burdensome for today's single-processor computer architectures. If the processing times for the forward and inverse Radon transforms were comparatively small, a large set of new CT algorithms would become feasible, especially those for 3-D and iterative tomographic image reconstructions. In addition to image reconstruction, a fast "Radon Transform Computer" could be naturally applied in other areas of multidimensional signal processing including 2-D power spectrum estimation, modeling of human perception, Hough transforms, image representation, synthetic aperture radar processing, and others. A high speed processor for this operation is likely to motivate new algorithms for general multidimensional signal processing using the Radon transform. Since commercial scanners and related hardware are not generally applicable to these problems, we need to address the problems of computer algorithms and hardware architectures for accurate, high-speed computations of the Radon transform and its inverse.

In the proposed workshop paper, we will first describe interpolation schemes useful in computation of the discrete Radon transform and backprojection and compare their errors and hardware complexities. We then will evaluate through statistical means the fixed-point number system required to accept and generate 12-bit input and output data with acceptable error using the linear interpolation scheme selected. These results set some of the requirements that must be met by our new VLSI Chip architecture. Finally we will present a new unified architecture for a single-chip processor for computing both the forward Radon transform and backprojection at high data rates.

MULTIPROCESSOR SYSTEM ARCHITECTURE

Our chip architecture is designed for use in a multiprocessor system based on the Parallel Pipelined Projection Engine (PPPE) proposed by Sanz, et al. [1]. The PPPE array of processors can efficiently implement the 2-D Radon computations for high-speed transform processing. In computing the forward transform, each processor computes the values of the Radon transform for one particular angle (an example of such a computation is shown in Figure 1). The image is passed a pixel at a time to all processors over Bus 1 in the PPPE, shown Figure 2. Each processor accepts the input pixel, determines which bins that pixel contributes to, performs the computations to update the transform values, and stores the results in local RAM. In this way, the contribution of each pixel to all the projections is computed in parallel.

The Radon transform equations implemented each clock cycle by one processor in the PPPE (for a given θ) using linear interpolation are:

Increment (x,y) in a raster-scan fashion.

Compute \( s = x \cdot \cos(\theta) + y \cdot \sin(\theta) \) and \( \text{bin} = \text{integer}(s) \)

\[
\begin{align*}
  r(\text{bin}, \theta) &= r(\text{bin}, \theta) + i(x, y)(1 - (s - \text{bin})) \\
  r(\text{bin}+1, \theta) &= r(\text{bin}+1, \theta) + i(x, y)(s - \text{bin}),
\end{align*}
\]

(1)
where \( i(x,y) \) is the pixel value at \((x,y)\) and \( r(s,\theta) \) is the forward Radon transform. The difference \( s-bin \) is the fractional distance of the projected \((x,y)\) location, \( s \), to \( \text{bin} = \text{integer}(s) \) measured along the \( s \)-axis. After the entire raster-scan image has been processed, Eqn. 1 gives the sampled Radon transform \( r(\text{bin},\theta) \). For maximum processing speed, there should be one processor per projection; otherwise multiple passes through the image must be made, with each processor computing the Radon transform values for a different angle on each pass.

For handling the backprojection, the PPPE architecture employs the same pipeline of processors. Each is preloaded with the high-pass filtered Radon transform values \( \hat{r}(\text{bin},\theta) \) for one particular projection angle. The image is reconstructed a pixel at a time - the value of each pixel is passed down the pipeline using Bus 2 in Figure 2, with each processor adding the contribution of its projection to that pixel. Using linear interpolation between adjacent bins, the equations are:

\[
\begin{align*}
  \text{Increment } (x,y) \text{ in a raster-scan fashion, compute } s \text{ and } \text{bin} \\
  i(x,y) &= i(x,y) + (1-(s-\text{bin})) \cdot \hat{r}(\text{bin},\theta) + (s-\text{bin}) \cdot \hat{r}(\text{bin+1},\theta)
\end{align*}
\]

for each projection angle \( \theta \).

It has been estimated that 64 of our VLSI chips, each clocked at 10 MHz, in the PPPE architecture could perform backprojection of 512 projections with 512 bins per projection to a 512 by 512 image in 0.21 seconds; over 300 times faster than the fastest multiprocessor system evaluated and over 3000 times faster than the fastest uni-processor system evaluated [2].

**VLSI ARCHITECTURE**

Our new unified architecture for a single-chip processor for computing both the forward Radon transform and backprojection at high data rates handles 1024 pixel by 1024 pixel images, and accepts up to 1024 projections over 180 degrees. The IC architecture is shown in Figure 3. This IC would be the key element in each of the processors in the PPPE array. It is fully pipelined, has three data paths, each five stages long. Each computation in the pipeline takes one clock cycle. Since the single on-chip multiplier is only one pipeline stage, it limits the minimum clock cycle duration to a worst case time of about 100 ns when the chip is realized using a standard 2-micron CMOS technology. Clock cycle times may be decreased by adding pipelining stages within the multiplier. The precomputed values \( \sin(\theta) \) and \( \cos(\theta) \) are sent to the VLSI processor by the host computer prior to the start of computation. Subsequently, \( s \) and \( \text{bin} \) are computed recursively since \( x \) or \( y \) in Equation 1 increment by one each clock cycle. The computed Radon transform values are stored in off-chip memory. The memory is arranged into two separate banks of RAM, one for the values for odd bin numbers and the other for even bin numbers. Each computation in the forward transform updates \( r(\text{bin}) \) and \( r(\text{bin+1}) \). Since these are always in the two separate banks of RAM, both can be accessed in one clock cycle. Likewise for the backprojection computation, each computation in the backprojection adds a value to the input pixel that is computed by linearly interpolating between the appropriate values \( r(\text{bin}) \) and \( r(\text{bin+1}) \). Again, since \( r(\text{bin}) \) and \( r(\text{bin+1}) \) are always in two separate banks of RAM, they can be accessed simultaneously in one clock cycle. Only one multiplier is required in the pipeline due to the ordering of the computations.

**IC IMPLEMENTATION**

Preliminary layouts of the data paths, excluding the single on-chip multiplier, have been completed using the LAGER data-path compiler [3]. The chip is estimated to require less than 15 square mm of die area in a 2-\( \mu \)-m CMOS process and less than 7 square mm in a 1.2-\( \mu \)-m process. Using the 1.2-\( \mu \)-m process results in roughly a 2.5 times increase in processing speed, to a 25 MHz clock rate. Each IC performs 7 arithmetic operations per clock cycle, giving estimated processing rates of 70 M operations per second in a 2-\( \mu \)-m CMOS process or 175 M ops/sec in the 1.2-\( \mu \)-m process. With 64 processors in the PPPE, the processing rates of the system would be 4.5 G ops per second in a 2-\( \mu \)-m CMOS process or 11.2 G ops/sec in the 1.2-\( \mu \)-m process. We expect the IC to be fabricated prior to the workshop, and measured performance data will be presented if available.
REFERENCES


Fig 1. The forward Radon transform computed for one angle.

Fig 2. The PPPE multiprocessor array.
Unified Architecture

Fig 3. The unified IC architecture for forward and backprojection computations.
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