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ENERGY

CONVERSION

MASTER

ADVANCED CONVERTER TECHNOLOGY

Technical Progress Report for the Period May 23, 1979—
May 22, 1980

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U. S. DEPARTMENT OF ENERGY

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Advanced Converter Technology

TECHNICAL PROGRESS REPORT

For Period May 23, 1979 through May 22, 1980

Prepared for

U. S. DEPARTMENT OF ENERGY
Project Manager D. Roesler

Under Contract DE-AC01-79ET29079

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Section 1

EXECUTIVE SUMMARY

This report describes the first year of a 36-month effort to define an advanced converter employing 1980's technology for use with advanced batteries. The effort is broken down into six major tasks as follows:

- Task 1 - Advanced System Definition
- Task 2 - Improved Logic and Controls
- Task 3 - Improved Power Circuit Subsystems
- Task 4 - Broader Operating Capability
- Task 5 - Battery Modeling
- Task 6 - Investigate Battery Converter Interface

Tasks 1 through 4 were partially completed and Task 5 was completed during the period. Work on Task 6 was not scheduled. The work performed is summarized in the following sections.

TASK 1 - ADVANCED SYSTEM DEFINITION

The Task 1 effort considered the feasibility of an advanced United Technologies Corporation fuel cell power conditioner for application with a battery source. This 10-MW converter is a two-bridge system employing a new commutation circuit with advanced control capability. Other features are the use of an auxiliary commutation circuit for surge capability, the use of pulse-width-modulation for harmonic control, and the ability to operate with one bridge inoperative.

The study examined the critical areas of the concept and produced initial estimates of its characteristics. The critical areas examined were the commutation circuit and the use of pulse-width-modulation to control harmonics. It was assumed that requirements for efficiency, dc input voltage range, and output harmonics were similar to the previous Department of Energy (DOE) and Electric Power Research Institute (EPRI) studies performed under Contract EX-76-C-01-2122 and Research Project 841-1, respectively.

The semiconductor characteristics were based on 77-mm thyristors. Manufacturers' projections for the next generation of devices were utilized for performance estimates. As the devices being tested under Task 3.1 of this program are experimental devices, the characteristics used represent the first generation of production devices.

The results of this study quantified the United Technologies Corporation (UTC) advanced converter adapted for battery operation. The concept was found to have significant cost and operational advantages over the 14-MW three-bridge, low switching frequency design considered under EPRI Project 841-1 on a short-term and

a long-term basis. Also, the characteristics of the unit when designed for 1.5 to 1 input voltage range are significantly better than a unit designed for a 1.7 to 1 input voltage range.

The benefits, excluding cost, derived from this system are:

Footprint - 40 percent reduction in footprint from the previous 14-MW design and present 9.6/4.8 demonstrator inverter.

Shipping - Can be shipped as a single 8-ft. x 29-ft. pallet (excluding the transformer) which is within standard trucking limits.

Installation - The complete system can be checked out at the factory using a factory transformer.

Rating Flexibility - The basic building block is a single bridge. For a narrow input voltage range (1.3 to 1) a two-bridge system can be designed to handle 11.5 MW.

Partial Outage - Systems designed for 1.5 to 1 dc voltage input range have 1/2 normal rating with one bridge out; 1.7 to 1 systems have somewhat lower partial rating capability.

The cost advantage was estimated by comparing the two-bridge advanced concept to the low switching frequency three-bridge concept. It was assumed that both systems would use the first generation thyristors previously discussed. On this basis, the low switching frequency system would have a 9.5-MW rating for a 1.7 to 1 input voltage range. The advanced two-bridge concept is 25 percent less expensive on a specific cost basis.

This system also has growth potential as it represents the ultimate system configuration and can be upgraded as improved devices become available without major additional development cost. Improved semiconductors can be inserted to improve efficiency, increase rating, and/or reduce cost.

The studies performed under this task show the advanced two-bridge concept to have cost and size advantages compared to the existing concept. Therefore, the program was revised to adopt the advanced concept as the baseline and emphasize its development.

TASK 2 - IMPROVED LOGIC AND CONTROLS

Task 2 provides for the design and development of control and diagnostic logic for the advanced converter. During the first contract year, a logic subsystem specification was prepared using the 14-MW three-bridge low switching frequency converter as a baseline. System requirements for sensing and control were identified in order to define the performance and operating speed of the logic approaches. Candidate logic technologies were compared against these requirements, the appropriate technologies were selected for each requirement, and a conceptual design was selected.

The features of the selected conceptual design are:

- Use of multiple microprocessors with approximately 70 percent of the hardware "off the shelf" single-board microcomputers.
- All digital design except for high-speed protection.
- Common bus used for majority of interprocessor communication with dedicated buses used where required by volume of data.
- Diagnostic system designed as an integral part of the logic.
- Optical communications between logic and converter to reduce susceptibility of logic to electromagnetic disturbances from high power circuits and lightning.

As compared to present self-commutated inverter logic, the improved control and logic subsystem has the following advantages:

- 70 percent reduction in parts.
- An order of magnitude reduction in interconnections.
- 75 percent cost reduction.
- 70 percent reduction in power consumption.
- Ability to be reprogrammed for other applications and power conditioner configurations.

TASK 3 - IMPROVED POWER CIRCUIT SUBSYSTEMS

Subtask 3.1 - Full-Scale Power Pole Development

Task 3.1 experimentally verifies the design of an advanced powerpole for a 14-MW three-bridge, low-frequency converter system operation over a 1.7 to 1 dc input voltage range. The program is being carried out in two steps. The first step is to verify the performance of the new 77-mm inverter grade thyristors and new 52-mm fast recovery diodes and their associated circuitry. The second step is to test the complete commutation circuit, including the auxiliary commutation circuit. During the first year, the initial step was successfully performed on schedule and work was initiated on the second step.

The effort performed in this first step may be summarized as follows:

- An existing full-scale development powerpole was modified to permit installation of 77-mm thyristors and 52-mm diodes.

- All film commutation capacitors were installed, and the commutation inductors were modified to give a 1.2-MW rating to the powerpole. The 1.2-MW rating was based on the voltage rating of this initial group of 77-mm thyristors.
- The power pole was tested at no-load over the design voltage range and the performance of the circuit was verified by comparison with an analytical model.

Static and dynamics tests were completed over the range from 400 to 2400 volts. No anomalies were observed during the tests.

The milestone to complete test of the 77-mm thyristors and 52-mm diodes was completed on schedule. Power pole performance testing at 2400 volts dc input was completed and 50 hours of endurance testing were completed.

The voltage waveform across the four main thyristors and their associated diodes were measured. The measurements agreed with those predicted using United's circuit analysis program.

TASK 4 - BROADER OPERATING CAPABILITY

Subtask 4.1 - VAR Generation Without a dc Source

The self-commutated converter can provide leading or lagging reactive power. This capability can be used to provide rapid response, continuously variable line voltage regulation. This capability has been investigated previously under EPRI Research Project 841-1 for the case where the energy source is connected. The effort under this task investigates the ability of the converter to perform this function during periods when the converter is not in use with the energy source.

The effort under this task consists of the design and experimental investigation of the controls required to permit VAR generation without a dc source, a recommendation of a full-scale demonstration, and an assessment of the benefits. The controls design utilized in the 4.8-MW Demonstration Inverter was modified, and the desired voltage regulation capability was demonstrated on a subscale basis in the 15-kW model system. Analytical studies verified the ability to charge the dc input filter capacitors from the utility line through the converter power stage. This latter ability eliminates the need for an auxiliary dc power supply.

To fully evaluate this concept, a demonstration of full-scale VAR only operation is necessary. Four full-scale system candidates were considered:

- The 1-MW pilot power conditioning system located at United's South Windsor Engineering Facility.
- The 4.8-MW Demonstrator power conditioning system located at the Consolidated Edison site in New York City.

- The advanced self-commutated converter which may be constructed for the Battery Energy Storage Test (BEST) Facility in New Jersey.
- The Storage Battery Electric Energy Demonstration (SBEED) converter proposed for the Wolverine and Northern Michigan rural electric cooperatives.

The concept selection was based on the following factors: demonstration ability, cost of demonstration, availability, and technology considerations. The technology consideration (the ability to demonstrate the capability with a converter technology that most closely reflects the system that will be commercially utilized) was the primary factor considered. It was concluded that the demonstration should be performed in the BEST advanced self-commutated converter system and that the voltage regulation demonstration will be low cost in hardware and manpower.

An economic assessment of this mode of operation shows that the battery converter can be of economic benefit in the "VAR only" mode of operation. The degree of benefit and the method of obtaining them is dependent on the system requirements for each user.

TASK 5 - BATTERY MODELING

A detailed knowledge of the battery-to-converter dc interface is required to design an optimized power converter. Information regarding the characteristics of advanced batteries was updated through a survey of manufacturers, and a battery modeling approach was developed that can be used in the analysis of the advanced batteries.

A survey of five advanced battery developers selected by the Department of Energy was performed to update the characteristics. These developers and their battery types are as follows:

- Argonne National Laboratory - Lithium/Metal Sulfide
- C&D Batteries - Lead Acid
- Energy Development Associates (Gulf & Western) - Zinc Chloride
- General Electric Company - Sodium/Sulfur
- Gould, Inc. - Zinc/Bromine

In general, good information on voltage versus current characteristics was obtained, but relatively little data on equivalent circuit models was available.

A literature search was performed to see if the required information on battery characteristics was available from published sources. Very little information concerning battery characteristics or general purpose battery models was obtained in a detailed review.

A preliminary battery model approach was defined, and a preliminary design for portable test equipment to obtain the data required to construct an equivalent circuit model was developed. The design is based on off-the-shelf equipment. Sufficient experimental work was performed to demonstrate the method's feasibility.

Section 2

INTRODUCTION

PROGRAM OBJECTIVES

The overall objective of this program is to define an advanced converter system employing 1980's technology in all subsystem and component areas for use in electrochemical energy storage systems. Additional experimental effort will validate elements of the advanced commutation circuitry on a full-scale breadboard basis. Improved models of battery electrical characteristics are being defined and experimental apparatus is being designed to measure these characteristics and to enable better definition of the battery-power conditioner interface. Improvement of energy-storage system performance through modification of battery converter characteristics will also be investigated.

PROGRAM APPROACH

This program was designed to define and confirm the preliminary design of an advanced converter based on circuit concepts from previous Department of Energy contracts. Efforts under this contract will also incorporate advanced semiconductors, advanced logic and controls, improved power circuit subsystems, broader systems capability, an expanded understanding of battery characteristics, and an investigation of the battery/converter interface.

During this first year of the contract, a new more advanced concept for power conditioning based on a concept defined by United for fuel cell use was evaluated. This high switching frequency concept has the potential for significantly reducing the size and cost of battery plant power conditioners. As a result, the Department of Energy authorized redirection of the program to first evaluate this new concept and then to reorient the program to adopt this concept as the primary one.

The areas of activity in each task are outlined below.

Task 1 - Advanced System Definition

In accordance with the technical direction from the Department of Energy, an evaluation of the high switching frequency converter concept for battery applications was conducted under this task.

Task 2 - Improved Logic and Controls

In order to maximize flexibility and reduce cost while increasing reliability, a system based on advanced digital computer elements is being developed. A logic subsystem specification has been prepared. A conceptual design which satisfies the requirements of this specification was selected from the alternate strategies which were identified.

Task 3 - Improved Power Circuit Subsystems

This task was broken down into three subtasks, as enumerated below:

Subtask 3.1 - Full-Scale Powerpole Development - This effort is required to verify the full-scale operation of and develop the "auxiliary commutation for surge" circuit which was verified in 1/10-scale under a previous Electric Power Research Institute (EPRI) contract. Additional work under this subtask is required to develop the use of the new 77-mm thyristors selected for use in this powerpole. During the first year of the contract, the powerpole was modified for use with the larger devices, the 77-mm inverter grade thyristor and the new 52-mm fast recovery commutation rectifier were tested and their performance was verified. In addition, an advanced all-film commutation capacitor specification was tested. Redesign of the powerpole to accomplish the addition of the auxiliary commutation circuit for surge is now underway.

Subtask 3.2 - Magnetics Investigation - The requirement for work under this task has been reduced by the new high switching frequency concept. No work was performed during the first year.

Subtask 3.3 - Inverter Bridge and Cooling Studies - This work has been postponed as a result of the selection of the high switching frequency design.

Task 4 - Broader Operating Capability

This task was broken down into four subtasks, as enumerated below:

Subtask 4.1 - VAR Operation Without a DC Source - This effort evaluated the ability of the converter system to provide leading or lagging reactive power and thus assist in voltage regulation of the utility system even while disconnected from the power generation or storage source. The potential of this capability was assessed by: (1) design and experimental investigation of controls, (2) recommendation for full-scale hardware demonstration, and (3) assessment of benefits. This task was completed during the first year of the contract.

Subtask 4.2 - Partial-Failure Operating Capability*

Subtask 4.3 - Alternative System Configurations*

Subtask 4.4 - Isolated Operation*

*Work under these subtasks was not scheduled during the first year of the program.

Task 5 - Battery Modeling

This task updates the information regarding battery characteristics (small-signal characteristics, large transient performance, protection requirements, and static charge/discharge profiles) through a manufacturer survey and develops a battery modeling approach that facilitates analysis of advanced battery systems. This analysis is used to quantify the battery characteristics which are important to the

converter design and to determine the battery characteristics important to the battery system design. This task was completed during the first year of the contract. The literature search and manufacturer survey were conducted, and the data obtained was evaluated. An approach was defined for a comprehensive battery model, and procedures for obtaining the data needed for realizing an equivalent circuit model were determined. A preliminary design of portable battery test equipment was developed, and candidate hardware was evaluated in a laboratory test.

Task 6 - Investigate Battery Converter Interface

In order to accomplish the evaluation of the high switching frequency system concept, this effort was postponed.

Section 3

TASK 1.0 ADVANCED SYSTEM DEFINITION

TASK DESCRIPTION

The Task 1.0 effort was initially intended to optimize, update, and investigate in detail the design of the 14-MW converter identified under EPRI Project 841-1 (1, 2). The work under Task 1.0 was subsequently redirected by the Department of Energy to consider the feasibility of a United proprietary concept for converter application with a battery source. This advanced concept was originally identified for Fuel Cell Power Plants and has the following features:

- Two High Switching Frequency Bridges
- New Commutation Circuit with Advanced Control
- Auxiliary Commutation for Surge
- Pulse-Width-Modulation for Harmonic Control
- Single-Bridge Operating Capability

The purpose of this study was to examine critical areas to determine feasibility and then produce a conceptual design. The critical areas to be examined are the commutation circuit and use of pulse-width-waveform modulation to reduce output harmonics.

STATUS

Analytical studies have established the feasibility of the advanced converter concept. With DOE concurrence the program was reoriented to adapt the 10-MW high-switching-frequency two-bridge design as the reference design. The work on this task is now directed towards the preliminary design of the advanced two-bridge converter.

BASIC SYSTEM CONFIGURATION

The configuration of the basic 10-MW system to be studied is shown in Figure 3-1. The output dc from the batteries is fed through two three-phase bridges, where the variable voltage dc is converted into regulated ac. In addition to regulation of the ac output, selected lower frequency harmonics are removed by use of pulse-width-modulation. The series reactors following the bridge provide the impedance between the converter and the utility line required for satisfactory controls operation. The series reactors also attenuate the higher frequency voltage harmonics. Cancellation magnetics which eliminate unwanted harmonics not eliminated in the bridge are shown as an option contingent upon the results of the study. Next, the ac is fed into an output transformer having delta and wye low voltage windings and a wye secondary. This transformer steps the output voltage up to the 13.8 kV of the utility line. Finally, a circuit breaker provides ac protection and isolation.

SYSTEM ELECTRICAL DIAGRAM OF ADVANCED CONCEPT

Figure 3-1. System Electrical Diagram of Advanced Concept

This concept has the potential for cost and footprint reduction over previous concepts because of the use of the bridge pulse-width modulation to reduce output harmonics. This reduces the number of bridges and series reactors required and minimizes the requirements for output harmonic reduction magnetics. The ability to reduce the requirement for output magnetics is contingent upon the ability to operate the bridges at higher switching frequencies than the 180 Hz used in previous designs without a significant loss in efficiency. This ability depends on improvements in commutation circuit technology and identification of appropriate pulse-width-modulated waveforms.

The new commutation circuit with improved controls is a proprietary development. Auxiliary commutation for surge is a concept which permits the commutation circuit to handle transients without incurring additional losses under normal conditions.

DESIGN CRITERIA

A summary of major design criteria used in this study is given in Table 3-1. The requirements for the design to be suitable for full-rated power output over a 1.7 to 1 voltage input range, have a minimum efficiency greater than 95 percent for either the charge or discharge portion of the cycle, and limit the maximum individual harmonic to less than 3 percent are similar to requirements in the previous Department of Energy Study (3) and the Electric Power Research Institute Study (1). Conservative device assumptions were made to assure early demonstration availability.

TABLE 3-1. DESIGN CRITERIA

-
- o Efficiency greater than 95% at full load and Voltage Range Equal to 1.7 to 1 as in Previous DOE, EPRI Studies
 - o Harmonics Meet Same Criteria
 - o Conservative Device Assumptions
-

COMMUTATION CIRCUIT ANALYSIS

Semiconductor Characteristics

The status of 77-mm thyristor development was reviewed and two semiconductor manufacturers were visited to update the projections. Table 3-2 shows the original 1977 EPRI survey projections compared with those of the first experimental devices procured under Subtask 3.1 of this contract. The main area in which these first devices did not reach the long term goals was in the area of forward voltage drop and maximum voltage drop. The third column shows the characteristics that can be expected from the next generation of 77-mm thyristors. The more conservative of the two manufacturers' estimates was used. It should be noted that these devices are short of the initial 1977 EPRI survey projections.

TABLE 3-2. STATUS OF 77-MM DEVICE DEVELOPMENT

	1977 EPRI Survey Projections	DOE Task 3.1	Characteristics Assumed For Asymmetrical Thyristors Based on Vendor Interviews
Chip Diameter (mm)	77	77	77
Forward Blocking Voltage (Volts)	3000	2400	2400
Forward Voltage Loss at 3000 Amperes (Volts)	1.3	2.1	1.8
di/dt (Amperes/ μ Sec)	800	800	500
dv/dt (Volts/ μ Sec)	500	500	500
Turn-Off Time, (μ S)	75	65	60
Availability Date	80's	Under Test	1981

The characteristics used for the main thyristor and its associated diode are given in Table 3-3. An asymmetrical thyristor gives a lower forward voltage drop for a given current than a standard thyristor. This is accomplished at the expense of reverse blocking voltage which is not "required" to be fully rated to 2400 volts because the main thyristor has a diode inverse parallel.

TABLE 3-3. PROJECTED SEMICONDUCTOR CHARACTERISTICS

-
- o MAIN THYRISTOR
 - o 77-mm WITH ASYMMETRICAL RATING
 - o 2400 VOLTS AND 1400 AMPERES AVERAGE
 - o 1.8 VOLTS FORWARD DROP AT 3000 AMPERES
 - o 60 μ S TURNOFF
 - o MAIN DIODE
 - o 52-mm WITH SOFT RECOVERY
 - o 2400 VOLTS AND 1050 AMPERES AVERAGE
 - o 2.9 VOLTS DROP AT 3000 AMPERES
-

Efficiency Calculations

The efficiency calculations were based on the foregoing estimates for the main thyristor and diodes, and the inductance and commutation losses were estimated from results of the 11-MW powerpole tests. It was assumed that the maximum allowable powerpole losses were 2.5 percent to obtain the desired 95 percent overall efficiency.

The results of these studies are shown in Figure 3-2. If powerpole losses are limited to 2.5%, the operating frequency for 1.7 to 1 dc input operating voltage ranges is limited to 420 Hz. Operation to a frequency of 660 Hz is permissible for dc voltage range ≤ 1.5 to 1.

HARMONIC REDUCTION

Approach

The 4.8-MW Fuel Cell Demonstration Inverter and the systems selected under previous Department of Energy and EPRI Contracts (1, 2, & 3) used a stepped wave approach to cancel harmonics. The inverter bridges were operated at 180 Hz to control voltage. The bridge outputs were operated phase shifted 20 electrical degrees with respect to each other. The outputs of the bridge were combined in magnetic structures to produce the stepped output voltage wave. The degree of harmonic cancellation is a function of the number of bridges. With 2 bridges, harmonics 5, 7, 17, 19, 29, 31, etc. are cancelled. As the triplen harmonics are cancelled in the three-phase bridge, the first harmonics to appear are the 11th and 13th. With three bridges, harmonics 5, 7, 11, 13, 23, 25, 29, 31, etc. are cancelled and the first harmonics to appear in the voltage output waveform are the 17th and 19th. The principal advantage of the stepped wave approach is that families of harmonics are cancelled, and those harmonics not cancelled are not increased in magnitude.

Figure 3-2. Projected Powerpole Efficiency

High-Frequency Pulse Width Modulation

The basic principles of high frequency pulse width modulation are described in Chapter 8 of Reference 4. In the classical method, the harmonics cancelled are a function of frequency and voltage control of the output may be substituted for cancellation of one harmonic. The following table illustrates the possibilities:

<u>Frequency of Operation</u>	<u>Harmonics Cancelled</u>
180 Hz	Voltage Control or 1 Harmonic Eliminated
300 Hz	Voltage Control plus 1 Harmonic Eliminated
420 Hz	Voltage Control plus 2 Harmonics Eliminated
540 Hz	Voltage Control plus 3 Harmonics Eliminated
660 Hz	Voltage Control plus 4 Harmonics Eliminated

The advantage of this system is that it minimizes the requirement for cancellation magnetics. The disadvantages are that the higher frequency operation will increase inverter bridge losses; the higher order families of harmonics are not cancelled and, in general, higher order harmonics are amplified. Higher order harmonics are attenuated by the series impedance. The minimization of the cancellation magnetics provides an efficiency improvement which tends to offset the increase in inverter bridge losses. The minimization of the cancellation magnetics also provides cost and footprint advantages.

Approach

The principal assumptions with respect to the utility interface are:

- o Maximum allowable individual voltage harmonic - 3 percent
- o Allowable total harmonics - 4 percent
- o Minimum utility short circuit capacity - 250 MVA
- o Utility impedance - inductive to 10th harmonic, then constant.

The last assumption is based on an approximation of the utility line at United Technologies' South Windsor plant as measured experimentally.

It was assumed that harmonics 5, 7, 11, and 13 could be reduced to suitable levels at the output transformer by the combination of the converter system bridge outputs without filtering. Using the classical system, this would require an operating frequency of 660 Hz as shown in Figure 3-2. However, the initial studies of commutation circuit design showed that the maximum allowable frequency for the 1.7 to 1 case of interest is 420 Hz. Therefore, the system selected for study for this case cancelled the 5, 7, 17, and 19 with magnetics and the 420 Hz switching was used in the bridge to reduce remaining harmonics and provide voltage control.

For the narrow range operation below 1.5 to 1 input dc voltage range, the harmonic cancellation transformers were eliminated and the system was operated at 660 Hz.

Results of Harmonic Reduction Studies

Preliminary 420 Hz switching patterns were identified using a UTC approach for the 1.7 to 1 dc voltage range case. These switching patterns were shown to provide acceptable voltage control and, in conjunction with the cancellation magnetics, reduce the output harmonic spectrum to essentially the specification levels. The maximum individual voltage at the utility bus is the 23rd which reaches 3.3 percent. All other individual voltage harmonics are less than 1.5 percent. While the 23rd harmonic slightly exceeds the 3.0 percent limit, it is assumed that future optimization will reduce this harmonic to an acceptable level. If such is not the case, a small filter will be provided.

The combined bridge output voltage, as it would be seen if the outputs of the two bridges were added to each other, is shown in Figures 3-3, 3-4, and 3-5 for ac input voltages of 1.27, 1.4, and 1.7 per unit, respectively. The voltage harmonics will be attenuated by the output magnetics. The resulting powerpole output currents for each of these conditions are shown in Figures 3-6, 3-7, and 3-8 for the assumed line impedance. These pole output currents are well defined, do not have any discontinuities, and have a ripple less than 10 percent.

Similar studies were performed for a 1.5 to 1 input dc voltage range system. In this case, a 660 Hz waveform was used to reduce voltage and provide voltage control, and the cancellation magnetics were eliminated. The individual voltage harmonics were found to be controlled to less than 2.0 percent at the utility bus.

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Figure 3-3. Bridge Output Voltage Waveform for Wide Voltage Range Converter
[Vdc = 1.27 Vdc (min)]

Figure 3-4. Bridge Output Voltage Waveform for Wide Voltage Range Converter
[$V_{dc} = 1.4\ V_{dc\ (min)}$]

Figure 3-5. Bridge Output Voltage Waveforms for Wide Voltage Range Converter
[$V_{dc} = 1.7\ V_{dc\ (min)}$]

Figure 3-6. Bridge Output Current Waveforms for Wide Voltage Range Converter
[$V_{dc} = 1.7\ V_{dc\ (min)}$]

Figure 3-7. Bridge Output Current Waveforms for Wide Voltage Range Converter
[$V_{dc} = 1.4\ V_{dc\ (min)}$]

Figure 3-8. Bridge Output Current Waveforms for Wide Voltage Range Converter
[$V_{dc} = 1.7 V_{dc} (\min)$]

CONCEPTUAL DESIGN

The conceptual design baseline selected was the 1.7 to 1 voltage range design. The results of the Task 5 survey and the Hittman report (5) show that a voltage range of the 1.7 to 1 magnitude is required to cover all of the advanced batteries considered. However, since three of the five advanced types can be covered with a system capable of 1.5 to 1 input dc voltage range capability, this case was also considered.

The basic circuit diagram is provided in Figure 3-1. Principal design parameters are given in Table 3-4. The description of the principal subsystems is given in Table 3-5.

Subsequent to the basic circuit design, a transient analysis of the converter powerpole was performed. This analysis indicated the waveforms correspond to previous analytical predictions and the voltage margins exceed 15 percent minimum for the 2400 volt thyristors and diodes.

Results of the preliminary electrical performance analysis are shown in Table 3-6 for full load at maximum voltage and minimum voltage. This analysis shows that efficiency is in excess of 95 percent over the entire range and is comparable to designs of the 14-MW inverter identified under EPRI Research Project 841-1 (1). Results for a 1.5 to 1 dc input voltage range are comparable.

TABLE 3-4. CONCEPTUAL DESIGN TABLE

CONVERTER SYSTEM RATING	10 MW
MINIMUM DC INPUT VOLTAGE	1760 VOLTS
MAXIMUM DC INPUT VOLTAGE	3000 VOLTS
NUMBER OF BRIDGES	2
BRIDGE AC OUTPUT VOLTAGE (L-L)	1280 VOLTS
BRIDGE AC OUTPUT CURRENT	2300 AMPERES
UTILITY LINE VOLTAGE (L-L)	13.8 kV

TABLE 3-5. DEFINITION OF PRINCIPAL SUBSYSTEMS

• BRIDGE
• MAIN THYRISTOR - 77-mm, 2400 VOLTS
• MAIN DIODE - 52-mm, 2400 VOLTS
• COMMUTATION THYRISTOR - 52-mm, 2400 VOLTS
• CLAMP DIODES - 52-mm, 2400 VOLTS
• SERIES REACTORS
• 120 μ h, 6 WITH CONSTRUCTION SIMILAR TO 4.8/9.6-MW DEMO
• HARMONIC CANCELLATION MAGNETICS
• 3 MVA EQUIVALENT - CONSTRUCTION SIMILAR TO 4.8/9.6 SUMMING TRANSFORMER (1.7 TO 1 INPUT VOLTS RANGE ONLY)
• OUTPUT TRANSFORMER
• 10 MVA, 13.8 kV L-L HIGH SIDE, 1280 V L-L LOW SIDE; WINDINGS - WYE HIGH SIDE, DELTA AND WYE LOW SIDE.

TABLE 3-6 ELECTRICAL PERFORMANCE

- SYSTEM RATING - 10 MW CHARGE AND DISCHARGE
- LOSSES

OPERATING CONDITION	FULL LOAD 1700V	FULL LOAD 3000V
BRIDGE LOSS - %	.8	2.3
MAGNETICS LOSS - %	1.2	1.3
AUXILIARY LOSS - %	<u>1.0</u>	<u>1.0</u>
TOTAL LOSS - %	3.0	4.6
CONVERTER EFFICIENCY - %	97.0	95.4

Mechanical configuration studies were performed to estimate the footprint required for the proposed system. As shown in Figure 3-9, the basic converter can be contained in a single, truck-transportable 8 x 29 ft. pallet. This is a significant advantage over the previous designs which required two 8 x 36 ft. pallets to transport the same rating. A preliminary site arrangement for the advanced converter is given in Figure 3-10. This shows a 40 percent reduction in footprint over the 9.6/4.8-MW low frequency, bridge design.

COST

A cost comparison was made of the advanced high-frequency two-bridge design with the low frequency three-bridge design. Both designs used the first generation production thyristors of this study. Table 3-7 shows that the advanced system gives a 25-30 percent cost reduction from the low frequency three-bridge design on a comparable basis.

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Figure 3-9. Conceptual Plan View of Single Pallet

Figure 3-10. Site Arrangement Advanced Converter
(9.6-MW, Three-Bridge Converter Shown for Comparison in Broken Lines)

TABLE 3-7. COST COMPARISON USING FIRST GENERATION PRODUCTION THYRISTORS

SYSTEM	LOW SWITCHING FREQUENCY 3-BRIDGE	ADVANCED HIGH SWITCHING FREQUENCY 2-BRIDGE	ADVANCED HIGH SWITCHING FREQUENCY 2-BRIDGE
RATING (MW)	9.5	10	10
INPUT VOLTAGE RANGE (V_{MAX}/V_{MIN})	1.7	1.7	1.5
RELATIVE COST REDUCTION - \$/kW BASIS	REVISED BASELINE	~25%	~30%

SUMMARY

The studies performed established the feasibility of the concept. The operation of the commutation circuit was analytically confirmed, and the ability to control harmonics in this advanced configuration was analytically confirmed.

A conceptual design study established the superior characteristics of the 10-MW two-bridge advanced conceptual design. The principle benefits are:

- Performance is equal to best previous design.
- 25 to 30% cost reduction.
- Single 8 x 29 ft. pallet is within normal shipping standards
- Maximizes degree of factory checkout.
- 40% footprint reduction.
- Can accommodate 11.5-MW for narrow input voltage range (1.3 to 1).
- Can operate with one bridge out - 1.5 to 1 and lower range designs have 1/2 rating capability, 1.7 to 1 range design has lower rating.

This system is felt to represent the ultimate system configuration. Improved semiconductors can be inserted to improve efficiency and/or increase rating and/or reduce cost.

Based on these studies, it was recommended that Task 1 and other tasks where appropriate be based on the 10-MW high-frequency two-bridge design. The DOE Project Manager concurred with this recommendation.

Section 4

TASK 2 IMPROVED LOGIC AND CONTROLS

TASK DESCRIPTION

Task 2 is the design and development of controls and diagnostics for the advanced converter. The following elements are included:

- Prepare a basic logic subsystem specification.
- Investigate logic component technologies and determine candidate technologies that are projected for use in 1980 and beyond.
- Identify several conceptual approaches in conjunction with the above investigation.
- Select an advanced logic and controls conceptual approach.
- Perform limited experimental evaluation in critical areas.
- Prepare a preliminary electrical design.

STATUS

First, a logic subsystem specification was prepared (Appendix 1). Next, the system performance requirements for sensing and control were identified in order to define the performance and operating speed of logic approaches. Candidate logic technologies were then compared against these requirements and the appropriate technology was selected for each requirement. Once the logic technologies were chosen, alternate strategies for the conceptual design were identified. Finally a conceptual design was selected.

DISCUSSION

Logic Specification

A logic subsystem specification based upon the 14-MW Baseline Converter and experience with the 1-MW pilot inverter and 4.8-MW fuel cell demonstrator inverter was prepared in a format independent of a specific hardware type or technology. This format insured subsequent selection of the most promising hardware approach.

Logic Component Technologies

In order to select the appropriate logic technologies for various logic tasks, the system performance requirements had to first be identified and then compared with hardware performance. System performance requirements are summarized below:

- (1) Sensing for protection and gating signals have the highest speed requirements and require the ability to operate at 200 kilobytes per second.

- (2) Inputs for the VAR and power regulator and control must be sampled at approximately 5000 samples per second.
- (3) The logic must complete a response to a power and VAR request in 100 milliseconds.
- (4) Control of converter current to avoid saturation of output magnetics requires a resolution of 3 microseconds.

Once the performance requirements were identified, they were compared with candidate hardware and the appropriate components were selected. The newest eight-bit microprocessors can handle the protection, analog-to-digital conversion and limited controls tasks as long as there are separate processors for each task. Sixteen-bit microcomputers are definitely equal to the task. Communication between the processors will be by way of common random access memory directed over a shared bus. High speed protection can be accomplished using monolithic analog to digital converters and sample and hold circuits controlled by the microprogram in a PROM (Programmable Read Only Memory). Low-cost signal converters are now available with greater than five microsecond sample rate.

Alternate Approaches to the Conceptual Design

Two basic approaches were identified, one (Figure 4-1) using a single-bus architecture and the other (Figure 4-2) using a multiple bus architecture. Alternate strategies, in addition to the bus architecture, were identified in the following areas:

- Bus communications protocol
 - Programmed input/output
 - Interrupt
 - Direct memory access
- Power and VAR control strategies
 - High speed analog to digital conversion, all digital control
 - Low speed analog to digital conversion, analog filtering
 - Feed forward, all digital
- Communications Hardware
 - Custom design
 - Standard bus
- Subsystem Alternate Designs
 - Redistribution of processing functions
 - Alternate hardware approaches to subsystem design.

Figure 4-1. Advanced Converter Logic Single Bus Architecture

Figure 4-2. Advanced Converter Logic Multiple Bus Architecture

Selection of Conceptual Design

A conceptual design was selected from the alternate approaches previously identified. The multiple bus approach was selected since a single bus is not capable of handling the required signal load.

General Description of Conceptual Design - The advanced logic conceptual design (Figure 4-3) uses multiple programmed microcomputers ("multiprocessor" architecture) to perform the same tasks as the 4.8-Demonstrator Logic with fewer parts and reduced interconnections. The resultant design has improved reliability, lower cost and also has greater flexibility due to the inherent programability of microcomputers and the common bus system architecture which allows for system expansion without redesign. Additional "off the shelf" single-board computers and/or computer peripheral boards can be simply plugged into a standard card rack in order to connect to the common bus.

Features of Conceptual Design - The conceptual design incorporates the following features:

- (a) Multiple microcomputer design. Approximately 70 percent of the hardware will be "off the shelf" single-board microcomputers, microcomputer peripheral boards and signal conditioners mounted in a standard chassis.
- (b) All digital design except for high speed protection. All but very high speed protection will be converted from analog to digital format, thus the machine will be almost entirely digital.
- (c) A common bus will be used for interprocessor communication. Dedicated buses will be used where the volume of data requires, for real time power and VAR control data.
- (d) Serial data links for external communication. The electrical interface for site communications, diagnostics and local control will be a standard RS-232C serial interface compatible with computer control. This approach simplifies the interface wiring and also permits direct interfacing with the utility's control system without the need for special hardware. Remote control via a telephone line will also be possible via a standard modem.
- (e) The diagnostic system will be an integral part of the logic rather than a separately designed item. This is possible because the logic's "system processor" is inherently designed to monitor the system status, thus diagnostic functions can be simply added to the system processor's software. An "intelligent communications controller" processor will convert diagnostic data from the system processor into ASCII messages to be transmitted over the serial communications link.

Figure 4-3. Selected Advanced Logic and Controls Approach

- (f) Optical communications between logic and converter. The power and VAR control data from the logic to the converter waveform generator will be via optical links to eliminate susceptibility to electromagnetic disturbances from high power circuits and lightning.
- (g) Power supplies will be switching regulator type for increased efficiency and reduced size and heat dissipation. SCR gate drive power supplies will be located in the converter bridges. The distribution of power supplies will reduce heat dissipation in the logic.

Comparison of Advanced Conceptual Design With 4.8 Demonstrator Logic - (Fuel Cell Power Plant Demonstrator being installed at Con Edison in New York City).

- Complexity

- (a) Number of Circuit Boards

The advanced logic will have 18 circuit boards compared to 59 which represents a 70 percent parts reduction.

- (b) Connections

Communication on the microcomputer based logic is via shared parallel buses on 83 pin backplane and some card edge cables for I/O, for a total of approximately 200 wires, an order of magnitude improvement.

- (c) Power Supplies

The advanced logic will require 162.44 watts at 70 percent efficiency (using switching regulated supplies) for a total power of 232 watts, a 72 percent reduction in power consumption. It will use 4 voltages rather than the 5 used by the 4.8 Demonstrator.

- Cost

In limited production this new logic will cost only 25 percent of the previous design.

- Flexibility

The 4.8 logic is a dedicated "hardwire" logic design that requires hardware modification for any new application. The advanced logic is much more flexible because:

- (a) Programmed microcomputer based designs can be modified by reprogramming.
 - (b) System processors and I/O peripherals communicate via a common bus permitting additional processing, I/O or memory capacity to be simply connected to the common bus without hardware modification.

- (c) Use of "off the shelf" single-board computers and peripherals in a standard chassis means that the additional hardware described in (b) above can be purchased and "plugged in" to a spare slot in the standard chassis.

Selection of Detailed Conceptual Design Approach

This section describes the reasons for selecting the specific approaches used in the conceptual design from the alternate approaches that were identified.

Alternate strategies had been defined for bus architecture, bus protocol, bus communications hardware, subsystem functions, and strategies for real time control of power and VARs.

Bus Architecture - An industry standard common bus for interprocessor and I/O data transfer was chosen to make a flexible design which can easily be expanded, and to simplify communications between different processors.

Dedicated buses were selected where data transfer was only between two devices and the volume of data (or repetition) was high. This approach reduces congestion on the common bus and allows parallel processing to increase system throughput.

Bus Communications (Protocol and Hardware) - The common bus will be a standard configuration for which the manufacturer has defined the protocols and also manufactures the bus arbitration hardware. The protocol basically allows any "master" processor to gain control of the bus via bus arbitration logic. When its transaction is complete, another "master" may gain control of the bus. A "slave" (which cannot control the bus) receives or transmits data by requesting an interrupt of a "master" processor. Interrupt arbitration logic controls multiple interrupt requests.

Processors using dedicated buses will communicate via I/O ports at each processor. Communication protocol will be by processor interrupts, i.e., one processor will interrupt the processor connected to its I/O port in order to send or receive data.

Strategy for Real Time Power and VAR Control - A digital implementation of closed loop control has been selected over the hybrid analog/digital approach to reduce cost and complexity. The digital implementation also has the advantage of increased capability. Digital comparison replaces many potentiometer adjustments formerly required. Digital computation replaces expensive analog multipliers. Actual power and VARs are computed from digitized current and voltage measurements. The actual computed values are compared with modified power and VAR requests (from the site control) to produce phase offset and percent fundamental data to the pole waveform microcomputers. The waveform microcomputers use these data signals to modify phase and voltage of the output waveforms. The modification of power and VAR requests to conform to equipment ratings is performed by computation of megawatt output limits based on dc source and ac line conditions.

Subsystem Functions - The logic is divided into several subsystems which perform simultaneous real-time control tasks in parallel with each other, communicating with each other via a common bus. Several possible ways to distribute the total processing requirements among the subsystems were considered and the following approaches were selected:

(a) Waveform Pattern Generation

Each pole has a dedicated single-chip microcomputer to generate the waveform pattern based on the following inputs:

(1) 60 Hz sync. pulse	(from phase locked loop)
(2) phase data	} (from system processor)
(3) % fundamental voltage data	
(4) dc unbalance data - from I/O processor via system processor	
(5) auxiliary comm. for surge and advanced commutation control status - from pole overcurrent protection hardware.	

The outputs of the pole microcomputer are logic level on/off signals communicated to gate amplifiers which increase the power levels sufficiently to drive the thyristors. The amount of processing required to generate a variable waveform pattern requires individual microcomputers for each separate pole waveform. The phase and voltage data sent to the waveform microcomputer must be preprocessed by a real time control processor (the system processor). Since pole overcurrent and dc unbalance sensing hardware are already located in the converter, the pole microcomputer performs these tasks also.

(b) System processor

The system processor is a single-board computer with hardware multiply capability that performs the following tasks:

- (1) Real Time control - Regulate AC power and VARs. Compare power and VARs (computed from measured volts and amps) to modified power and VAR requests to produce phase offset and percent fundamental data to the pole microcomputers. The modification of power and VAR requests is performed by computation of megawatt output limits based on dc source and ac line conditions.
- (2) Control system initialization, startup, shutdown by communicating status words to/from the other two master processors, and by monitoring site requests (via the communications processor) and subsystem status.
- (3) Control system diagnostic and system self test.

(c) High speed analog to digital (A/D) logic

The high speed A/D logic computes actual power and VARs for use by the system processor in real time control. The logic consists of an 8 bit processor with hardware multiply capability connected to 4 A/D converters via a multiplexer. The processor computes power and VARs every 1.3 milliseconds from two voltage and two current inputs simultaneously sampled at four times the frequency of the maximum converter harmonic.

The power and VAR computation could have been done by the system processor, but would have possibly resulted in too much processing overhead for the system processor to do all of its other tasks. When the timing requirements for the system processor are studied in detail, we may find that it also has time to do this task, in which case the high speed A/D logic need not have its own processor.

Abnormal frequency and instantaneous over-voltage protection will also be done by this processor since it inputs the line voltage waveforms and can synthesize a slowly changing waveform for comparison with the line. Under normal conditions the line voltage waveform would be in synchronism with the synthesized waveform. Any rapid change in line waveform will produce a difference between it and the synthesized waveform, which can be detected. A 60 Hz pulse synchronous to the synthesized waveform will also be produced by this processor.

(d) Sequencer and I/O processor

The sequencer and I/O processor is a single-board computer connected to digital and analog slave I/O boards via a common bus. Its functions are:

(1) Input/Output

- (a) Analog inputs
- (b) Analog outputs to the local panel meters (optional)
- (c) Digital inputs
- (d) Digital outputs to system peripherals

(2) System Sequencing

Sequences system through a start or stop based on stored program which responds to control words from the system processor and to analog and digital events which it monitors.

(3) Low Speed Protection

Checks analog and digital status against out of limit conditions stored in its memory. Upon detection of an out-of-limit status, it simultaneously:

- (a) Transmits a system interrupt.

- (b) Delivers a shutdown status word to the system processor.
- (c) Stores a shutdown data word for subsequent retrieval by system diagnostic routine. Note that this I/O processor also monitors the status of the high speed protection so that its data word also contains knowledge of hardware shutdowns/interrupts.
- (e) System communications processor

The system communication processor is a single-board computer which performs the following communications tasks:

- (1) Performs serial to parallel data translations for 4 full duplex data links to site control, local control, diagnostics and (optional) remote control. Handles all communications protocols and other communications overhead.
- (2) Stored program contains ASCII message blocks required for transmittal in response to data words sent from system processor (for diagnostics).
- (3) Repetitively monitors selected system status and transmits data on serial links.
- (4) Decodes messages from serial links into requests for system processor.

Summary

The work under this task has shown that a conceptual design using multiple programmed microcomputers can be used to replace the present generation of logic with lower cost and improved reliability as the principal benefits. The selected concept has sufficient flexibility to readily adapt to future configurations with improved commutation circuits and varying number of bridges and also to source configurations other than battery, such as solar and fuel cells.

The significant features of this new design are the use of an "off-the-shelf" single-board microcomputer, a common bus for intercommunications, an integral diagnostic system, and optical communications between the logic and the converter.

The conceptual design has a 70 percent reduction in parts, an order of magnitude reduction in connections, and a cost reduction of 75 percent in limited production over the previous design which was based on logic technology available in the mid-1970's.

Section 5

TASK 3 - IMPROVED POWER CIRCUIT SUBSYSTEM
REDUCES COST AND IMPROVES EFFICIENCY

SUBTASK 3.1 - FULL-SCALE POWERPOLE DEVELOPMENT

Task Description

This task verifies an advanced powerpole design experimentally using full-scale hardware. The design is based upon the RP841-1 14-MW three-bridge converter system (1) which operates over a 1.7 to 1 voltage range with a minimum voltage of 2200 volts. The EPRI design requires two 3000 volt, 77-mm thyristors in series which are projected for mid-1980's availability. As the present first generation 77-mm devices are rated at 2400 volts, the experimental powerpole is limited to a maximum operating voltage of 3000 volts. To meet the work statement requirement of 1.7 to 1 voltage range, the powerpole will be designed for operation from 1760 to 3000 volts. The experimental powerpole will have a 1.2-MW rating corresponding to an ~11-MW converter system rating over the design range.

The design will be determined in two steps. The first step is to test, verify and characterize the new 77-mm inverter-grade thyristor and the new 52-mm fast recovery commutation rectifier and the advanced all film commutation capacitor. This step also verifies an effective snubber circuit for the larger thyristor and rectifier.

The second phase of this task includes the addition of the auxiliary commutation circuit for surge.

The major milestone of the first phase of this task is to evaluate all the major components of the full-scale powerpole which includes dynamic operating characteristics, power description, and overall performance of the circuit.

The major milestone of the second phase is to complete the addition of an auxiliary commutation circuit for surge for a 1.7:1.0 input voltage range and to demonstrate full-load commutation and auxiliary supplemental commutation. An estimate of efficiency is performed through computer developed programs.

Status

The first phase of this subtask has been completed successfully, and the results are discussed in this report. The second phase, which includes auxiliary commutation for surge, has been initiated.

Powerpole Development

Introduction - The object of the first phase of this subtask is to modify the existing, full-scale powerpole previously developed by United (Figure 5-1) to incorporate the new components for an advanced 1.2-MW powerpole. The modified powerpole will have first generation 77-mm inverter type thyristors, 52-mm fast recovery rectifier and all-film low loss commutation capacitors. The activities performed under the first part of this subtask were:

- Checkout of the full-scale development powerpole operational logic, shutdown/start control and safety controls.
- Installation and test of the commutation thyristor presently used on the 4.8-MW Demonstrator.
- Modification of the commutation circuit to include all new film capacitors and test.
- Installation and test of the first generation 77-mm thyristor and 52-mm fast recovery rectifiers.
- Modification and test of the snubber network for two series devices per switch operation and first generation device characteristics.

Figure 5-1.
Full-Scale Development Pole

(WCN-4840)

Design Ground Rules - A design was completed for a full-scale advanced wide-voltage range converter bridge using advance converter components. The new components include 77-mm thyristors, 52-mm fast recovery rectifiers, and all-film, low loss commutation capacitors.

Each converter system, Figure 5-2, is made up of three bridges and each bridge is made up of three powerpoles. Figure 5-3 shows the schematic of the major powerpole components for the split-C circuit without the auxiliary commutation for surge circuit.

Figure 5-2. 14-MW Converter Module Block Diagram Simplified Schematic

QP ₁	→	QP ₄	-	main thyrsitor
D ₁	→	D ₄	-	main diodes
QC ₁	→	QC ₄	-	commutation thyristors
C ₁			-	input capacitor
C ₂ , C ₃			-	commutation capacitors
L ₁	→	L ₄	-	commutation inductors
S ₁	→	S ₁₂	-	voltage sharing and shaping networks

Figure 5-3. 1.2-MW Development Powerpole

A list of ground rules used in designing the powerpole follows:

- Three bridge system based on EPRI 841-1 design (1).
- Voltage range of 1.7 to 1 with a minimum of 1760 volts.
- Split-C normal commutation circuit sized to commute $1.27 \times$ nominal peak load current where the 1.27 factor is composed of the following factors:
 - ripple current
 - ac line-to-line voltage unbalance
 - low ac line voltage condition.
- Auxiliary commutation circuit for surge to commute 1.6 times the nominal peak load current. This 1.6 factor is implemented in the EPRI 841 converter design and is implemented to handle the increased load currents due to lightning strikes. This will be included in the second phase of this design.
- First Generation 77-mm thyristors
- First Generation 52-mm diode
- Modified existing full-scale powerpole mainframe to meet new design requirements.

Existing components such as an in-house wound air core inductor were modified to meet the 1.2-MW design requirements.

Powerpole Design - The basic 1.2-MW development powerpole electrical schematic is shown in Figure 5-3. The design criterion of this 1.2-MW powerpole is the same as that implemented in the Research Project 841 design (1).

The circuit components of the 1.2-MW development powerpole design are:

- Filter capacitor - 6 cans at 450 μ fd, 4000 VDC for a total of 2600 μ fd.
- Pole fuses - 590A @ 4000V.
- Power thyristor, 2400 volts @ 1500 amperes (see Figure 5-4).
- Commutation thyristor, 1500 volts, 675 amperes
- Main diode, 2400 volts @ 1050 amps.
- Commutation capacitor, 10 cans at 16.9 μ fd/can at 6000V Pk-Pk.

- Commutation Inductor - 5.9 μ h
- di/dt (series) inductor - 3.25 μ h.

WCN 6403

Figure 5-4. 77-mm Thyristor, 52-mm Thyristor

The heat sinks used in the 9.6-MW development powerpoles are being utilized in this phase of the program. There were three series thyristors in the previous design and only two are required for the 1.2-MW design because of the higher blocking voltage on the first generation 77-mm thyristors. A solid copper bus bar is used as a substitute for the third thyristor. This was implemented to facilitate the powerpole testing. New heat sinks and clamps will be tested and evaluated during the second phase of the rebuild.

Powerpole Fabrication - Fabrication during the first phase of the program was performed in several steps. The powerpole was tested and verified after each step of modifying the powerpole. This minimizes complex problems which may occur due to the changes made.

Powerpole fabrication was performed as follows:

- Gate interface boards were modified to the latest 4.8-MW demonstration design and standards. This provides better overall noise immunity which is required for the 77-mm thyristors.
- Modified the commutation circuitry to include the 52-mm Westcode commutation thyristors. These devices have better current capabilities and lower reverse recovery charge than the devices previously used. These devices were shown to be a very highly reliable device.
- Installed the 77-mm thyristors and the 52-mm rectifiers into the present heat sink arrangement and modified the snubbers for two devices in series operation instead of three.
- Changed the commutation circuit to upgrade the system for 1.2-MW pole operation. This included changing the commutation and series inductors and adding the new all polypropylene film dielectric capacitors.
- Modified the logic shutdown control to incorporate a loss of air flow shutdown sequence. This is required for unattended operation.

Testing - Testing was performed in several steps to verify the operation of the powerpole. Test procedures include operation at 400 VDC, 800 VDC, and 2400 VDC. Two general categories of testing are static and dynamic testing.

Static tests are performed with the input voltage at a set level and the gate drives de-activated. The voltage is measured across each thyristor and diode. Comparisons are then made to verify the static sharing snubber sizing. The sizing of the static sharing snubber is determined by the difference in leakage currents through any of the two series devices. If the difference were greater than 100 VDC at an input voltage of 3000V, the possibility for overvoltage on one of the devices is greatly increased in the blocking state.

Dynamic tests are conducted at the appropriate values to verify the thyristor and diode operating characteristics. Comparisons are made between all two series devices to verify the proper matching. Parameters checked are turn-on time, voltage sharing, dv/dt , di/dt , snubber design, and others. The data generated is compared to calculated values and computer analysis program results.

Performance Analysis - Powerpole performance was determined analytically by utilizing an ASTAP computer model to verify pole operation and United's design program to determine the pole's tare power losses. These results can now be compared against actual pole data. The comparisons of static sharing at 400 Vdc input are given in Table 5-1. Agreement between measured and predicted values is excellent.

TABLE 5-1. POWERPOLE PERFORMANCE ANALYTICAL VS. ACTUAL

Device	QP1	QP2	QP3	QP4	D1	D2	D3	D4	C2	C3
Measured Voltage	100.2	99.8	100.2	100.6	98.9	100.6	99.6	100.8	200.5	199.8
Predicted	100.	100.	100.	100.	100.	100.	100.	100.	200.	200.

Dynamic Testing at 800 VDC - Dynamic testing was performed at 800 VDC to assure dynamic sharing of all series thyristors and rectifier devices, and proper commutation waveforms before testing at higher voltage levels. Data taken were compared with theoretical results to determine if higher voltage testing should be initiated.

Dynamic Testing at 2400 VDC - Dynamic testing included all thyristor and diode voltages, commutation currents, and input current. These results are compared to the theoretical values. The waveforms generated by the ASTAP program utilized resistor switches for thyristors which will make some of the voltage waveforms slightly different than they actually are.

Figures 5-5 through 5-9 show both the theoretical and measured waveforms for operation at 2400 VDC. The largest difference in the thyristor and diode waveforms occurs during the initial voltage spike occurring at 5 μ sec. Studies show that this is caused by diode reverse recovery charge not taken into account in this ASTAP program. The remaining waveforms are well within the instrumentation accuracy of 5 percent.

Tare Losses - A UTC in-house developed powerpole tare loss program was modified to incorporate the 1.2-MW component characteristics to determine the tare loss distribution in the powerpole. The voltage drop-current curve and the pulse loss characteristics were put into the Fortran powerpole tare loss program. These characteristics were taken from the manufacturer's recently published data sheet on the commutation thyristor and the commutation fast-recovery rectifier. A complete data sheet on the 77-mm unit was not available when the tare loss program was executed. The 77-mm characteristics were derived from scaling the 52-mm characteristics to match data points received from the manufacturer.

The filter commutation and snubber capacitors' values and dissipation factor specified by the respective manufacturers were used in the tare loss program. The in-house wound inductors were measured using a microprocessor controlled resistance-capacitor-inductor bridge. The resistance of the power bus was measured. The component values obtained from the manufacturer or measured were implemented in both the ASTAP powerpole simulation program and the tare loss program.

Figure 5-5. 1.2-MW Pole Commutation Currents at 2400 VDC

Figure 5-6. Test Results of 1.2-MW Powerpole 77-mm Main Thyristor - QP1 (2400 Vdc)

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Figure 5-7. Test Results of 1.2-MW Powerpole
77-mm Main Thyristor - QP2 (2400 Vdc)

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Figure 5-8. Test Results of 11-MW Powerpole
77-mm Main Thyristor - QP3 (2400 Vdc)

Figure 5-9. Test Results of 11-MW Powerpole
77-mm Main Thyristor - QP4 (2400 Vdc)

The powerpole tare loss distribution is given in Table 5-2. The total losses calculated are within 10 percent of total measured tare losses.

Most of the errors between the total measured power and the calculated losses can be attributed to translation of the device characteristics from the data sheet to the computer program and the variance in each semiconductor device. There may be some differences between devices of the same type. The data sheet describing the semiconductor devices represents the characteristics of an average device. Not having the complete characteristics describing the 77-mm thyristor also attributes to this error. Smaller errors can be attributed to the tolerance in the manufacturer's components, especially the capacitors.

TABLE 5-2. COMPUTED TARE LOSSES

Semiconductors	5538 watts
Snubbers & Resistor Networks	3599
Inductors, Capacitors, and Fuses	<u>827</u>
Total Computed Losses	9464 watts
Total Measured Losses	10,440 watts

Summary

The first phase of this program demonstrated the successful application of first generation 77-mm inverter grade thyristor and the fast recovery 52-mm main diode. These power semiconductor components were designed and manufactured to United's specifications for advanced power converter designs. The powerpole voltage and current dynamic characteristics can be analytically predicted within the accuracies of the instrumentation. Figures 5-5, 5-6, 5-7, 5-8, and 5-9 show the powerpole voltage and current waveforms comparison of analytically predicted waveforms to those tested on the powerpole. The excellent prediction increases the confidence level of the advance powerpole component design.

The powerpole tare loss distribution was computed and compared to the total losses measured during powerpole testing with excellent results. There is less than 10 percent difference between the total measured and total distributed loss computed at no load. The computation of tare loss distribution in the powerpole utilizes a computer program developed in support of previous powerpole development programs. The 10 percent difference between computed and measured tare loss can be attributed to variance in the semiconductor characteristics from device to device and differences between the device characteristics and manufacturer specification sheets. In the case of the 77-mm thyristor, total device characteristic specifications were not available. The information required for the tare loss computer program uses specifications of a 52-mm thyristor scaled to match available test data.

The new all-film commutation capacitor performed to expectations. The overall temperature rise was low, the worse case being a 10°F rise above ambient temperature operating at 2400 volts. As evident by the commutation current and make-up current (Figure 5-5), the commutation circuit losses are low, partly attributed to the new all-film capacitors.

The maximum operating voltage was limited to 2400 volts on the powerpole for the first phase of the powerpole development. The limiting factors were maximum, commutation current pulse rating of the 38-mm commutation thyristor and voltage limitation and power dissipation of the main thyristor and diode snubber capacitor and resistors. These limiting factors are being eliminated in the second phase of the powerpole rebuild. A 50-mm commutation thyristor is being incorporated along with a redesign snubber network for a two series switch ensemble.

The development powerpole accumulated a total of approximately 50 hours of high voltage operation with encouraging results. The new components - all polypropylene film commutation capacitors, new fast recovery main diode, and the new 77-mm inverter grade thyristor - performed well during the first phase of the test.

Section 6

TASK 4 - BROADER OPERATING CAPABILITY

Task 4, Broader Operating Capability, evaluates the benefits to utilities of four optional features that could be included in the advanced converter design: VAR operation without a dc source, partial failure operating capability, alternative system configurations, and isolated operation capability. The effort under Task 4 is broken down into individual subtasks for each feature. Under Task 4, the benefit to utilities of each of these features is defined to determine if inclusion in the advanced converter design is to be recommended and, if it is, how it should be accomplished.

SUBTASK 4.1 - VAR OPERATION WITHOUT A DC SOURCE

Task Description

Subtask 4.1, VAR operation without a dc source is discussed in the following section; the remainder of the subtasks are scheduled later in the program.

The self-commutated converter can provide leading or lagging reactive power. During periods when the converter is not in use with the energy source, this capability can be used to provide rapid-response line voltage regulation. The effort under this subtask addresses three areas in the assessment of this potential benefit: 1) Design and experimental investigation of controls 2) Recommendation for full-scale hardware demonstration, and 3) Assessment of benefits.

Status

All of the work under Subtask 4.1 was completed during the reporting period.

Design and Experimental Investigation of Controls

Introduction - The technical feasibility of utility voltage regulation was previously demonstrated under the DOE E(49-18)-2122 program. It is desirable that voltage regulation be supplied also when the dc source is inactive so that other means will not have to be employed when the dc source is not available. In this mode, the converter losses must be supplied from the utility line, and the input filter capacitors in the converter must be charged either from the utility line or from a small auxiliary power supply. A more precise method is required to control the power associated with the losses in a stable manner. This will require modifications to the existing controls, which were designed to control the power under real power output conditions. The controls design and method of charging the input capacitors are the major technical areas to be investigated. The approach taken to complete this portion of the subtask is shown in Figure 6-1.

Figure 6-1. Approach

Basic Converter System Operation - Figure 6-2 shows the interconnection of the various blocks in the converter system. The basic function of each block is described in the following pages.

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Figure 6-2. Converter System Block Diagram

The dc source consists of an unregulated dc voltage supply. This could include either battery or fuel cell power. The dc voltage source supplies power to the converter which changes the dc power to ac power. The effective series impedance is the lumped effect of the magnetics and converter switching elements. This can be modeled as a series impedance between an effective converter voltage generator and the utility line. Power and VAR flow from the converter is accomplished by controlling the phase and magnitude of the converter voltage generator with respect to the utility line.

The self-commutated converter has the intrinsic characteristics of a voltage source similar to a conventional generator. This permits independent regulation of both real and reactive power and provides a clean interface with the utility line. This effect becomes apparent in the vector diagram of Figure 6-3.

Figure 6-3. Converter Operation Vector Diagram

The power and VAR regulator controls the converter's phase and voltage magnitude so the converter will deliver the demanded power and VAR levels. The two remaining blocks in Figure 6-2 are the power and VAR foldback circuitry. These two blocks are used to condition the power and VAR demand signals so the kVA rating and voltage control limits of the converter are not exceeded. The operations of these functions are widely adjustable to ensure compatibility with different dc power sources. Under normal converter operation, these blocks are transparent and need not be considered in the system response.

Effect of Granularity in Controls - The converter's power and VAR controls are digital in nature. The digital implementation of these controls results in an inherent granularity in the controller's output. If a converter is to operate in a VAR only mode, without a source of dc power, the converter must derive its tare losses from the utility line. Since this mode of operation will require the converter to accurately draw small amounts of power from the utility line, the effect of the granularity in the converter controls must be investigated.

The converter phase controls are primarily responsible for regulating the flow of real power to and from the converter. This circuitry controls the phase of the converter voltage with respect to the utility line. The controller uses an eight-bit representation to control phase between -15° and $+15^\circ$ referenced to the utility line voltage. This produces a granularity in the phase controller output as follows:

$$\frac{+15^\circ - (-15^\circ)}{2^8} = 0.117^\circ$$

Determination of the acceptability of this granularity will require analysis at the converter's worst case operating point. This is the point at which the flow of real power, to or from the converter, is most affected by the converter phase angle. From the fact that we are primarily interested in operating points around zero real power, VAR only, and from reinspection of the vector diagram in Figure 6-3, this operating point occurs when the converter voltage is greatest in magnitude. This corresponds to the operating point at which the converter is supplying full leading VARs to the utility system. Analysis of the granularity in the 15-kW model system follows.

The utility line voltage for the 15-kW converter is 288 Vrms measured line to neutral. The converter's output impedance consists of an 8.48 mH inductance and a 1.72 Ω resistance. At the operating point at which the converter is supplying full leading VARs, the converter output impedance, the voltage across this impedance and the converter output current are related by Ohm's law as follows.

$$\frac{\Delta V}{Z} = I = \frac{\text{Full VAR}/3}{V_{\text{Line}}} \quad /90^\circ \text{ per phase}$$

Substituting values for the 15-kW system and solving for the required ΔV yields

$$\Delta V = \frac{15 \times 10^3 / 3}{288} \quad /90^\circ \quad [1.72 + j2\pi 60 \cdot 8.48 \times 10^{-3}] = 63.02 \quad /151.72^\circ$$

At this operating point, the converter voltage is the sum of the required ΔV and the utility line voltage.

$$V_{\text{conv}} = V_{\text{line}} + \Delta V = 288 \quad /0^\circ + 63.02 \quad /151.72^\circ = 234.4 \quad /7.318^\circ$$

A power flow error results from the rotation of the converter voltage vector by the minimum granularity of the phase controller.

Rotating the vector and solving for the new " ΔV " across the converter output impedance yields the following

$$\Delta V' = V_{\text{conv}} - V_{\text{line}}$$

$$\Delta V' = 234.4 \quad /7.318^\circ - 288 \quad /0^\circ = 62.75 \quad /152.1^\circ$$

Solving for the resulting current flow through the converter output impedance yields

$$I' = \frac{\Delta V'}{Z} = \frac{62.75 \quad /152.1^\circ}{[1.72 + j2\pi 60 \cdot 8.48 \times 10^{-3}]} = 17.29 \quad /90.4^\circ$$

On a three-phase basis this corresponds to a reactive power output of 14.94 KVARs and real power input of -104 watts. This real power drawn from the utility line will tend to charge the dc filter and raise the dc voltage. The dc filter on the 15-kW model system consists of an 8.25×10^{-2} F capacitor bank. Assume that this minimum power error is maintained for one 60-HZ cycle. If the dc voltage does not change drastically during this period, the dc current will be

$$I_{dc} = \frac{P}{V_{dc}} = \frac{104}{150} = 0.693A$$

where

P = power error due to phase granularity

V_{dc} = nominal dc voltage

I_{dc} = dc current

The resulting voltage error in the dc filter would be

$$V = \frac{1}{C} \int_{t_0}^t I_{dc} dt = \frac{1}{8.25 \times 10^{-2}} \int_{t_0}^t 0.693 dt = 0.134V$$

where

V = dc voltage error

C = input filter capacitance

I_{dc} = dc current

Since the dc voltage range for the 15-kW model system is from 130 Vdc to 180 Vdc, the voltage error due to the phase controller granularity represents only 0.2% of the total dc voltage range. Thus it appears that the granularity of phase control in the system should present no problem.

A similar investigation was performed of the phase controller granularity in a full-scale, 14-MW converter system. It showed the resulting dc voltage change would be 22.6 volts. The dc voltage range for the 14-MW converter is from 2200 V to 3700 V, and the voltage change due to the phase granularity only represents 1.5 percent of this range. This voltage deviation should prove no problem.

Operation Without dc Source (15 kW) - Design of a stable method of dc voltage control with no dc source present was accomplished by utilizing the converter response model developed in RP841-1 Task 4 and reported in Reference 1. The model is comprised of four major subsystems which govern the total system dynamics: the

dc source and filter, the voltage controller, the phase controller, and the output power train. To facilitate controls development, this model has been simplified to include only those blocks which directly affect real power flow. The simplified model which has been linearized about a zero real power operating point is shown in Figure 6-4. The additional controls necessary to regulate dc voltage are shown in the figure as an identified block labeled "additional controls".

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Figure 6-4. Simplified 15-kW Power Controls Model

The additional controls take an error in the dc bus voltage and use it to correct the converter input power level. The required additional controls in Figure 6-4 were determined by application of the root-locus method to the simplified model. The root-locus method provides an easy-to-use graphical method of predicting closed-loop transient response of control systems. In designing a linear control system, the root-locus method proves quite useful since it suggests the manner in which the system transfer function should be modified so that the response meets system performance specifications. Repeated application of the root-locus method yielded an acceptable method of dc voltage control for the 15-kW model system. Figure 6-5 shows the resulting root-locus diagram and required additional controls.

Since the additional controls necessary for dc voltage control were developed from a simplified linearized model, it was necessary to test them on the ASTAP* computer model used for RP-841 Task 4 (1). This computer model included the granularity of the converter controls as well as the tare losses in the converter. Since the computer model yielded an acceptable system response, the additional controls developed were implemented in hardware on the 15-kW model system. The hardware tests proved to be very stable, and the machine's normal VAR capability was not substantially affected. Figure 6-6 shows the results of a VAR step in both the computer model (A) and the actual hardware (B). There is good agreement between the computer model and the actual hardware.

6-8.

Figure 6-6A. 15-kW Model System Experimental Results

Figure 6-6B. 15-kW Computer Simulation.

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Operation Without dc Source (14 MW) - Stable operation without a dc source was accomplished for the 14-MW converter system by starting with the converter response model developed for EPRI in RP841-1 Task 4. To facilitate controls development, this model was simplified to include only those blocks which directly affect real power flow. Repeated application of the root-locus method failed to result in a satisfactory method of dc voltage control. The best results obtained used a constant gain feedback and required the elimination of the input integrator to the phase controller. This method of control proved inadequate, since the feedback gain required for system stability was insufficient to provide the required steady-state accuracy of the dc voltage. The lower accuracy of the 14-MW system compared with the 15-kW model system is associated with the inability to implement low resistance circuits like those of the full-scale hardware in a subscale model system.

Since the closed-loop feedback controls which were developed proved to be inadequate, it seemed appropriate to try to add feedforward controls to them to produce an acceptable system response. Feedforward control is the control of undesirable effects of measurable disturbances by approximately compensating for them before they materialize. The simplified model of the controls with feedforward is shown in Figure 6-7. The feedforward controls that are added will approximately compensate for the converter tare loss by directly affecting the converter's phase angle as a function of the converter output VAR level.

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Figure 6-7. Simplified 14 MW Power Controls Model

The feedforward controls for the 14-MW converter were developed by solving for the phase angle required to compensate for the converter tare losses. The converter tare losses are the sum of two components. One loss component is constant and is the result of energy circulating within the converter to commutate the thyristors. The other loss component is due to the conduction of output current and is linearly related to the converter's output MVA. A computer program was used to solve for the required converter phase angle as a function of the converter's tare losses. The output from this program was a graph of the required converter phase angle vs. the converter's output MVA. The graph is shown in Figure 6-8. This curve is easily approximated by the following linear equation

$$\text{Phase} = -1.68 \times -0.193$$

Where

X = per unit converter VAR output(-1→1)
(since real power ≈ 0)

Figure 6-8. Converter Phase Angle vs Converter VAR Output

The feedforward and feedback controls were added to the 14-MW converter ASTAP computer model. This converter model includes the granularity of the converter controls as well as the tare losses in the converter. The model exhibited acceptable response characteristics as evident from the DC voltage variation resulting from a full VAR Step as shown in Figure 6-9.

Figure 6-9. 14-MW Computer Simulation

Analysis of Input Capacitor Charging - The start-up of a 14-MW converter without a source of dc power requires that the dc input filter be initially charged by some external means. Two straightforward methods are available to initially charge the dc filter. The first method is to charge the filter with a small external dc power supply. This method would require a 3000 Vdc, 15-kW dc power supply and would charge the filter in approximately 30 seconds. The second method would be to close the ac breaker and let the utility line charge the filter through the converter's normal power train. A simplified power train model was used to develop a computer program to analyze this transient. The dc voltage transient is shown in Figure 6-10. The charge-up dc voltage transient does not exceed 96 percent of the maximum dc voltage rating. This is within the acceptable converter operating range. The method of charging the input filter through the converter's power train was selected as the optimum method since it requires no additional power equipment.

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Figure 6-10. DC Filter Charge-Up From AC Line Two-Bridge System

Automatic VAR Dispatch - To obtain the maximum benefit from a self-commutated converter system, the converter's VAR output level should be automatically dispatched as a function of the utility system conditions.

Any measurable utility system parameter could be used to control the converter's VAR output level. These parameters include utility system voltages, currents, and transmission system power factors. Two methods of VAR dispatch as a function of the scaled utility system voltage were demonstrated on the 15-kW model system.

The first control method demonstrated was a direct closed-loop control. In this method of control the scaled utility system voltage was compared to a set point, and the resulting error signal was integrated and used to set the converter's VAR output level. This method of control proved to be very fast and accurate. The rate of response was primarily governed by the converter's normal response time ($\frac{1}{2}$ second). Since closed-loop integral control was used, the steady-state accuracy was 100 percent.

The second method of control demonstrated was an iterative control technique. In this control strategy a small change in VAR flow is initiated, and the resulting effects on the utility line are observed. If the observed effects are beneficial to the system, the process is repeated in the same direction. If the effects are detrimental to the utility system, a change in VAR flow is initiated in the opposite direction. This method is very versatile in that it does not require the utility system's control parameter to be a previously defined function of the

converter's VAR output level. This control versatility allows the same controller to operate with any one of several different utility system variables. The implementation of this method on the 15-kW system required more additional hardware than the direct control method. This, however, is not a serious drawback in the control method. Implementation in a full-scale power system would require the addition of only a small amount of software to the system's master site controller.

Summary of Computer Simulations - This effort demonstrated voltage regulation in the 15-kW Model System. The current controls and logic design were modified to allow a subscale system demonstration of VAR Operation Without a DC Source. Analytical studies verified the ability to apply those modifications to full-scale systems, as well as the ability to charge the dc input filter capacitors via the utility line through the converter power train; thus negating any requirements for an auxiliary dc power source.

The results of the 15-kW Model System and analytical efforts on their application to full-scale systems are summarized below:

The 15-kW Model System demonstrated:

- Operation in the "VAR only" mode with an auxiliary dc power supply as incorporated in the 4.8-MW Demonstrator Power Conditioner
- Inherent response to real and reactive dispatched power demand
- Operation in the "VAR only" mode without an auxiliary dc power supply with tare loss supplied by the utility line and relative phase angle controlled in a function of the converter dc bus voltage
- Operation as described directly above with the VAR flow controlled proportional to the utility line voltage deviations from a desired set point
- Operation with VAR flow controlled by an iterative process to maintain a desired utility line voltage level.

The Analytical effort resulted in:

- A computer analysis of the 15-kW Model System with the appropriate controls modifications that showed good agreement with the test demonstration and confirmed the analytical process
- Adaptation of that analytical process to verify the ability of full-scale systems to operate in the voltage regulation mode.
- Confirmation of the ability to charge the dc input filter capacitors from the utility line through the converter power train in full-scale systems.

Other considerations included:

- Utilization of the converter for power factor correction where the VAR flow is controlled as a function of measured utility line power factor

- Utilization of the converter to enhance system stability where the reactive or real power flow is controlled as a function of any parameter related to stability; such as system frequency.

Recommendation for Full-Scale Hardware Demonstration

Introduction - The previously described analytical and 15-kW Model System demonstration efforts provide the basis for instituting a demonstration of voltage regulation without a dc source in full-scale hardware. The full-scale systems candidates to be considered for that demonstration are:

- The PC19 Pilot Power Plant Power Conditioning System
- The 4.8-MW Demonstrator Power Conditioning System
- The BEST Advanced Converter System
- *• The SBEED Converter

The selection of one of these power conditioning systems for the full-scale demonstrated was based on;

- Availability
- Ability to demonstrate features of voltage regulation
- Cost

A full-scale demonstration plan will be prepared for the selected system. Items included in the full-scale demonstration plan were:

- Design modification of logic and controls to incorporate the voltage regulation without a dc source capability
- Any other required hardware modifications to the system
- Implementation and verification checkout of the modified logic/controls
- A definitive test program to verify operation in a voltage regulation mode without a dc source
- A cost estimate for the overall demonstration
- A scenario describing a systems approach to utilizing the self-commutated converter to its full capacity which includes system stability enhancement as well as voltage regulation and power factor correction.

Candidate Systems - The candidate power conditioning systems under consideration are summarized in Table 6-1 as to their location, status, presently planned utilization and accessibility.

* SBEED will not be fully addressed here, but should be considered. Testing at SBEED which incorporates voltage regulation and system stability enhancements has been proposed.

TABLE 6-1. CANDIDATE POWER CONDITIONING SYSTEMS

System	Location	Status	Presently Planned Utilization	Test Bed Accessibility
PC19	UTC Lab.	Operational	Development testing	(4) excellent
4.8 MW Demo	New York City	Operational 1980	Operational feasibility demonstration	(2) good
BEST	New Jersey	Operational (1) 1983	Advanced technology evaluation	(3) excellent
SBEED	Michigan	Operational (1) 1983	Feasibility demonstration	(2) good

(1) Not contracted at date of this assessment

(2) Not in present plan and would require scheduling into planned utilization.

(3) Provided advanced power conditioner is implemented

(4) May be dismantled to provide laboratory space for future development efforts

Table 6-2 provides a systems description summary of the candidate systems.

TABLE 6-2. SYSTEM SUMMARY OF CANDIDATE POWER CONDITIONING SYSTEMS

System	Power Rating	Type of DC Source	DC Voltage Operating Range	Number of Bridges	Type of Harmonic Reduction	Type of Logic	AC Utility Interface Volt. Level	To Operate in Stand Alone Voltage Regulation
PC19	1 MW	DC power supply	1180 to 1750 Vdc	3	magnetics	digital	14.4 kVac	modify controls
4.8 MW Demo	4.8 MW	Fuel Cell	2680 to 3450 Vdc	3	magnetics	digital	13.8 kVac	modify controls
BEST ¹	1 to 2 MW	Battery	500 to 1000 Vdc	1 or 2	switching pattern	micro-processor (advanced)	13.8 kVac	baseline design ²
SBEED ³	10 MW	Battery	2000 to 3000 Vdc	3	magnetics	digital	13.8 kVac	modify controls ³ design

¹ Proposed BEST facility converter - design details not available, not contracted.

² Proposed system incorporates feature into basic logic design per work being done under Task 2.

³ Modify design and operate in test mode. Note - not yet contracted.

Table 6-3 summarizes the previously described selection criteria on a relative basis as applied to the candidate systems and adds a technology consideration which is weighed heavily: it being most appropriate to demonstrate the capability with a converter technology that most closely reflects the system that will be commercially utilized.

TABLE 6.3 - RELATIVE SUMMARY OF SYSTEM SELECTION CRITERIA

Relative position given with lowest number being most favorable				
Candidate Converter	Availability	Demonstration Ability	Cost (1= least expensive)	Technology Consideration
PC19	1	2	2	3
4.8 MW Demo	2	2	3	2
BEST*	1	2	**1	***1
SBEED*	2	1	3	2

* Provided this converter program is implemented

** Present proposal designs capability in - no add on design cost as with other candidates

*** Will reflect latest technology of the candidate converters

Notes:

- 1) If BEST or equivalent is not implemented, the capability may be a moot point
- 2) Demonstration should include demonstration of stability enhancement; already proposed for SBEED

System Selection - The evaluation of the four selection criteria for system selection (availability, demonstration ability, cost and technology).

With the technology consideration weighed heavily, the logical system choice is the BEST Advanced Self-Commutated Converter System. It is rated second only in the demonstration ability category and is top rated in the other three categories. It is also recommended, due to its most favorable converter rating/ feeder rating ratio that the ability of the self-commutated converter to enhance system voltage regulation, power factor, and stability also be demonstrated in the SBEED Program.

The two efforts will provide:

- 1) A demonstration of the technology most closely reflecting that which will be used in commercially designed systems
- 2) A demonstration in a system showing the commercial/economic benefits of battery energy storage.

Full-Scale Demonstration Plan -

- Logic Control and Hardware Modification

Two previously mentioned items to be included in the demonstration plan were logic/control design modifications and any hardware modifications required. Selection of the BEST Advanced Converter deletes most of those two. The BEST facility site controller for the Advanced Self-Commutated Converter would require the following to provide the capability to demonstrate voltage regulation.

Inputs - 1) Signal representing utility line voltage to be regulated

2) Signal representing desired line voltage

Functions - Regulator closed loop control that determines the difference of the inputs and generates an appropriate error signal which is conditioned and provides a VAR demand signal

Output - VAR demand signal to the converter

Designating the site controller for functions of this type allows a fixed converter design with the site controller providing custom system requirements. This control philosophy can be applied for use with any control parameters, such as power factor or system stability.

- Implementation and Checkout

A simple control designed around a well-documented site controller will be "plug-in" implemented, or could be baseline designed into the site controller. Control checkout would consist of three stages:

- 1) Simulated input/output evaluation - converter not operating
- 2) Operate converter with control open loop and assess VAR demand signal to converter
- 3) Operate closed loop and assess and analyze converter VAR generation and its effect on line voltage regulation.

The UTC self-commutated converter contains protection circuitry to prevent operation outside its rated kVA capability, regardless of site controller demand signals. Thus it will supply reactive power to its maximum capacity only and a site controller demand for higher levels will not create an overload problem. This feature exemplifies the philosophy of utilizing the self-commutated converter with its control logic and self protection in a baseline design and placing the power (real or reactive) demand function at the site controller.

• Test Program

Once the required system control modifications and their implementation and check-out are completed, a two stage test program is recommended; Figure 6-11 provides an outline.

- Stage 1 - Perform open-loop baseline testing with control adjusted to respond to a VAR demand signal and maintain a steady state line voltage regulation
- Stage 2 - Determine the system closed-loop operation over a range of control response times with the VAR demand signal time constant varied from steady state to a maximum transient.

Prior to control design an analytical effort is required to define the proper boundaries for a control response range. A computer analysis which incorporates a BEST Utility line feeder model and a converter model must be performed to determine the control design requirements, and to minimize any negative effects such as system instability or interaction with the utility line power factor correction capacitor controllers. The analysis should result in determination of a range or set of response times over which the voltage regulation control can operate without any negative system effects, and will provide expected test results which can be compared to the actual test results.

PRELIMINARY ANALYTICAL EFFORT - MODEL AND ANALYZE UTILITY LINE, CONVERTER AND CONTROL

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Figure 6-11. Test Program Outline

United's experience in digital and analog computer simulations, with the necessary inputs describing the BEST facility utility interface, permits the desired analysis. A similar effort was undertaken to design the control for the 15-kW Model System demonstration and to determine full-scale system control requirements for converter operation into the distribution feeder at United's Fuel Cell Operations Facility.

Required Instrumentation, as shown in Figure 6-12, would consist of:

- 1) A high-speed, high-accuracy voltage recorder for monitoring the line voltage control input, both steady state and transient
- 2) A utility line disturbance monitor to measure utility line transient and RMS voltage changes - triggers voltage recorder to obtain data or response to various utility line voltage changes
- 3) A high-speed, high-accuracy recorder for measuring the control output VAR demand signal and the converter delivered vars (a four channel transient analyzer would satisfy 1) and 3)), plus recording of the signal representing the desired line voltage regulated level.
- 4) A voltage recorder for monitoring the converter dc input filter capacitor voltage
- 5) Not absolutely required, but of interest; a recorder to monitor the status of any utility line power factor correction capacitor bank switches.

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Figure 6-12. Voltage Regulator Instrumentation

Testing would then consist of a week of open loop testing to determine the ability of the converter VAR generation to affect the line voltage and several weeks of operation in the voltage regulation mode (contour system operation to allow testing of this mode during all time periods). Experimental test data would be analyzed to determine response to the various system voltage fluctuations and the test data then compared to the analytical predictions.

Discrepancies between test method results and the analytical method results can then be resolved and the appropriate analytical/test adjustments made. Once the two methods are in agreement, the analytical process will be verified and can be utilized with confidence for analysis of other potential system uses.

The final results of the test program would include:

- A proven analytical technique for predicting operation and designing a control for operation of a self-commutated converter as a voltage regulator
- Test results showing the ability and benefit of converter voltage regulation
- An indication of potential system problems that might occur in this mode
- A proven instrumentation scheme for further studies and/or analysis of other utility distribution feeders

o Program Cost Estimate

Costing of this program was difficult as it primarily consisted of cost deltas and add-ons from an overall system program. This rough estimate was broken down into six major elements:

- Analytical effort-preliminary and ongoing
- Control design and implementation
- Hardware
- Control checkout
- Instrumentation
- Test program

The estimates, where appropriate, were given in manpower and material cost; Table 6-4 summarizes these estimates.

TABLE 6-4. MANPOWER AND COMPONENT COST ESTIMATE

Test Plan for Full-Scale Voltage Regulation Without A DC Source

Item	Hardware Component Cost Estimate	Manpower Estimate	Description
	thousand of dollars	man-months	
• Preliminary Analytical		2.00	System modeling and baseline analytical design
• Ongoing Analytical		2.00	Analyze all test/analytical results
• Control Design		.50	Design, construct and implement
• Control Construction		.50	Control into the BEST Facility
• Control Implementation		.50	Site Controller
• Hardware	1.0		Voltage regulation control components and package
• Control Checkout		1.00	Verify control operation statically and dynamically after implementation
• Instrumentation*	1.0	.50	Define and procure instrumentation sensing interfaces and connect instruments
• Test Program		2.50	Phase 1 and 2 test efforts
<u>TOTALS</u>	2.0	9.50	

*Assumes instruments are available at the BEST Facility.

• System Scenario

Future alternative energy systems will result in a significant penetration level of solid state power conditioners being interfaced to the existing utility grid system. The self-commutated converter will constitute a large portion of that penetration level. Its primary function will be to condition power from various dc sources for peaking, base load, and other utility generation applications. Development efforts should also include and exploit its inherent ability to perform other functions such as utility line voltage regulation, power factor correction, system stability enhancement, to insure availability for future applications.

Any utility company employing self-commutated converters should utilize them to their full capabilities, and present as well as future demonstration efforts should include segments that address that overall utilization capacity.

The system scenario thus constitutes the following for installations such as initial battery load leveling or fuel cell tests:

- Demonstrate and verify baseline power conditioning and handling capability vs. predicted design performance
- Extend the demonstration to include:
 - 1) The benefits of VAR generation for line voltage regulation and power factor correction
 - 2) The benefits of stability enhancement with real or reactive power as required

Advanced planning that factors in the overall self-commutated converter features, coupled with the low cost of incorporating those activities into microprocessor based logic designs for the site controller and converter, can provide the overall system evaluation at a minimal cost delta over the baseline assessment.

● Conclusions

- 1) A full-scale test demonstration of the self-commutated converter acting as a utility line voltage regulator should be performed at the BEST Facility
- 2) The voltage regulation demonstration will be low cost in hardware and manpower
- 3) BEST and SBEED should also be utilized for demonstrating the self-commutated converters ability to enhance system stability and to provide power factor correction
- 4) Future full-scale demonstration should include overall systems capability testing in their baseline definition.

Assessment of Benefits

Introduction - The voltage regulation capability exists as a feature users of self-commutated converter systems have at their disposal whether the dc source is operating or not. This capability should be factored into the overall system operation in a manner that extracts the maximum benefits. With the ability inherent and the cost/complexity for exploiting the ability essentially negligible, the economic benefit incurred is primarily a function of the cost of operating the converter (electrical operating cost) compared to the cost of alternative VAR sources such as power factor correction capacitors or inductors (installed cost capitalized over a specific period, plus electrical operating costs). Mean time between failures and availability are also areas that must be considered in assessing the system benefit. This analysis will concern itself primarily with the economics of operating the self-commutated converter as a VAR generator vs. the installed and operating costs of power factor correction capacitors and inductors (shunt reactors). The areas of mean time between failure and availability will be discussed as to their impact along with considerations for VAR control applications. This analysis assumes a reasonable voltage regulation capability at all

times. This may not be true at the peak real power operating point. If the system is operated as spinning reserve capacity, then this capability will be available. However, if the system is expected to be operating at peak real power when the VAR capability is required, then either the converter must be oversized or a trade-off must be made to optimize operation between real and reactive power. If the converter is oversized, then a small increase in system capital cost and a small decrease in efficiency must be considered a cost of this capability. Table 6-5 summarizes the reactive power compensation methods to be assessed and indicates the items considered in the economic analysis.

TABLE 6-5. REACTIVE POWER COMPENSATION METHODS

Items Considered in Economic Analysis			
Method	*Equipment Cost	*Installation Cost	**Electrical Operating Costs
Self-commutated Converter (var only)			X
Substation Type Power Factor Correction Capacitors	X	X	X
Shunt Reactors	X	X	X
Static Var Generators	X	X	X

* Includes ancillaries such as fusing, switchgear, wiring, etc.

** Electrical energy supplied by utility line

Self-Commutated Converter - Operation of the self-commutated converter in the VAR only mode requires that the utility system provide the electrical power required by the converter for commutation magnetics excitation, conduction losses, and other ancillary equipment such as logic, controls, fans, etc. The amount of power required varies as a function of the operating efficiency of the converter which is established primarily by the amount of VARS being generated (conduction losses) and the level at which the dc bus is maintained (impacts commutation losses). The magnetics excitation and ancillary equipment power requirements are essentially constant regardless of VAR loading or dc bus level.

Under EPRI Research Project 841-1, "AC/DC Power Converter for Batteries and Fuel Cells," and as reported in Reference 1, an efficiency study of a 14-MW wide range advanced converter was performed. Figure 6-13 shows converter efficiency vs. dc voltage at 1/4 and rated power taken from that study and it will be utilized as the basis for establishing converter electrical power requirements for this analysis of electrical operating costs.

While the efficiencies from Figure 6-13 are for real power operation, the electrical power requirements supplied by the utility line during VAR only operation do not differ significantly. For this analysis the losses associated with the converter efficiency will be considered, whether the load is real, reactive, or any combination of real or reactive up to the kVA rating of the converter.

As Figure 6-13 shows, the dc bus voltage level has a significant impact on efficiency especially at lower load levels, with efficiency increasing as the dc bus voltage decreases (power remains fixed at 1/4 or full). That is due to the lower dc bus voltages resulting in lower commutation losses, and it dictates that the most economic operation in the VAR only mode will be at as low a dc bus voltage as possible. From the work done previously in this subtask, it can be assumed that while in the VAR only mode the dc bus voltage can be controlled to within $\pm 10\%$ of a desired level. Allowing about a 10% voltage margin to prevent nuisance low voltage dc interrupts, a nominal dc bus voltage operating level of 2600 Vdc will be utilized for this assessment of electrical operating costs. Figure 6-14 shows the converter losses at 2600 Vdc from 1/4 to full kVA as extracted linearly from Figure 6-13.

Figure 6-13. Efficiency vs DC Voltage for 14-MW Wide Range Converter

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Figure 6-14. Converter Losses vs kVA Load at Constant Input of 2600 Vdc

Figure 6-14 shows that reactive power losses per KVAR become less when the converter is operating in a real power mode and generating VARS within its kVA rating. In that mode the losses associated with the VAR generation are the difference between the loss for real power operation and the total loss due to overall kVA loading. For example, if a 1.0 kVA converter operated at 0.5 kW real power at 1.0 power factor (equaled 0.5 kVA), loss would be a little over 51 watts per kVA (kW). At 0.5 kW real power, the VAR capacity to rated kVA is:

$$\text{VAR capacity} = \sqrt{(1.0)^2 - (.5)^2} = \sqrt{.75} = .866 \text{ KVAR}$$

Rated kVA losses are 34 watts/kVA from Figure 6-20

Total losses for each point above are:

- 51 watts/kVA x .5 kVA or = 25.5 watts
- 34 watts/kVA x 1.0 kVA = 34 watts

Thus 8.5 watts additional loss is incurred in adding .866 KVARs to a 0.5 kW real power load. VAR only operation at .866 KVARs (kVA @ zero P.F.) would result in approximately (.866 KVARs x 39 watts/kVA) 33.7 watts loss.

This study will concern itself with assessing the benefits of VAR only operation. The above analysis merely points out the fact that wherever the economics are benefited by VAR only converter operation: operation with reactive power added to real would show a greater benefit (provided that total real and reactive loading is less than the machine KVA rating).

Reactive Power Systems Considered

This analysis will concern itself with reactive power systems of 10 megavar rating in the 15 kilovolt equipment class. The systems to be analyzed are as follows.

Battery energy storage self-commutated converter - The system is shown in Figure 6-15 in simplified block diagram form and is assessed under these ground rules:

- Capital cost charged to real power generating duty
- No dc source in var-only mode
- Energy losses as shown in Figure 6-14
- Assume incremental maintenance costs evolved from var-only operation are negligible

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Figure 6-15. Battery Energy Storage Converter System

Power factor correction capacitors - As shown in Figure 6-16, the system consists of the capacitor bank which is connected to the utility line via an oil-filled switch and a protective fuse. The economic assessment considers the installed cost of the oil-filled switch, protective fuse and the capacitor bank, plus the operating energy cost.

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Figure 6-16.

Power Factor Correction Capacitors

The installed equipment costs were lumped together and result in a figure of \$11.00 per kVAR for a 10 MVAR system. The operating energy requirement is 1.0 watt/kVAR based on the following:

- As shown in Figures 6-17 and 6-18, the capacitor loss is 0.6 watt/kVAR
- Added to the 0.6 watt/kVAR are the discharge resistor loss plus miscellaneous wiring, switchgear and fuse losses which result in the 1.0 watt/kVAR.

POWER CAPACITORS WITH MIXED PAPER AND POLYPROPYLENE DIELECTRIC

Paper presented in the name of Study Committee No 15 (Insulating Materials)

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SUMMARY

A new dielectric system consisting of alternate layers of biaxially-oriented polypropylene film and kraft-cellulose tissue impregnated with polychlorodiphenyls has been developed to replace the conventional impregnated-paper dielectric in power capacitors.

Capacitors employing the new composite dielectric system can be made in unit ratings up to 150 kVar and possibly larger for special applications with losses in the order of 0.5 to 0.6 W/VAR; this compares with unit ratings up to 100 kVar and losses of 1.9 to 2.2 W/kVar for the best all-paper capacitors.

The report after a general illustration of the new capacitors gives more detailed information on losses and their behaviour with temperature; voltage and time on temperature and its distribution in the interior of the capacitors and on problems for the detection of partial discharges

Capacitor, Dielectric, Paper, Polychlorodiphenyl, Polypropylene.

Figure 6-17. Paper from Annual CIGRE (Conference International des Grands Redoux Electriques) Conference Proceedings

Figure 6-18. From McGraw Edison Bulletin 76029, May 1976.

Shunt reactor - The system consists of an oil circuit breaker for connecting the shunt reactor to the utility line as shown in Figure 6-19.

Figure 6-19. Shunt Reactor System

From data obtained from Westinghouse literature*, the installed cost for a 10 MVAR system for the shunt reactor and circuit breaker is \$3.80/kVAR. The operating energy requirement is 6 watts/kVAR which consists of 5.7 watts/kVAR for the shunt reactor from Figure 6-20 and 0.3 watts/kVAR miscellaneous for wiring and switchgear.

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Figure 6-20. Shunt Reactor Operating Losses from Westinghouse Literature

Static VAR generator - This system most closely resembles the converter system in regards to being able to supply leading or lagging reactive power with infinite variable control. As shown in Figure 6-21, it is the most complex of the systems whose only function is to supply reactive power.

The installed equipment cost is \$17.2/kVAR based on the earlier costs for capacitors, shunt reactors, fuses, and switchgear, plus \$2.4/kVAR estimated for the static shunt reactor switch. The operating losses for this analysis are 5 watts/kVAR based on the average between:

- 1.0 watt/kVAR for just the capacitor portion
- 9 watts/kVAR for just the shunt reactor portion, which consists of the previously discussed 6 watts/kVAR for the reactor plus miscellaneous, and 3 watts/kVAR for the static switch

*Westinghouse General Catalog Reference 33-000, Section PL 45-423, pp. 2 and 3.

Figure 6-21. Static VAR Generator

Reactive Power Systems Comparisons

Table 6-6 shows the comparison between the four systems in regards to energy loss while operating. The battery converter has higher losses that are somewhat offset by its capital cost being attributed to its operation with the battery source. Table 6-7 shows the comparison between the systems for annual capital cost. As would be expected, the most complex and flexible of the other systems, the static VAR generator, has the highest annual capital cost.

TABLE 6-6. ENERGY LOSS COMPARISON

<u>SYSTEM</u>		<u>LOSSES</u> <u>WATTS/VAR</u>
<u>BATTERY</u>		
o	INCREMENTAL LOSS AT 25% CONVERTER REAL LOAD	60
o	INCREMENTAL LOSS AT 50% CONVERTER REAL LOAD	52
o	INCREMENTAL LOSS AT 75% CONVERTER REAL LOAD	43
o	INCREMENTAL LOSS AT 100% CONVERTER REAL LOAD	34
POWER FACTOR CORRECTION CAPACITOR		1/4
AIR CORE DRY TYPE SHUNT REACTOR		6
STATIC VAR GENERATOR		5

TABLE 6-7.: CAPITAL COST COMPARISON
(1980 DOLLARS)

SYSTEM	INSTALLED CAPITAL COST, \$/KVAR	USEFUL LIFE, YEARS	ANNUAL CAPITAL CHARGE, %	ANNUAL OWNING COST, \$/KVAR/YEAR
Battery Converter	0	---	---	0
Power Factor Connection Capacitors	11.0	20 Yrs	.18	\$1.98/kVAR/Yr
Air Core Dry Type Shunt Reactor	3.8	20 Yrs	.18	\$.68/KVAR/Yr
Static VAR Generator	17.2	20 Yrs	.18	\$3.10/kVAR/Yr

* Includes Capital Recovery, Interest & Fixed Charge Burdens, and Return on Investment

Table 6-8 summarizes the value attributed to the operating losses, based on fuel cost overhead and maintenance and shows a total value of electricity of \$.024/kilowatthour. Table 6-9 then shows a cost comparison for the systems for owning and operating them. The battery converter has the lowest owning cost for the "VAR only" operating mode, but has the highest operating cost.

TABLE 6-8. VALUATION OF ELECTRICITY LOSSES

Value Electricity at Incremental Cost Of Production

- Fuel Cost
- O & M Cost

U. S. Average Fuel Costs

- Average Fossil Fuel Cost = $\$1.85/10^6$ Btu
- Average Heat Rate = 10,500 Btu/kWh
- Average Fuel Costs = .5¢/kWh

Total Value of Electricity = 2.4¢/kWh

TABLE 6-9. ANNUAL OWNING & OPERATING COST COMPARISON

System	\$/KVAR/Yr Owning Cost	\$/KVAR/Yr Operating Cost		
		Hours/Yr Utilization		
		440 Hrs (5%)	880 Hrs (10%)	1300 Hrs (15%)
<hr/>				
<u>Battery</u>				
Converter				
50% Avg Load	0	.55	1.10	1.65
75% Avg Load	0	.45	.90	1.35
100% Avg Load	0	.36	.72	1.08
Capacitor Power Factor Connection	\$1.98	.003	.005	.008
Air Core Shunt Reactor	\$.68	.06	.13	.19
Static VAR Generator	\$3.10	.05	.11	.16

Economic Assessment Summary

Figure 6-22 summarizes the assessment of annual owning and operating costs for the four reactive power systems considered. The battery converter is shown to be of economic benefit relative to the other three reactive compensation methods based on the hours per year it is utilized in the reactive power mode. For example, Figure 6-22 depicts that if the utility system requirement is for 10 MVARs (converter 100% average load curve) to be delivered for less than 2400 hours per year, the battery converter is economically superior to the power factor correction capacitor. That, of course, assumes that the battery converter has been installed as part of a battery energy storage system and is available for VAR only operation during the hours that reactive power is required.

Figure 6-22 also shows that the battery converter economically compares most favorably with the static VAR generator, which is the only conventional method that has a comparable flexibility in regards to lead/lag reactive ability coupled with infinite control variation.

The overall significance of the study is that within operating time limitations the battery converter can compete economically with conventional means of reactive power compensation. Users of the battery converter must take into account the economics and availability aspects that apply to their utility systems to determine the most appropriate and beneficial use they can make of this self-commutated converter operating feature. The battery converter is not, and should not be, promoted as a general duty substitute for power factor correction capacitors or shunt reactors. However, if the converter is part of a system that requires reactive compensation for appropriate periods of time, the converter can be economically superior to the more conventional approaches. For example, if short term instances

occur where reactive power is required for system stability, it may prove advantageous to utilize an available battery converter rather than installing one of the other methods.

Conclusions

- 1) The battery converter can be of economic benefit in the "VAR only" mode of operation.
- 2) The benefit(s) and how to extract it (them) is dependent upon the system requirements for each user.

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Figure 6-22. Annual Owning and Operating Cost Comparison - Power Factor Control Systems

Section 7

TASK 5 - BATTERY MODELING

TASK DESCRIPTION

In order to design an optimized power converter for use with advanced batteries in battery energy storage systems, a detailed knowledge of the battery-to-converter dc interface must be acquired. This is necessary to ensure that the battery converter system operates with the highest possible efficiency under normal conditions, and that all parts of the system are properly protected during abnormal operating conditions. Examples of the type of data needed include the small-signal characteristics, large-transient performance, protection requirements, and static charge/discharge profiles. The objective of this task was to update the information regarding these characteristics through a manufacturer survey, and to develop a battery modeling approach that would facilitate analysis of these advanced battery systems. Such analysis could be used to quantify those battery characteristics important to the converter design, and to determine the battery characteristics important to the battery system design. An additional requirement was the preliminary design of a portable battery tester that could be used to obtain the data required by the selected modeling approach. Task efforts were supported by a literature search that attempted to locate specific sources of information regarding modeling and testing of the selected battery types.

STATUS

Task 5 work was completed during this reporting period.

LITERATURE SEARCH

Purpose

A literature search was performed to determine if some of the required information on battery static and dynamic characteristics could be located in previously published sources. This would help direct the task and support its conclusions and recommendations, as well as help pinpoint areas where published information is lacking. Two major areas were investigated: battery characteristics, such as charge/discharge profiles and protection requirements; and, battery equivalent circuit modeling techniques.

Results

Approximately three dozen technical articles and reports were obtained for review; a bibliography of the most appropriate publications is presented in Appendix 2. Although a few of these references provided much detail about the electrochemistry construction, performance, and costs for some of the advanced batteries, relatively little information was found regarding their transient characteristics, protection requirements, or static voltage/current vs time profiles. Those references dealing with battery models showed that there are nearly as many different models as there

are investigators. Very few "general purpose" battery models were found. Most deal with electrochemistry effects or state-of-charge and are mathematical models rather than equivalent circuit models.

MANUFACTURER SURVEY

In order to better understand the battery-to-converter interface, United conducted a survey of several advanced battery manufacturers. The U. S. Department of Energy (DOE) selected the manufacturers to be surveyed; they are listed in Table 7-1, with their respective battery types.

TABLE 7-1 ADVANCED BATTERY MANUFACTURERS SELECTED BY
DOE FOR SURVEY

MANUFACTURER	BATTERY TYPE
Argonne National Laboratory	Lithium/Metal Sulfide
C&D Batteries	Lead/Acid
Energy Development Associates (G+W)	Zinc/Chloride
General Electric Company	Sodium/Sulfur
Gould, Inc.	Zinc/Bromine

The primary objective of this survey was to obtain detailed, up-to-date electrical characteristics for each of these advanced batteries. A questionnaire was developed to elicit the required information. Table 7-2 is an outline of the survey questionnaire format; the complete document appears as Appendix 3.

Battery manufacturers provided good cooperation in responding to the survey. Manufacturers supplied good V/I data, some protection information, but relatively little equivalent circuit model data. Considering the present state of the art, this is consistent with expectations regarding the amount of detailed information available. A summary of the survey results is given in Table 7-3.

Reduction of the data obtained from this survey included comparison with data from two previous battery manufacturer surveys, conducted by United (3) and by Hittman Associates (5). A number of major electrical parameters were compared for each battery type; the results are shown in Appendix 4. There is good agreement among the three sources of battery information. Although this survey yielded more detailed information in some areas, there are still a few areas where additional data will be required before the battery energy storage system requirements are defined. Most notably, better information will be required regarding the protection requirements of advanced batteries.

TABLE 7-2. QUESTIONNAIRE OUTLINE

SECTION	TITLE	INFORMATION REQUESTED
I	Voltage/Current Characteristics	V/I Curves, VMAX, VMIN, Control Requirements
II	Efficiency and Capacity	A-hr and W-hr Efficiency and Capacity
III	Battery Protection	Fault Characteristics, V/I Withstand, Ripple Tolerance
IV	Battery Arrangement	Cell Connections for 100-MWhr System
V	Equivalent Circuit Models	Transient Models for Cell and System, Plus Test Methods Used to Obtain Them

TABLE 7-3. SURVEY RESULTS SUMMARY

CHARACTERISTICS (PER CELL)	LITHIUM/ METAL SULFIDE	ZINC/CHLORIDE	SODIUM/SULFUR	ZINC/BROMIDE	LEAD/ACID
V _{min}	1.0	1.6	1.6	1.5	1.7
V _{max}	1.6	2.3	2.3	2.0	2.6
Voltage Ratio	1.6	1.4	1.4	1.3	1.5
Fault Current (Per Unit)	---	6	4-10	5	100
Ripple Tolerance	---	>10% (Current)	~14% (Current)	---	10% (Voltage)
V/I vs. t Curves	No	Yes (Constant Current)	Yes (Constant Current)	Yes (Constant (Current)	Yes (Constant Power)
Equivalent Circuit Model	No	No	Yes	No	Yes

BATTERY MODELING

Introduction

The objectives of this portion of the task were to:

- Develop a battery equivalent circuit modeling approach that could be applied to advanced batteries;

- Specify a method for testing advanced batteries to obtain the required data for modeling;
- Prepare a preliminary design of portable test equipment that could be used for such testing.

Battery equivalent circuit models are needed to facilitate analysis of the battery-converter dc interface.

Investigation of the battery's response to both normal transients (e.g., switching or sudden load changes) and abnormal transients (e.g., dc bus faults or lightning strikes) will help to define operational limits and protection requirements. The effects of ripple on the battery can be studied using equivalent circuit models; this will help to determine converter specifications. In general, analyses utilizing battery models will enhance the ability to design the battery/converter system. For performing the above analyses, a battery model should be capable of predicting the following battery characteristics:

- Terminal voltage as a function of load current for both steady-state and transient conditions;
- Impedance as a function of frequency.

These characteristics may be dependent upon a variety of factors, such as:

- State of charge
- Operating point (present load)
- Previous history of the battery and its age
- Temperature.

The degree of dependence varies widely, and there are also other factors not considered here. The test method used to collect data to establish the battery equivalent circuit model parameters should be fast (to account for time variations in the above factors) and should not affect the battery operation while measurements are taken. In addition, the model should be simple and easy to implement. Unfortunately, no such ideal test procedures or models were located.

Only two of the five advanced battery manufacturers surveyed in this task had determined equivalent circuit models of their batteries. In addition, it was concluded from the literature search that there are nearly as many approaches to modeling as there are investigators involved with this subject. Several articles have addressed the applicability of different models to specific batteries (6), while others have addressed the use of different models for analyzing the use of different batteries in specific applications (7). Still others have attempted to derive generalized models for use in computer simulations (8, 9). However, this literature search yielded no single model that appeared adequate for general application to the study of utility-scale battery energy storage systems under a wide range of steady-state and transient conditions and for different physical conditions such as age, temperature, etc. Therefore, it was decided to construct a

model with the hopes of satisfying these requirements in such a manner that the appropriate model parameters could be obtained by a relatively simple test procedure, which also would be specified. The approach taken is outlined below.

Modeling Approach

As described above, there are a number of factors that might affect the battery's performance under a given set of operating conditions. It may be logically assumed that these factors could affect the form of the battery equivalent circuit model. Therefore, the model developed in this task provides the user with enough flexibility to account for such factors. The resulting model may be as simple or as complex as desired, depending on the accuracy required or the range of operating conditions to be studied.

Figure 7-1 shows the block diagram for a generalized battery model. This model is a Thevenin equivalent consisting of an ideal voltage source (EOC) (Block 5) and a series impedance (Block 1 - Fast Small-Signal Response). EOC is the battery open-circuit voltage, which is dependent upon certain physical parameters (Block 4) such as age and temperature, and on state of charge (Block 3). The small-signal response is an electrical equivalent that is synthesized from the battery's frequency response. The frequency response (Bode plot of impedance magnitude and phase vs. frequency) is obtained as follows.

NOTES: (Refer to block numbers)

- (1) This block is an electrical equivalent circuit synthesized from the battery frequency response obtained by testing under various operating conditions.
- (2) This block varies the small-signal response according to the system operating point (what terminal voltage results from a given load current).
- (3) State of charge can be determined by integrating current with respect to time; its major effect is on E_{OC} .
- (4) Physical parameters that affect the battery might include age, temperature, etc.
- (5) E_{OC} is an "ideal" voltage source representing the battery open circuit voltage for the condition of interest.

Figure 7-1. Generalized Battery Model Block Diagram

Using the Bode plots generated by testing the battery, a transfer function for the battery is obtained. This transfer function can then be used to synthesize an equivalent circuit in one of several forms by standard analytical techniques. Reference 10 describes response testing and transfer functions; References 11, 12, 13, and 14 describe network synthesis techniques. Figure 7-2 outlines the procedure used to develop an equivalent circuit model from battery testing.

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Figure 7-2. Determination of Battery Equivalent Circuit Model from Test Data

A number of Bode plots must be obtained for a battery, corresponding to different operating points, states of charge, and physical parameters. The results of these tests under different conditions dictate the form of the circuit in Block 1, and the way Block 1 is modified by Block 2. In addition, the variation of EOC with state of charge and physical parameters is determined through dc steady-state tests; new sets of Bode-plot data are taken and equations are written to describe the dependence of EOC on each parameter.

Each block in the model must therefore be determined by the user. However, as stated above, the model is flexible in that any of the blocks may be expanded or deleted, depending on the user's interests. Although the circuit model so developed is intended to be linear (i.e., consisting of resistors, capacitors, and inductors), an individual user may find some non-linear form more suitable. Other applications may dictate that the model be left in La Place transfer function form for convenience of calculation and manipulation.

Test Procedure and Equipment

A generalized test procedure was determined for finding the form and contents of the blocks in the model of Figure 7-1. The first step is to perform dc tests to establish the battery V-I characteristic and determine its sensitivity to such variables as state of charge and physical parameters. This yields the relationships needed to complete Blocks 3 and 4 in the model. These impedance measurements are taken (using one of several methods outlined below) to provide the data needed to derive or synthesize the model for Block 1. These measurements are taken over a range of operating points to determine the contents of Block 2, which will vary the elements of Block 1 according to operating points on the load curve (voltage/current characteristic).

The final activity in this task was to determine the requirements for test equipment needed to obtain data for constructing the generalized battery model. This equipment falls into two categories:

- (1) Static load bank (resistors) and voltage/current instrumentation to determine V/I characteristic for battery under different states of charge, and physical parameters. See Figure 7-3.
- (2) Dynamic test equipment - The objective is to obtain the frequency response data needed for the model. One method is shown in Figure 7-4. A custom-built pulsed loading scheme is used to take an individual impedance measurement (calculated from a voltage and current measurement) at each discrete frequency in the spectrum of interest.

THIS SET-UP IS USED TO MEASURE THE BATTERY'S STATIC V/I (VOLTAGE vs. CURRENT) CHARACTERISTIC FOR VARIOUS BATTERY STATES OF CHARGE, TEMPERATURES, OR AGE ETC.

Figure 7-3. Test Set-Up for Determining Battery Static Voltage vs. Current Characteristic

THIS SET-UP IMPOSES A SMALL SINUSOIDAL SIGNAL ON THE STEADY-STATE BATTERY CURRENT. BATTERY IMPEDANCE AT A PARTICULAR FREQUENCY IS FOUND FROM THE RATIO OF THE AC VOLTAGE TO THE AC CURRENT.

Figure 7-4. Test Set-Up for Determining Frequency Response of Battery

United has built and used successfully this type of equipment for testing fuel cells and obtaining data required to construct their equivalent circuit models. However, since many measurements are required to cover the frequency spectrum of interest, this method is somewhat slow. As a result, the battery state-of-charge could vary enough to affect the measurements (assuming that the equivalent circuit actually depends on state-of-charge).

The alternative method is to use a commercially available digital waveform analyzer to take the frequency-response measurements. This resolves the speed-of-measurement problem, since it is a broad-band, nearly instantaneous method of generating a Bode plot for a particular battery operating point. Such a technique also simplifies data-taking and data reduction, and also simplifies the design of the portable battery tester.

An example of the type of instrument recommended for this application is the Hewlett-Packard 5420-A Digital Signal Analyzer (Figure 7-5), which is described in detail in Hewlett-Packard product literature. Figure 7-6 shows a block diagram of a test set-up for taking battery frequency response measurements using the "white noise" source contained in the HP5420-A.

Figure 7-5. HP5420A Digital Signal Analyzer

The Hewlett-Packard 5420A Digital Signal Analyzer utilizes sampled data techniques to perform a wide variety of single and dual channel measurements over a 25 kHz frequency range. Measurements include Time Record Averaging, Auto and Cross Correlation, Impulse Response, Auto and Cross Spectrum, Transfer Function and more. Important features include Band Selectable Analysis, which provides excellent frequency resolution, and built-in data storage on digital magnetic tape cartridges. The instrument also contains a random noise generator, which is useful as a test stimulus, and it provides a fully-annotated dual-trace display with flexible cursor capabilities. The 5420A may optionally be equipped to provide alphanumeric and graphic hardcopy directly on an HP Model 9872A Graphics Plotter. All measurements illustrated in this note were recorded in this fashion.

Figure 7-6. Simplified Test Set-Up for Battery Frequency Response Using Digital Signal Analyzer

The digital signal analyzer (DSA) takes fast Fourier transforms of the two analog input signals (Channels 1 and 2), and from them calculates impedance for the range of frequencies generated by the on-board white noise generator, dc to 25 kHz. The Bode plot (impedance magnitude and phase) is displayed on the cathode ray tube (CRT) and can be drawn on the accompanying X-Y plotter. The data from each run can be stored digitally on a self-contained magnetic tape cassette for later analysis and manipulation and can be displayed again at a later time.

An evaluation of the recommended test equipment was performed to assess its capability for taking battery frequency response data. Using the HP5420-A as shown in Figure 7-7, a small automotive-type lead-acid battery was tested under various conditions of charge and discharge. Figure 7-8 shows a typical Bode plot obtained from the testing.

Figure 7-7. Test Set-Up for Evaluating HP5420A Digital Signal Analyzer for Battery Frequency Response Testing

Figure 7-8. Example Bode Plot Obtained from Evaluation of Battery Test Equipment: Impedance Magnitude and Phase vs. Frequency, Charged Lead/Acid Storage Battery During Charge.

It was concluded that this method would be suitable for advanced battery testing. Table 7-4 shows the estimated costs for constructing a portable battery tester based on this concept. This preliminary modeling approach and test equipment design requires further refinements before actual implementation. The range of battery types to be tested, and the voltage and current levels that the tester must accommodate will have to be considered.

TABLE 7-4. BATTERY TEST SYSTEM COST ESTIMATE

ITEM	COST (1980 \$)
<u>Small-Signal Tester</u>	
HP5420A Waveform Analyzer	30,000
Plotter	5,000
Drive Circuit & Connections (Small Signal)	1,500
Voltmeter	250
Ammeter	250
Shunt	100
Connecting Power Cables	100
Carrying Cases	<u>200</u>
	37,400
<u>Static VI Tester</u>	
Load Resistors	2,000
Transistor Switches & Heatsinks	2,500
Drive Circuits	1,000
Cabinet	200
Instruments	<u>2,000</u>
	7,700
Assembly	10,000
Test	2,000
Procedures & Manuals	<u>6,000</u>
TOTAL	<u>\$63,100</u>
(Excludes G&A and Fee)	

Summary

Efforts conducted under this task have shown that, although there is much published information concerning advanced batteries, few details are given regarding equivalent circuit models or electrical protection requirements for these systems. A survey of five advanced battery manufacturers yielded some additional information, but these areas need additional attention before batteries and converters can be combined into reliable energy storage systems.

A preliminary battery modeling approach was defined in this task. Also, a preliminary design was developed for portable test equipment required to obtain the data required to construct an equivalent circuit model by this approach. This battery tester makes use of commercially available hardware wherever possible. Further effort will be needed to refine both the modeling technique and the test equipment design, although initial trials demonstrated the method's feasibility.

Experience with the proposed test equipment indicated that the test equipment was readily set up, the equipment was quick and easy to use and the results were very creditable.

Based on the relative success to date, and the lack of information required to produce models of advanced batteries, it is recommended that appropriate testing be included in the advanced battery program to determine battery modeling information.

Section 8

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APPENDIX 1 - LOGIC SUBSYSTEM SPECIFICATION FOR DEPARTMENT OF
ENERGY ADVANCED CONVERTER

APPENDIX 2 - LITERATURE SEARCH BIBLIOGRAPHY

APPENDIX 3 - ENERGY STORAGE BATTERY QUESTIONS

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CORPORATION'S 1976 SURVEY AND TO THE HITTMAN REPORT

APPENDIX 1

LOGIC SUBSYSTEM SPECIFICATION FOR DOE ADVANCED CONVERTER

FCR-2072

Prepared for
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1.0 SCOPE AND OBJECTIVES

1.1 Scope

This specification establishes the requirements for the logic and control subsystem for an advanced self-commutated multi-bridge converter being designed under DOE Contract AC01-79ET-29079. This 14 MW converter was originally defined under EPRI 841-1 and is being refined under DOE AC01-79ET-29079 for the storage battery application. The design should also be applicable to fuel cell input and alternate power circuit considerations. The logic design of the current 4.8MW Fuel Cell Demonstrator Inverter was used as background for this effort.

1.2 Objectives

The overall objective of this specification is to describe the required characteristics of an advanced logic subsystem using large and very large scale advanced digital logic elements to meet the system specifications. Specific objectives are: (1) Provide at least a 75% reduction in the number of components performing the same functions in the 4.8MW design. (2) Achieve lower cost, reduced size and improved reliability. (3) Provide a more flexible system with the ability to incorporate additional operating features and alternative system configurations with programming software changes and minimal hardware additions. (4) Design to permit simplified maintenance utilizing self-checking during operation or test and use simple diagnostic displays to identify failed functions.

2.0 14-MW CONVERTER PERFORMANCE

The controls shall provide the following performance when installed in the 14-MW converter system.

2.1 Utility Line Conditions

Line Voltage Level	13.8 kV design point (capable of being designed for line voltage levels of 12 to 69 kV).
--------------------	--

2.1.1 Converter Operating Range -

Average Voltage $\pm 5\%$	Full MVA
-5% to -20%	85% of rated
+5% to +10%	85% of rated
Line/Line Voltage Unbalance	
<2%	Full MVA
2% to 5%	75% of rated

2.2 Converter DC Terminals

Non-Operating Max. voltage at terminals 4500

Operating

Max. Voltage at Terminals 3740

Min. Voltage at Terminals 2200

Voltage/current Envelope See Figures 1 and 2.

2.3 Converter AC Terminals

Phases 3

Wires 3

Frequency, Hz 60 Hz nominal (will operate between 57 and 61 Hz.)

Max. apparent Power $14 \text{ MVA} = \sqrt{\text{MW}^2 + \text{Mvar}^2}$

Max. Real Power $\pm 14 \text{ MW}$

Max. Reactive Power (MVAR) $\pm 14 \text{ Mvar}$

Max. Current Delivered Under Fault Conditions 110% of rated on an rms basis integrated over one cycle.

Harmonic Voltages No single converter-generated harmonic >3% and total converter-generated harmonic distortion less than 5%.

2.4 Converter Modes

2.4.1 Standby - Breakers and disconnects open, unlocked and operative.

This mode occurs:

- (1) On command from site controller.
- (2) When protection circuits detect specific abnormal conditions.
- (3) When the converter remains interrupted for more than 15 seconds.
- (4) When there are more than two interrupts in 15 seconds or 6 interrupts in 2 minutes.

2.4.2 Operating - There are three operating states:

- (1) Charge batteries as dispatched by site controller
- (2) Supply power to line from battery or fuel cell as dispatched by site controller.
- (3) Var only: Supply vars to line as dispatched by site controller. The dc source disconnect is open and the line supplies converter losses.

2.4.3 Interrupt - Converter is off, but breakers and disconnects closed. Shunt load is connected during the interrupt for the fuel cell case.

This mode occurs when specific protection limits are exceeded. Converter is programmed to restart once parameters are within operating limits. The protection limits which cause interrupts are d.c. bus voltage outside limits, pole current too high, line voltage outside limits and line frequency outside limits.

2.5 Design Life

No material or design shall limit life to less than 20 years.

2.6 Response

Power response can be programmed to change from no load to full load for any time between 100 milliseconds to 20 seconds.

Var response can be programmed to change from no vars to maximum vars for any time between 300 milliseconds and 20 seconds.

2.7 Maintenance Goals

The minimum interval between failures is 20,000 hours with repair time less than 4 hours.

This mean time between preventive maintenance is 8600 hours with maintenance time to be 1 hour or less.

2.8 Accuracy of Sensing and Control

The overall accuracy of control and protection sensing shall be $\pm 1\%$ of full range with the following exceptions:

- (1) Real power accuracy is ± 170 kW minimum.
- (2) Reactive power accuracy is $\pm 3\%$ of full MVA.
- (3) Timing of sequences is $\pm 0.1\%$.
- (4) Accuracy of abnormal frequency protection is ± 0.1 Hz.
- (5) Tripping accuracy due to line voltage transients is $\pm 5\%$.

Fig 1. Representative Battery Operating Cycle Envelope-Steady State

Fig 2. Representative Fuel Cell Operating Envelope-Steady State

3.0 SECTION DEFINITIONS

3.1 Subsystem Block Diagrams

Figure 3 depicts several logic functions that exist implicitly independent of the type of logic elements used.

Figure 3. Logic and Controls Subsystem (Functional)

3.2 Basic Converter Control Section

The function of this section is to provide switching commands for the power pole thyristors in the proper sequence to generate the required output waveform for real and reactive power flow.

3.2.1 Thyristor Gate Drive Subsection -

- o Function - The gate drives convert logic level switch commands from the sequencer to the power level required to drive the thyristor gates.
- o Inputs - The inputs are logic level switch commands from the sequencer subsection.
- o Outputs - The outputs are gating signals to the thyristor interface circuits located in the converter.

3.2.2 Sequencer Subsection -

- o Function - The sequencer translates the waveform pattern produced by the waveform generator into a fixed sequence of switching commands that are sent to the gate drives. The sequence of the switching commands controls the timing of the thyristor gates. A subsequent change the state of a power pole is inhibited until the previous sequence of switch commands has been completed.
- o Inputs - The inputs are modulated waveform patterns from the waveform generator and a start/stop command.
- o Outputs - The outputs are logic level switch commands that are sent to the gate drives.

3.2.3 Waveform Generation Subsection -

- o Function - The waveform generator produces a pulse width modulated waveform pattern in response to signals from voltage and phase difference controls. Figure 4 shows an edge notch pattern. Note that the minimum requested modulation pulse width is much greater than the minimum pole switching time established by the sequencer to prevent the waveform distortion.
- o Inputs - The inputs are signals from the voltage and phase controls.
- o Outputs - The outputs are modulated waveform patterns to the sequencer subsection via the circulating dc current control subsection.

3.2.4 Circulating DC Current Control Subsection -

- o Function - This circuit measures dc current flowing in the output of the converter bridges and then reduces this current by modifying the modulation pattern supplied to the gate sequencer. The modified pattern delays the rising and falling edges of the waveform by different amounts to introduce a small dc voltage which limits circulating current to less than 1% rated ac output. Refer to Appendix B for a description of requirements for limiting dc unbalance current flow.
- o Inputs - The inputs are dc current signals from the output of the converter bridges and modulated waveform patterns from the waveform generator
- o Outputs - Outputs are modified waveform patterns to the sequencer subsection

RELATIVE MAGNITUDE OF HARMONIC VOLTAGES

NOTCH ANGLE (θ)	FUNDAMENTAL VOLTS	3rd HARMONIC VOLTS	5th HARMONIC VOLTS
0°	1.0	0.333	0.2
6°	0.989	0.301	0.146
24°	0.827	-0.127	-0.4
48°	0.338	-0.873	-0.4
60°	0.0	-1.0	0.0

WHERE $V = (2 \cos N \theta - 1) / N$

WHERE $N = \text{HARMONIC (1 FOR FUNDAMENTAL)}$
 $= 1, 3, 5, 7, (2K-1)$

45-23

Figure 4. Modulation Patterns

3.3 Power and Var Regulation and System Sequencing Section

The function of this section is to:

- (1) Sequence the converter through operating modes on request from supervisory control, local control, or converter protection logic.
- (2) Regulate watts and vars based on supervisory control or local control request by sending signals to basic converter control.

3.3.1 Power and Var Regulation Subsection - The function of this subsection is to regulate real and reactive power by sending phase and voltage signals to the basic converter control in response to power requests from the supervisory or local control. This subsection consists of the voltage and phase difference controls and power and var regulators.

o Voltage Control

Function - The voltage control delivers a voltage signal to the Basic Converter Control in response to signals from the regulator. A description of 4.8-MW logic voltage control range is included in Appendix A.

Inputs - The inputs are an error signal from regulator, a set signal from sequencer, line volts, and converter dc volts.

Outputs - The voltage controller delivers a percent fundamental signal to the Basic Converter Control.

Operation - The voltage controller computes the fundamental voltage to be delivered by power poles to provide the required difference between converter bridge outputs and the utility line. When an error signal from the regulator is present, the voltage difference is changed until the error signal disappears. The voltage control holds the new voltage difference when error input is zero.

o Phase Control

Function - The phase controller modifies output power by providing the basic control with phase reference voltages to offset converter bridge output phase with respect to the line phase in response to requests from the regulator. A description of the 4.8-MW phase control range is described in Appendix A.

Inputs - The phase control inputs are an error signal from regulator, line voltage representations and a set signal from the sequencer.

Outputs - The control supplies reference voltages for converter bridge output at a phase difference with respect to the measured zero crossings of the line.

Operation - When an error signal is received from the regulator, the phase difference changes. The phase difference is fixed when the error signal from the regulator returns to zero.

o Power and Var Regulator

Function - The power and var regulator sends power and var request signals to the phase and voltage controllers. These signals are determined by computing actual power and vars and subtracting these values from modified supervisory control requests.

Inputs - The inputs are signals from the power and var modification subsection, and line voltage and current representations.

Outputs - The measured power difference is supplied primarily to the phase difference controller. Var difference is supplied primarily to the voltage difference control. Measured watts and vars are available for system monitoring.

Operation - The power and vars produced by the converter are computed and subtracted from the modified site control requests.

3.3.2 Power and Var Modification Subsection -

o Function - The power and var modification logic modifies supervisory control power requests to keep the converter within its operating limits.

o Inputs - The inputs are line volts, power, vars, and dc voltage.

o Outputs - Modified power and var requests to the power and var regulator.

o Operation - 'Slewing rate' functions limit the rate of change of power and var request signals supplied to the regulator. Var requests are limited by power level to hold the converter to rated MVA. MVA requests are limited when source or line parameters are outside full rating limits.

3.3.3 Sequencing Subsection - The function of sequencing is to sequence the on/off controls of the converter and its peripherals through startup, stop, and shutdown in response to the status of system parameters, program timers, and supervisory or local control panel requests.

A typical automatic start sequence is:

A. Initial Conditions

1. The logic is running.
2. Safety locks are removed and mechanical isolators closed.
3. Alarms are reset.
4. If no problems exist, converter ready signal is sent to site controller.

B. Startup sequence - converter mode

1. The site controller issues command to start in a particular mode.
2. The dc bus gets charged until the dc voltage matches the voltage of the source (Battery or Fuel Cell).
3. When the proper voltage level is reached, the sequencer connects the source to the converter by means of a motorized disconnect.
4. The ac breaker is closed.
5. The converter is turned on at an initial condition of phase and voltage difference with respect to the line.
6. After a delay to allow any startup transient to decay the sequencer allows the phase and voltage controls to bring the converter to its requested power level, at a fixed rate of change.

C. Startup Sequence - Var only mode

1. If var only operating mode is selected, there is no dc source connected.
2. Transition can be made from var only to converter mode by matching dc link and battery voltages, closing disconnect and then going to requested power.

D. Interrupt sequence

1. A protective circuit detects a parameter out of limit.
2. The converter is halted.
3. A shunt load may be connected to hold dc voltage within limits for starting converter with fuel cell source.
4. The logic checks if parameters are back within limits. When all parameters are OK the converter is restarted at initial conditions and then returns to requested power at a fixed rate.

5. Parameters checked could include dc and ac voltages and commutation capacitor voltages.

E. Go to standby

The converter is turned off. Switchgear is opened and other peripherals are turned off.

3.3.4 Operation With Local Control - The local control emulates the site controller for normal operation, and also has selectable test modes to check out the converter, logic and peripherals at zero or reduced power and voltage. Typical tests under local control would be verification of system sequencing and checking thyristor gate drives. Manual single stepping through the startup sequence is also used in checking functions. Protective functions such as ac or dc under-voltage are disabled by software during low-level testing to eliminate the need to install hardware bypasses.

3.4 Protection

The protection circuits prevent or limit damage to the converter and source. The protection covered here does not include features normally part of a system component such as a breaker.

3.4.1 Source Protection - The converter shall be interrupted for the following reasons:

- o DC under and overvoltage

If an under or overvoltage occurs while the converter is running, it is interrupted, otherwise it is inhibited from starting.

The source to converter disconnect shall be interlocked such that an open disconnect cannot close if voltage difference is out of limits, and a closed device shall not be opened if current is above a safe level. A high current interruptor shall be provided, which shall activate itself if current remains above the capability of the disconnect.

- o The converter shall go to standby when:

1. The shunt load is on for more than 15 seconds. (Fuel Cell)
2. Shunt load overtemperature is experienced. (Fuel Cell)
3. The high current dc interruptor actuates.

3.4.2 Utility Line Protection -

- o The converter shall be interrupted for the following reasons:

1. Line voltage greater than 10% above nominal.
2. Line voltage of less than 20% below nominal

This interrupt is on an inverse time basis between -20% and -50% of line, and instantaneous below 50%.

3. Line voltage between phases differs by more than 5%.
 4. A line voltage impulse (of up to 50 microseconds) of greater than 1.4 times peak of nominal wave. Line impulses between 1.1 and 1.4 reduce overcurrent setting linearly to 1 per unit.
- o The converter shall go to standby when:
 1. There are three interrupts in 15 seconds or 6 interrupts in 2 minutes.
 2. There is a interrupt of greater than 15 seconds.
 3. The output magnetics differential protection detects a fault.
 4. The AC line contactor trips open.

3.4.3 Converter Protection -

- o The converter shall be interrupted for the following reason:

The magnitude of any pole current exceeds the comparison point.

- o The converter shall go to standby on the loss of any of the following:

The air for cooling or the cooling air sensor.

A TBD number of dc bus filter capacitors.

A pole or output fuse.

The communication to the site-controller.

The line synchronization signal.

The critical (UPS) bus

Any logic power supply voltage.

o Protection Reset

Almost all go to standby conditions require inspection of the power conditioner system and thus cannot be remotely reset. The only go to standby conditions which can be remotely reset are those due to:

- (a) Multiple interrupts
- (b) Shunt load on for greater than 15 seconds
- (c) Improper mode selection

3.5 Logic Power Supply

The power supply provides regulated dc voltages for all functions to run the converter from the site or remote controller. The supply is normally operated from the UPS (Uninterruptable Power Supply). Switching type power supplies are preferred because of their lower losses and size.

The mean time between failure (MTBF) shall be greater than 30,000 hours. The MTBF shall be achieved using redundant supplies for each dc voltage required. The following rules shall be followed in the design:

- (1) Loss of any single supply of a redundant pair shall result in a warning being issued.
- (2) Loss of any supply voltage shall generate a go to standby signal for the converter supply.
- (3) A manual logic reset shall be required on power-up or after loss of a critical bus.
- (4) The power supplies shall start automatically when critical power is supplied (UPS).
- (5) The diagnostics and local control shall have separate power supplies for functions not classified as critical converter protection.
- (6) The power supply input shall be evenly distributed across three phases of UPS bus.

The dc voltage regulation is based on specific current control requirements or $\pm 5\%$ whichever is less.

- (7) Storage capacitance on dc voltages is required for safe shutdown of the converter on loss of the UPS.

3.6 Local Control and Display

The logic shall include an integral local control/display panel to allow local control of the converter and local display of operating parameters.

Display - The following parameters shall be displayed. The metering signals for these displays shall be independent of control signals for the same parameters.

- o Converter status
- o Converter dc volts
- o Converter dc amps
- o Vars
- o Watts
- o Notch (or percent modulation)
- o Phase angle between converter and line
- o Sequencer step and mode of operation
- o AC Line volts - 3 phases, high side
- o AC Line amperes - 3 phases, high side
- o Source or battery current

Local Control - The local control shall provide control capability for the following parameters:

- o Adjust power and vars
- o Adjust voltage and phase differences for line parallel unregulated operation
- o Select operating or checkout mode
- o Select start go to standby
- o Select interrupt run converter
- o Enable single step advance through checkout sequence

3.7 Diagnostics

The logic shall contain its own diagnostic capability for monitoring converter status with external instrumentation, and for recording system out-of-limit conditions and converter and system faults to facilitate maintenance and repair.

The analog and digital data produced by the diagnostics shall be available for local or remote analysis or display. The diagnostics shall include a non-volatile storage medium with readout connection for external access. Diagnostics data shall be accessed without affecting performance of the converter

3.8 System Interfacing

The interface between the logic and rest of the system shall be as follows:

3.8.1 Supervisory Control - All input-output between logic and site supervisory control shall be in digital form. The format shall be the presently used RS-232C or the newer RS-366-A depending on individual installation requirements. At least two full duplex paths should be used for reliability and to allow transmitting data independent of converter operation. Adequate surge protection and/or isolation shall be provided on signal lines to prevent damage to the logic input device.

3.8.2 Peripherals - Input/Output between logic and system equipment such as switchgear, metering transformers, etc, may be in either digital (status) or analog form. Input-output between logic and external equipment must be isolated.

o Status (Digital) signals

Solid-state optical couplers are the preferred means of isolation for status signals. Different couplers shall be installed depending on the requirements of the peripheral.

o Analog Signals

No voltage greater than 120 volts ac shall be brought into the logic enclosure. Signal lines shall have one side grounded at the source. All dc analog signal leads coming from the converter or peripherals should be impedance limited and surge protected.

3.8.3 Local Control and Display -

All input-output between the logic and the local control and display is in digital form. Signal format should be the same as the supervisory links.

3.8.4 Diagnostics -

Same type input-output as local control

3.8.5 Gating -

Defined under gating description in Appendix A.

4.0 OTHER GUIDELINES

4.1 Mechanical Designs

Power Supply - Switching type power supplies shall be used.

The power supplies may be separated in the cabinet from the logic for cooling purposes.

Cabinet - The cabinet construction shall conform to indoor operation of industrial equipment. The logic cabinet shall be designed for free standing floor mounting with all cables leaving through the bottom. Provision shall be made for crane and forklift moving. Liftings lugs shall be provided.

All doors and cable exits shall be gasketed to limit entrance of dirt into the cabinet. The cabinet shall be of metal construction with doors and panels electrically bonded to the internal logic ground bus. All doors shall incorporate EMI gaskets to assure EMI shielding.

Circuit Boards - Logic cards shall be conformal coated. Circuit boards shall be double sided, 2 oz copper, G10 material. All connector fingers shall be nickel passivated, gold plated. All traces shall have a tin/lead overcoat. Plated through holes are required. Unused areas shall be solder masked.

Component designations shall be labeled on both sides of the boards. At least 3 connector pins on each side of the board shall be labeled.

The connectors and cards shall be compatible noble metal plated.

Cards shall be routed to form the connector insert using a reference point adjacent to the connector.

Card guides and connectors shall be mounted to tolerances which assure proper alignment of card fingers and socket contacts. Card ejectors shall be provided.

The number of interconnections shall be minimized by using large area logic cards.

Connectors - To make equipment servicable, all wiring between subassemblies (card racks, panels, etc.) shall include connectors.

Interconnecting cables shall use plugs and sockets capable of withstanding vibration and abuse. Contacts shall be noble metal plated.

The card connectors shall be low insertion pressure type with at least two contact fingers per card pad.

A single point ground bus shall be incorporated. All card racks shall establish a dc logic common return point to the bus at a point of reasonable proximity to the card rack.

Isolation of High Level and Low Level Wiring - AC power and other high level signals shall be physically isolated from low level signal wiring by routing in separate bundles and other appropriate means.

Servicability - All subassemblies shall be designed for ease of removal and shall have access via doors or removable panels. Circuit boards shall have front access so that they can be easily removed. Card rack backplane wiring shall be accessible. Card racks and other subassemblies shall include test connectors for hookup of external diagnostic equipment.

Local Control Panel - Local control panels and displays that are not part of a permanent installation may be less rugged in design. Standard computer type hardware may be used for these functions.

Safety screens shall be provided for cathode ray tubes.

Hardware Installation - All connectors shall be installed using vendor recommended tools to assure reliable operation.

All stripping of insulation shall be done with the proper tools to avoid damaging conductors and assure proper contact.

Screws and nuts for holding panels and doors closed should be captive to avoid loss during maintenance or repair.

4.2 Environmental Requirements

The logic enclosure is designed for indoor use. However, added sealing may be required where corrosive producing material is in air.

The logic shall be designed to operate in an ambient air temperature of 10°F to 120°F.

Accuracy of control and protection parameters are specified for an ambient temperature range of 32°F to 110°F (0° - 40°C).

Switching type logic power supplies shall incorporate adequate filtering to limit interference with operation of logic and controls.

4.3 Testing and Acceptance of Logic

The logic components and cabinet wiring shall be tested and a functional acceptance test shall demonstrate the operation of the logic using simulated signals. Final acceptance shall depend on demonstration of correct operation on a model system.

Documentation shall include schematics, mechanical and electrical assembly drawings, parts lists, component design specifications, all software programs and algorithms, PC board artwork, real-size negatives, and PC board assembly drawings.

Instruction and maintenance manuals shall be provided, which shall include sufficient data to completely define all user operating requirements and user maintenance requirements. Reference to manufacturers' manuals of components purchased by the logic and controls vendor is permissible.

APPENDIX A VOLTAGE AND PHASE CONTROL RANGE FOR CONVERTER OPERATION

The following assumptions have been included with converter performance requirements in order to determine voltage and phase control range.

The series inductive reactance is about 22%.

The series resistance of the converter output and transformer circuits is less than 3% because converter efficiency is greater than 96% at full load.

When source and line voltages are fixed, the full range of power variation is achieved by a ± 12 degree phase change and the full range of lagging and leading VARs is achieved by a 23% voltage control variation. The actual source and line voltages are not fixed, however, and when the 1.7/1 source variation and the -20% to +10% line variation are taken into account, the actual phase and voltage control ranges must be ± 15 degrees and 3 to 1, respectively.

The fundamental output voltage is varied by edge notch modulation¹ according to the following relation.

$$\text{Fundamental voltage} = 2 \cos (\text{notch}) - 1$$

The notch varies from 6° to 49° , due to power pole switching time limits.

¹ 'Edgenotch' modulation refers to a scheme where the leading and trailing pulses in a pulse width modulated waveform are varied in width.

APPENDIX B REQUIREMENTS FOR LIMITING DC UNBALANCED CURRENT FLOW

DC currents are present in the output of a converter pole due to differences in forward drops in the semiconductors. The currents must be held to less than 1% of rated ac output to avoid saturation of magnetic devices. While it is true that the main transformer will receive ampere turns from the line instead of saturating, the resultant even harmonic line currents may be higher than the permissible distortion.

The large converters have efficiencies in excess of 96%. Therefore the output resistance seen by the power poles must be about 2% or less. The correction in dc current by voltage control is thus $< 1\%$ of 2% or $< .02\%$. DC current is corrected by changing pole output voltage. Voltage control is accomplished by advancing or retarding one or more of the switch points of the pole during a cycle. For 60 Hz operation 1% current correction can be accomplished by a waveform change for one switch point of 3 microseconds per cycle. A change of one microsecond on 3 switches produces the same correction.

The source of dc unbalance, the difference in forward drops of the semiconductors could be as high as 1 volt. This is 0.5% at a dc bus voltage of 2000 volts. This suggests that a correction range of ± 12 microseconds is required to handle the normal spread of conditions.

For an output impedance of 22% with the inductors between the poles and the rest of the magnetics, the per unit inductance is $.22/377 = 5.8 \times 10^{-4}$. With a .05% voltage difference the change in current over one cycle is $.05\%/5.8 \times 10^{-4} \times .01667 = 1.4\%$. A granularity as high as 3 microseconds appears to be adequate for controlling dc unbalance currents.

The minimum change of 3 microseconds produces a correction of 1.4% in 3 cycles. The rate of current change is slow enough to allow dc measurement over more than one cycle in order to filter out the ac load current.

APPENDIX 2

LITERATURE SEARCH BIBLIOGRAPHY

- I. Battery Characteristics
- II. Equivalent Circuit Modeling

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APPENDIX 3
ENERGY STORAGE BATTERY QUESTIONS
September 1979

United Technologies Corporation
United States Department of Energy
Contract DE-AC01-79ET-29079

ENERGY STORAGE BATTERY QUESTIONS

We kindly request your assistance in answering the following questions regarding the advanced battery you are developing for electric utility energy storage applications. Your participation was suggested by the United States Department of Energy (DOE), as part of DOE contract DE-AC01-79ET-29079, "A Program to Develop Advanced Converter Technology for Battery Applications" with United Technologies Corporation. This information is needed to define the battery/ converter interface requirements for advanced battery energy storage systems that will operate on utility networks.

The objective of this task is to determine the electrical characteristics of advanced batteries and develop a preliminary equivalent circuit model that represents their steady-state and transient response. These characteristics and models will be used to allow matching of battery and converter characteristics for best overall efficiency and maximum power transfer in utility energy storage applications. In addition, the program will define the preliminary design for portable test equipment that can be used to obtain data required to model battery characteristics.

Please provide the answers to the following questions on a per-cell basis (except where noted) and extrapolate to the full-scale production design where possible.

Specify the type and size of the cell used as the basis for answering these questions.

I. Voltage/Current Characteristics

This information will establish the electrical parameters (such as voltage range) required for converter system design and optimization.

1. On a separate sheet, show the constant-power voltage and current profiles vs. time for a 7-hour charge, 5-hour discharge operating cycle. These curves should represent values experienced in actual cycling of a cell; i.e., they should account for cell efficiency. Indicate the effects of aging on cell performance by showing beginning-of-life and end-of-life values, including the effects of cell failures, and state the design life _____ years or _____ cycles.
2. (a) If constant-power data is not available, or if that mode of operation is not desirable, explain why not and give the preferred mode plus its V/I vs. t curves as in 1 above.
- (b) If 7-hour charge, 5-hour discharge cycle data is not available, provide cycle data that is available and give an assessment of the significance of operation for the requested cycle times.
3. What are the maximum charge voltage and minimum discharge voltage for this operating cycle, plus their expected tolerance for production cells?

	<u>Beginning of Life</u>	<u>End of Life</u>
Maximum potential (V)	_____	_____
Tolerance ($\pm$ mV)	_____	_____
Minimum potential (V)	_____	_____
Tolerance ($\pm$ mV)	_____	_____

4. Describe any special or abnormal voltage or current characteristics that occur at the end of charge or discharge, or during the transition between charge and discharge (e.g., taper charge or discharge to zero voltage).
5. What test techniques were utilized to obtain the above steady-state operating characteristics?

II. Efficiency and Capacity

This section provides data for establishing system size and cycle efficiency, and helps determine the requirements for battery test equipment.

1. What are the per-cell design values for:

	<u>Beginning of Life</u>	<u>End of Life</u>
Ampere-hour efficiency	_____ %	_____ %
Watt-hour efficiency	_____ %	_____ %
Capacity (watt-hours)	_____	_____
Capacity (ampere-hours)	_____	_____

III. Battery Protection

The following information will help define the requirements for protecting the battery energy storage system components, and will facilitate the design of battery test equipment.

1. Graphically describe the cell's bolted fault characteristic (current vs. time).
2. How long can the cell tolerate (without damage) a bolted fault (e.g., how much time for a specified percentage overcurrent)?

3. What are the maximum values of voltage and current a cell can withstand?

$V_{\max}$ _____ volts
 $I_{\max}$ _____ amperes

4. What are the maximum ripple current and voltage permissible for this cell design?

Ripple current _____ mA (or _____ %)
Ripple voltage _____ mV (or _____ %)

5. How was the data for this section obtained (e.g., describe the test scheme or analysis used)?

IV. Battery Arrangement

Information regarding battery system arrangement is required for system design, protection studies, and loss projections.

1. Sketch the envisioned series/parallel arrangement of cells for a 100-MWhr battery system.

2. What is the maximum voltage allowable for a series cell arrangement?

3. What size single-cell or multi-cell test rigs are utilized for steady-state and transient testing, to which a battery test system could be interfaced?
4. Show the number, type, size, and construction of proposed intercell and intermodule connectors for the battery system. Also, list their electrical resistance and inductance.

V. Equivalent Circuit Models

The use of equivalent circuit models will aid in studies of protection coordination and system response; also, this data will help determine the requirements for and design of battery test equipment.

1. Show a single-cell equivalent circuit model that represents its transient electrical characteristics.
2. Show a battery system equivalent circuit.
3. How were these models derived (e.g., specify the type of analysis or tests)?

Thank you for your participation.

APPENDIX 4

COMPARISON OF 1979 SURVEY RESULTS TO UTC'S 1976
SURVEY AND TO THE HITTMAN REPORT

BY	R. ROSATI		TITLE	BATTERY SURVEY SUMMARY		YEAR	SERIES	JOB NUMBER
DATE	12/10/79		BATTERY TYPE :	LEAD/ACID				DOE
MODEL			MANUFACTURER :	C & D Batteries		PAGE		

PARAMETER (PER CELL)	DATA SOURCE		
	1976 UTC SURVEY	1979 UTC SURVEY	HITTMAN REPORT
CYCLE TYPE	NOTE : ESB data 7-hr chg / 5-hr dischg const. power	8-hr chg / 4.8-hr dischg ↑ const. voltage ↑ const. power	
V _{MAX} (BOL)	2.33	2.6	2.6 - 2.7
V _{MIN} (BOL)	1.64	1.7	1.6 - 1.7
VOLTAGE RATIO (BOL)	1.42	1.53 ^{MAX V/R}	1.5 - 1.6
V _{MAX} (EOL)		2.45	
V _{MIN} (EOL)		1.7	
VOLTAGE RATIO (EOL)		1.44	
V _{WITHSTAND}		2.8 ✓	
I _{WITHSTAND}		20,000 A	
V _{RIPPLE} (MAX)		5-10%	
I _{RIPPLE} (MAX)		NA	
I _{FAULT} (PER UNIT)	>40 p.u. (40,000 A @ .04 sec)	>100 p.u. (77,000 A @ 1 sec)	
OPERATING TEMP.		~ 25 °C	
EFFECT OF TEMP. ON PERFORMANCE		relatively well known (see literature)

UNITED
TECHNOLOGIES
POWER SYSTEMS DIVISION

ENGINEERING CALCULATION SHEET

BY	R. ROSATI	TITLE	BATTERY SURVEY SUMMARY		YEAR	SERIES	JOB NUMBER
DATE	12/10/79	BATTERY TYPE : ZINC/BROMINE					DOE
MODEL		MANUFACTURER : GOULD			PAGE		
PARAMETER (PER CELL)		DATA SOURCE					
		1976 UTC SURVEY	1979 UTC SURVEY	HITTMAN REPORT			
CYCLE TYPE		NOT SURVEYED	4-hr chg./4-hr. dischg. Const. Current	5-hr chg./5-hr dischg. Const. Current			
V _{MAX} (BOL)			2.0	1.95 - 2.00			
V _{MIN} (BOL)			1.5	1.00 - 1.30			
VOLTAGE RATIO (BOL)			1.33	~ 1.7			
V _{MAX} (EOL)			2.05				
V _{MIN} (EOL)			1.45				
VOLTAGE RATIO (EOL)			1.41	MAX. V/R			
V _{WITHSTAND}							
I _{WITHSTAND}			self-limits at 5 pu. fault current				
V _{RIPPLE} (MAX)							
I _{RIPPLE} (MAX)							
I _{FAULT} (PER UNIT)			~ 5 pu.				
OPERATING TEMP.				20-60°C			
EFFECT OF TEMP ON PERFORMANCE							

BY	R. ROSATI	TITLE	BATTERY SURVEY SUMMARY		YEAR	SERIES	JOB NUMBER
DATE	12/10/79	BATTERY TYPE :		SODIUM / SULFUR			DOE
MODEL		MANUFACTURER :		GENERAL ELECTRIC CO.	PAGE		

PARAMETER (PER CELL)	DATA SOURCE		
	1976 UTC SURVEY	1979 UTC SURVEY	HITTMAN REPORT
CYCLE TYPE	7-hr. chg./5-hr. dischg.	7-hr. chg./5-hr. dischg. Const. Current	5-hr. chg./3-hr. dischg. Const. Current
V _{MAX} (BOL)	2.314	2.287	2.4
V _{MIN} (BOL)	1.373	1.586	1.6
VOLTAGE RATIO (BOL)	1.68	1.44	1.50
V _{MAX} (EOL)		2.397	
V _{MIN} (EOL)		1.440	
VOLTAGE RATIO (EOL)		1.66 ^{MAX} V/R	
V _{WITHSTAND}		3.5	
I _{WITHSTAND}		86.2 A	
V _{RIPPLE} (MAX)		29.8 mV (BOL) 44.6 mV (EOL)	
I _{RIPPLE} (MAX)		2.466 A	
I _{FAULT} (PER UNIT)		4 p.u. instantaneous rising to ~10 p.u. in 180 seconds	
OPERATING TEMP.		330° C.	300-400° C
EFFECT OF TEMP. ON PERFORMANCE			

BY	R. ROSATI	TITLE	BATTERY SURVEY SUMMARY	YEAR	SERIES	JOB NUMBER
DATE	12/10/79	BATTERY TYPE :	ZINC/CHLORINE			DOE
MODEL		MANUFACTURER :	EDA	PAGE		

PARAMETER (PER CELL)	DATA SOURCE		
	1976 UTC SURVEY	1979 UTC SURVEY	HITTMAN REPORT
CYCLE TYPE	5-hr. chg./5-hr. disch. CONST. POWER?	7-hr chg./5-hr disch. CONST. CURRENT	CONST. CURRENT CHARGE
V _{MAX} (BOL)	2.23	2.3	2.28
V _{MIN} (BOL)	1.80	1.6	1.92
VOLTAGE RATIO (BOL)	1.24	1.44	1.19
V _{MAX} (EOL)		2.35	
V _{MIN} (EOL)		(assume 1.6)	
VOLTAGE RATIO (EOL)		<div style="border: 1px solid black; padding: 2px;">1.47</div> MAX V/R	
V _{WITHSTAND}			
I _{WITHSTAND}		6 p.u.	
V _{RIPPLE} (MAX)			
I _{RIPPLE} (MAX)		> 10%	
I _{FAULT} (PER UNIT)		30 p.u.	
OPERATING TEMP.			5°-60°C
EFFECT OF TEMP. ON PERFORMANCE

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ENGINEERING CALCULATION SHEET

BY	R. ROSATI	TITLE	BATTERY SURVEY SUMMARY		YEAR	SERIES	JOB NUMBER
DATE	12/10/79	BATTERY TYPE : LITHIUM/METAL SULFIDE					DOE
MODEL		MANUFACTURER : ARGONNE NAT'L LAB.		PAGE			
PARAMETER (PER CELL)		DATA SOURCE					
		1976 UTC SURVEY	1979 UTC SURVEY	HITTMAN REPORT			
CYCLE TYPE		10-hr chg./10-hr. disch. Const. Power	No Data Given (maybe see '76 survey)	7-hr chg. (data incomplete)			
V _{MAX} (BOL)		1.6	1.6	1.6			
V _{MIN} (BOL)		1.0	1.0	.9-1.0			
VOLTAGE RATIO (BOL)		~ 1.6	1.6	1.6-1.8			
V _{MAX} (EOL)			1.6				
V _{MIN} (EOL)			0.8				
VOLTAGE RATIO (EOL)			2.0	MAX V/R			
V _{WITHSTAND}		2.0	1.65				
I _{WITHSTAND}		100 A					
V _{RIPPLE} (MAX)		} RIPPLE HAS LITTLE EFFECT ON PERFORMANCE					
I _{RIPPLE} (MAX)							
I _{FAULT} (PER UNIT)		~ 2 x rated					
OPERATING TEMP.		450°C		400-500°C			
EFFECT OF TEMP. ON PERFORMANCE		+ 25°C - 475°C no effect on perf.					

A4-5

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ADVANCED CONVERTER TECHNOLOGY

Technical Progress Report

for Period

May 23, 1979 through May 22, 1980

FCR-2210

Prepared for the

U.S. Department of Energy

Project Manager Dietrich Roesler

Under Contract DE-ACO1-79ET29079

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In reply please refer
to: FCR-2210

August 19, 1981

Chief Publishing Branch
U.S. Department of Energy - TIC
P.O. Box 62
Oak Ridge, TN 37830

Attention: Mr. James N. Holt,
Chief Publishing Branch Officer

Subject: Contract No. DE-AC-01-79ET29079

Reference: Technical Progress Report, FCR-2210,
Submitted on July 24, 1981

In the above referenced report we mistakenly used internal data sheets for pages A4-1 through A4-5. These internal data sheets include a proprietary notice which is not applicable to this document. I have enclosed the revised pages with the notice deleted.

I have also enclosed a title page which removes the patent notice as we now have DOE patent approval.

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July 28, 1981

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Attention: Mr. Dietrich Roesler, ET EES, Mail Stop 3344

Subject: Data Submittal, Technical Progress Report FCR-2210

Reference: (1) Contract No. DE-AC-01-79ET29079
(2) Draft Technical Progress Report, FCR-2210,
Submitted on January 23, 1981

The U. S. Department of Energy Patent Counsel has now reviewed the above document and approves the report for general distribution.

Please amend your copy accordingly by deleting the notice at the foot of the title page.

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