UCRL-CR--105776

DE91 007126

received by OSTI
FEB 06 1991

RADON TRANSFORM COMPUTER

W. Current, P. Hurst, G. Ford,
E. Shieh, I. Agi, C. Nguyen, D. Patterson

October 1990

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FINAL REPORT ON
"RADON TRANSFORM COMPUTER"
RESEARCH ACTIVITIES

PREPARED BY
WAYNE CURRENT, PRINCIPAL INVESTIGATOR

PARTICIPANTS
WAYNE CURRENT, PAUL HURST, GARY FORD,
ERIC SHIEH, ISKENDER AGI, CLARE NGUYEN, AND DAVE PETERSON

EECS Department
University of California
Davis, CA 905616

Submitted to STEVE AZEVEDO
LNL
October 31, 1990

I. INTRODUCTION

The overall goal of this project is to evaluate the potential of extremely fast hardware architectures for image processing. Primary focus is upon hardware realizations of the Radon transform and backprojection because of their applicability to computed tomography. In this report, we summarize our results from September 1989 through October 1990 in the design, realization, and characterization of a Radon transform and backprojection multiprocessor board.

The Radon transform and its inverse (a filtered backprojection) have been used in the area of image reconstruction, particularly for computed tomography (CT). However, it has more general applications in image processing and is restricted in its use by its large computational demands. Like the Fourier transform in the late 1960's, the Radon transform could possibly impact many areas if forward and inverse transforms could be computed very rapidly. Highly optimized algorithms and multi-processor hardware architectures for the forward and inverse Radon transform have been and are being studied to allow maximum improvements in computational speed. This UCD project is on the leading edge in developing such a computational "engine", a "Radon transform computer" (RTC), that could be applied to a variety of applications. Two hardware approaches to realizing the "Radon transform computer" have been designed at UCD. The first uses commercially available, general purpose digital signal processing (DSP) integrated circuits (ICs). We have constructed and tested a "Radon Transform Processor" (RTP) multi-processor board that uses TMS320C25 DSP chips. The RTP has 4 DSP chips in place and is expandable. These studies demonstrate that a multi-processor DSP chip realization of the RTC can be substantially faster than other presently available alternatives. A second approach is based upon a UCD-designed fully custom CMOS VLSI IC optimized for the forward transform and back-projection calculations. The chip architecture is pipelined to allow data to enter the processor at a rate of one point per clock cycle. As fabricated in a common 1.5-micron CMOS technology, this chip will operate at estimated clock frequency between a worst-case 27 MHz and a best-case 50 MHz, allowing reconstructions at video rates. This chip

design is reported upon in our separately submitted "Final Report on the "REAL-TIME MULTI-DIMENSIONAL PROCESSING HARDWARE DESIGNS" Project".

In both hardware designs above, we are using the Parallel Pipeline Projection Engine (PPPE) system architecture [1-3] for our high speed Radon transform computer. The PPPE architecture consists of a group of processors with 2 data distribution paths; one bus that connects all processors in parallel, and a processor-to-processor path is used to pipeline data through the processors. In computing the forward transform, each processor computes one projection of the Radon transform for one particular angle. Each processor, operating in parallel with the others, takes the input pixel, computes the appropriate bin to add the pixel value to in the transform space, performs the addition, and stores the result in local RAM. When the complete image has been processed, the Radon transform of the image is stored in local memory of the processors. For maximum processing speed, there should be one processor per projection; otherwise multiple passes of the image must be made with each processor computing the Radon transform values for different angles on the multiple passes. For handling the back projection, the PPPE architecture employs the same group of processors, each being preloaded with the Radon transform values for one particular projection angle. The image is reconstructed a pixel at a time - the value of each pixel is passed down the pipeline, with each processor adding the contribution of its projection to that pixel.

Our interests are in the high-speed reconstruction of high-resolution images from collected projection data, and the computation of the forward transform, especially for more sophisticated multiple pass algorithms. Our Radon transform computer specifications require computing the forward transform and backprojection, handling 1024 pixel by 1024 pixel images, using 720 projections over 180 degrees, using 16-bit collected data, and processing data as rapidly as possible, possibly as much as 100 times faster than existing hardware for Radon transform computations.

In an effort to achieve these goals, we focused our research activities in three areas during the 1989-90 funding period. These activities are:

1. Design, construction, and testing of a multi-processor RTP prototype board to compute the Radon transform and backprojection using four TMS320C25 DSP chips.
2. Design, simulation, and layout of a custom CMOS VLSI chip with a unified Radon transform/backprojection architecture that will be capable of at least 10MHz data rate processing of images.
3. Evaluation of the hardware requirements for high speed filtering of data to be backprojected.

In this final report, we summarize some of our results from September 1989 to October 1990. The design, construction, and testing of a four-processor prototype multi-processor (RTP) board using TI TMS320C25 DSP chips (item 1) has been completed. We are now finishing the extensive detailed final documentation of the RTP hardware and software. This extensive documentation will be provided to Steve Azevedo when we return the borrowed workstation and deliver the RTP to LLNL. A summary of the test results are in Section II. The design of our fully custom CMOS VLSI chip (item 2) has been completed. The chip has been designed, the layout completed, and the chip is now going through its final pre-fabrication simulations. The present status of the custom chip design activity will be summarized in the separately submitted "Final Report on the "REAL-TIME MULTI-DIMENSIONAL PROCESSING HARDWARE DESIGNS" Project". Evaluations of the hardware requirements for fast filtering of data for filtered backprojection (item 3) have been completed and are summarized in Section III.

In the next section, we briefly summarize the test results of the TMS320 multi-processor prototype RTP board evaluation.

II. RTP MULTI-PROCESSOR BOARD

The Radon Transform Processor (RTP) board prototype operates as a slave to LLNL's Integrated Solutions (IS) workstation, which contains a Motorola 68020 processor running the UNIX operating system. The RTP coprocessor interfaces to the host via the VMEbus. The expandable prototype contains 4 TMS320C25 DSP chips.

RTP Coprocessor Operation

The overall operation of the RTP coprocessor is as follows. For the backprojection, the workstation's 68020 loads the projection data and C25 backprojection program code into the dual ported memory on the coprocessor board. Subsequently, the host resets the DSP chips. Upon reset, the DSPs begin calculating the backprojection (and filtering) in a parallel/pipelined fashion. To reconstruct the image, the first DSP calculates a portion of the first pixel. Once this calculation is complete the partial pixel value is passed down the pipeline to the second DSP which adds its contribution to that pixel while the first DSP begins calculations of the second pixel's partial value. Partial pixel values are passed down the pipeline until the last DSP, after adding its contribution, writes the reconstructed pixel value to the VMEbus via an on-board output FIFO. When the output FIFO is full the host reads and stores the pixel values in the high speed memory located on another card in the IS system. This process is continued until the entire image is reconstructed. For the forward projection, the 68020 loads the forward projection C25 code and resets the C25s. Then the host writes pixel values to the coprocessor through an on-board input FIFO. The C25s calculate the forward projection and the results are stored in the on-board RAM. When the C25s are done, the host may access the transform values for further processing.

RTP Hardware

The RTP coprocessor hardware construction is complete. The coprocessor is constructed on two double-height VME wire wrap boards. In Figure 1 it is shown mounted in the IS workstation. For maximum processing speed, fast 25 ns static RAM is used which allows the C25s to run at full speed (10 MHz). Experiments summarized in Section II demonstrate that the 4-processor RTP operates at rates that approximate those predicted for parallel processors.

RTP Software

Each C25 in the system runs identical code but uses different angle and projection data. Code for implementing the forward and backprojection routines on the C25 schedules the computations such that the C25s stay compute bound. Host control code has been written that includes loading and unloading projection and pixel data, loading program code, and controlling the various board functions.

Experimental Results

Timing experiments were performed. The first image used was the Shepp Logan phantom head image which is 80 x 80 pixels and the second was a 128 x 128 pixel image of a portion of a printed circuit board. Eighty projections were used in the phantom head image and 128 projections were used in the circuit board image. The relatively small images were used since the Integrated Solutions workstation does not contain sufficient memory to completely process larger images. The two runs involved taking the forward transform, filtering the results using the host processor, and backprojecting the filtered projections. The results for the forward and backprojection calculations, excluding the filtering, are presented in Table 1. We see that the phantom image required 0.92 seconds to forward project and the circuit board image required 3.7 seconds to forward project. The backprojection operation for the images required 0.72 seconds and 2.9 seconds, respectively. The reason for the difference in timings between the forward and backprojection is due to the fact that the forward projection performs some 32-bit computations, while the backprojection does not. Since the TMS320C25 is a 16-bit processor, additional memory fetches and computations are necessary. In Table 1 we see that processing a 128 X 128 image takes four times as long to backproject than the 80 X 80 image. This is because, firstly, the number of clock cycles to compute the backprojection varies with the square of a linear dimension of the image. Secondly, with the larger image, 128 projections are taken versus 80 (i.e. $(128/80)^2 = 4.096$). For the first two images, the mean squared error is listed. These values are identical to floating point computations. The original images are shown in Figure 2 and the reconstructed images are shown in Figure 3.

Forward Transform Clock Cycle Analysis. Using the TMS320C25's software simulator to compute the forward transform, it was determined that the C25's require approximately 51 clock cycles to compute the two interpolated transform values for one pixel. This value does not include C25 initialization or looping overhead. The overhead incurred by the initialization code requires 278 cycles and the looping code requires $12 \times (\text{number of pixels})$. The initialization code is run only once at the beginning of the computations. Although the initialization overhead is negligible compared to the entire forward or backprojection operations, the looping overhead is not negligible and accounts for approximately 30% of the total DSP processing time.

Backprojection Clock Cycle Analysis. In the backprojection routine, the C25's require approximately 47 cycles to compute one pixel value from one projection. This value differs from the forward projection since the backprojection strictly uses 16-bit values whereas the forward transform computations involves some 32-bit computations. Since the C25 is a 16-bit microprocessor additional overhead is incurred. This fact explains the difference in the timings of the forward and backprojection columns in Table 1.

It is interesting to analyze the time that the C25 processors are actually performing computations i.e. additions, multiplications etc. The instructions in the C25 backprojection routine have been classified into the following four categories. They are mathematical operations, memory operations, looping operations, and miscellaneous overhead. If the operations above are labeled M, F, L, and C, respectively, the following relationship describes the relative amount of time the processors are performing the different operations during reconstruction.

$$\text{Number of clock cycles} = \text{pixels} * \text{projections} * [13M + 21F + 12L + 3C].$$

Here we see that the looping overhead accounts for approximately 26% of the total execution time which is close to the amount of time the DSP is doing mathematical computations. This relatively high percentage is a consequence of the internal pipeline operation of the TMS320C25. We also see that the backprojection operation is relatively memory intensive as one would expect. A similar analysis of the forward projection routine produces similar results.

I/O Communication Delays. In real digital systems, I/O communication delays are an important factor in maximizing system throughput. The design of the RTP and of the software minimizes I/O bottlenecks and hence maximizes reconstruction times. The first communication channel to consider is the pixel data path from the host to the RTP. The host transfers one 16-bit pixel to the RTP every 400 ns. A 80×80 image with 80 projections requires one pixel every 112 μs , hence the interface is able to keep the input FIFO full and the C25's compute bound. The second channel is the pipeline connecting the C25's. Since each DSP executes copies of essentially the same code, each DSP will be done with one partial pixel calculation at approximately the same time. The C25's pass the partial pixel value down the pipeline and read the next pixel value. The delay involved here is the time needed for an individual DSP to write out a pixel value, to read a status port and then to read its input port. This delay is approximately 18 clock cycles.

Processing Larger Images. In the present hardware configuration of the RTP, each C25 has 64 Kwords of data memory which limits the amount of projection data that can be downloaded to the RTP in one run. For a four and eight processor RTP the largest images that can be processed in one run are 304×304 and 430×430 pixel images, respectively, with 304 and 430 projections, respectively. For larger images, a subset of the projections is downloaded for each run and the process is repeated multiple times. An eight processor RTP and a 1024×1024 image with 1024 projections will require six passes before the image is completely reconstructed. For each of these six passes, the C25's data memory is loaded with 23 projections. The RTP is reset and the image is partially reconstructed. On the subsequent passes, another 23 projections per processor are loaded with the previous run's partial pixel values. The host writes these pixels into the input FIFO so that the contributions of the current pass can be added to the values calculated in the previous passes. This process is continued until the entire image is reconstructed using all 1024 projections. With the current configuration of the RTP with four TMS320C25's, a 1024×1024 image with 1024 projections requires approximately 25 minutes to reconstruct.

III. FILTERING

Reconstruction of an image with the Inverse Radon Transform is obtained through the two steps of the filtered backprojection operator. First, each projection is filtered by a one-dimensional rho filter, the result then is back projected to yield the reconstructed image.

The filtering operation can be performed either in the spatial domain or the projection domain, which naturally gives rise to two different methods of finding the filtered backprojection: the convolution backprojection method and the filter backprojection method. In the convolution method, the filtering operation is implemented by a direct convolution in the spatial domain; in the filter backprojection method, the frequency response of the filter is implemented with the Fourier transform of the image projection.

The convolution backprojection method was found to be computationally cumbersome and not suitable for high-speed parallel/pipelined processing as needed in this research [4] and is not discussed further here. The filter backprojection method appears computationally best suited for our applications [5]. The filter frequency response required for the Inverse Radon Transform emphasizes high spatial frequencies, which results in noise amplification. To limit the unbounded nature of the frequency response, bandlimited filters are usually implemented and the goal in selecting the filter is to achieve the optimum trade-off between the filter bandwidth and the noise suppression. A DSP chip, the TMS320C25 16 bit processor, is used to implement the filter algorithm. The input data is an array of 256 real numbers, each 32 bits in length that includes 24 integer bits and 8 fractional bits. An FFT is first performed on the input array with 16 bits to represent each FFT weight. The output of the FFT is multiplied with the filter coefficients that are also 16 bits each. Finally an inverse FFT is performed on the filtered data to change back to the spatial domain. It was found [5] that the FFT-based filtering could be completed with good accuracy using the TMS320C25. Complete FFT, filtering, and inverse FFT of a 256 by 256 image with 256 projections is completed in 72 s.

IV. REFERENCES

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Machine	Image Size	No. of projections	Forward	Backprojection	MSE
RTP	80 X 80	80	.92 s	.72 s	0.027
	128 X 128	128	3.7 s	2.9 s	0.006
SUN 3/160	128 X 128	128	308 s	560 s	0.006

Table 1
Radon Transform Processor Board Performance

Figure 1 Radon Transform Processor Boards

Figure 2a Original image 1

Figure 2b Original image 2

Figure 2c LLNL reconstructed image 3

Figure 3a Reconstructed image 1

Figure 3b Reconst

Figure 3c RTP Reconstructed image 3

END

DATE FILMED

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