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RELIABILITY OF PACKAGED BEAM-LEAD
TRANSISTORS BUILT WITH DIFFERENT
PRE-SEAL ASSEMBLY TECHNIQUES

By J. P. Gracey

Published October 1978

Topical Report
W. C. Coupland, Project Leader

Prepared for the United States Department of Energy
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**Kansas City
Division**

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RELIABILITY OF PACKAGED BEAM-LEAD TRANSISTORS BUILT WITH
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The reliability of two TO-18 packaged beam-lead transistors was studied using high temperature reverse bias and high temperature storage as accelerated aging methods. Three pre-seal assembly techniques were evaluated and compared based on reliability test results. Results were affected by the use of damaging breakdown voltage tests during part of the experiments.

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SUMMARY

This project is a reliability study of two canned beam-lead transistors, the SA2211 and the SA2212, which are used interchangeably in several Bendix applications. The report also is a study of three pre-seal transistor assembly techniques: pre-seal cleaning in deionized water and alcohol, vacuum baking without special cleaning, and conformal coating of the chip without special cleaning.

Experimental techniques included the use of high temperature reverse bias (HTRB) and high temperature storage (HTS) as accelerated aging tests. These tests were performed on subgroups of SA2211 and SA2212 transistors assembled into TO-18 cans using the different pre-seal processes. The various subgroups were placed on HTRB or HTS, then removed for electrical evaluation testing at certain time intervals to generate failure-in-time curves. HTRB times of 72 to 1344 hours at temperatures of 175 to 300°C were used.

Results were affected by the use of breakdown voltage tests as a part of the electrical evaluation test sequence. These tests caused degradation of SA2211 transistors by shorting through a region of thin oxide under either the base or emitter metallization to the underlying silicon which forms the collector. Device-to-tester incompatibilities produced oscillations during breakdown voltage testing of SA2212 transistors which caused degradation. In addition, some SA2212 transistors had passivation cracks under the chip anchor pad which were shorted during breakdown voltage tests. Breakdown voltage tests were discontinued when it became known that they were causing device degradation. However, since all experimental subgroups had been tested in this way several times, quantitative evaluation of reliability became impossible.

The absence of significant numbers of failures in the experimental subgroups once breakdown voltage testing was discontinued suggests that the long term reliability of both the SA2211 and SA2212 may be high. Also, the similarity of the results of the three SA2211 subgroups with different assembly techniques shows that none of the techniques is preferred over the others and that all three can be used to build reliable transistors.

Another conclusion which is evident from the testing results is that the routine use of breakdown voltage testing as a part of an evaluation test sequence should be avoided. Such tests operate a transistor in a potentially degrading mode, which is unrealistic for any application, while providing little useful information.

DISCUSSION

SCOPE AND PURPOSE

This study was designed to evaluate simultaneously the effects of various pre-seal cleaning or assembly techniques on canned beam-lead transistors, and the reliability of the SA2211 and SA2212 beam lead transistors using both high temperature storage (HTS) and high temperature reverse bias (HTRB) as means of accelerated aging.

PRIOR WORK

Testing techniques, failure criteria, and methods of assessing reliability were reported in Semiconductor Preconditioning Techniques.¹ Primary references in the literature are publications of Kemeny^{2,3} and Peck.⁴

ACTIVITY

The goals of this study were:

- To determine if specific assembly process techniques, including pre-seal cleaning, pre-seal vacuum bake, and the application of conformal coating, should be preferred in the assembly of canned beam lead transistors; and
- To determine if specific beam lead transistors (the SA2211 and SA2212) were capable of high reliability under end-use conditions which include long term storage under bias.

Experimental Grouping for Process Technique Studies

Use of beam lead semiconductors in Bendix-built hybrid microcircuits has become commonplace. However, use of beam lead devices in a discrete package such as a TO-18 can is a relatively new process. Development of a special header and of special processing techniques have become necessary, including the process required for final pre-seal cleaning and the need for a conformal coating over the beam lead chip. For this project, three basic process technique groups were established and compared.

- One group was washed in DI water, rinsed in alcohol, inspected for handling damage, baked in dry nitrogen, capped, and sealed in dry nitrogen.

- One group was inspected for handling damage, vacuum baked at 125°C for 16 hours, within 4 hours baked in dry nitrogen, capped, and sealed in dry nitrogen.
- One group was inspected for handling damage, coated with conformal coat, baked in dry nitrogen, capped, and sealed in dry nitrogen.

In addition to these three groups, a fourth group was selected which was built with an entirely different packaging method (a TO-5 ceramic package) at a different location. This group is described more completely in following paragraphs.

Experimental Grouping for Reliability Studies

Beam lead transistors are procured by Bendix as whole etch-separated wafers with the chips still mounted on a glass plate or sapphire disc. The wafers are electrically probed, and the electrically acceptable chips are removed from the original array and transferred to an expanded array. Visually defective chips are removed from the expanded array, and the remaining devices are used in various Bendix applications.

For this study, two types of transistor chips from various identified wafers from two manufacturers were selected for assembly into TO-18 transistor packages. The devices had undergone all normal supplier and Bendix processing and were at the point of use.

The first transistor type selected was the SA2211, electrically equivalent to the 2N2484. The second type was the SA2212. The SA2211 and SA2212 are used interchangeably in Bendix applications.

Experimental Procedure

Approximately 600 SA2211 transistors taken equally from two wafers were bonded to clean TO-18 headers at Bendix. The devices and clean caps were shipped to another firm where the three assembly process techniques were applied to subgroups of the 600 transistors. All work was carried out on a high reliability controlled assembly line. A similar assembly was performed on approximately 225 SA2212 transistors from two wafers, except that all devices were assembled with a pre-seal vacuum bake. None were washed or conformally coated. Figure 1 illustrates how the groups were split and identified, and the type of testing ultimately performed on each subgroup.

Figure 1. Processing Flow Charts for the Various Experimental Groups

Figure 1 Continued. Processing Flow Charts for the Various Experimental Groups

In addition to the subgroups already described, a comparison group of SA2211 transistors was selected which had been packaged in an entirely different manner. Chips were selected randomly from four wafers and bonded into TO-5 ceramic packages. This packaging method was expected to provide an interesting comparison with the TO-18 metal-can packaging groups because the ceramic devices were not hermetically sealed. In fact, the beam-lead chips were actually open to the atmosphere because of the small hole intentionally cut in the device cap. The TO-18 metal-canned devices were hermetically sealed. Figure 1 also illustrates the flow charts for the ceramic devices.

Upon completion of assembly, the transistors were returned to Bendix to begin the experimental test procedure. Each subgroup was first tested electrically; electrical tests, conditions and limits are described in Appendix A. After failures were removed, the subgroups were processed through either High Temperature Reverse Bias (HTRB) or High Temperature Storage (HTS). Each subgroup was removed from HTRB or HTS for electrical testing at various time intervals, then returned to the same condition. In this way a curve of failure rate versus time-on-test could be generated and compared among various subgroups. HTRB and HTS conditions and removal times for each subgroup are described in Appendix B.

Use of Accelerated Tests to Determine Reliability

It is impractical in most cases to assess reliability by placing a group of transistors or diodes under the exact conditions of the system in which they are to be installed, because system storage or operating times are typically many years. Therefore, it is necessary to use accelerated tests to bring out failure modes in a short period of time and to project the results to actual circuit storage or operating conditions. Examples of such accelerated tests are high temperature storage (HTS), power burn-in, and high temperature reverse bias (HTRB). Long experience of other observers in assembling data from accelerated life tests leads to the expectation that failure rates will follow what is known as a log-normal distribution. This means that if the log of the time-on-life-test is plotted versus the accumulative percent failure on "probability" paper, then the result will be a straight line after a period of time. Figure 2 is an example of such a plot. The scales on the x-axis are chosen so that if the plot is a straight line, then the variable plotted on the y-axis has a "normal" or "Gaussian" distribution, the familiar bell-shaped distribution curve.

In practice, a straight line often appears only after long times on life test. A straight line will sometimes occur at shorter times, but the "S" shaped curve of Figure 2 is very common. The

Figure 2. Plot of Percent Failing Versus Time-on-Test for 175°C HTRB on an SA2216 Transistor Group

upper portion of the curve is straight indicating a log-normal distribution. However, the lower portion is not at all straight. The reason for this shape is the presence of two distinct distributions, or reliability levels, in the total population. A relatively small percentage of devices fail very quickly. Such devices are known as "freaks," "sports," or "early failures." A second larger group, the main portion of the population, fails at a much lower rate. In Figure 2, the upper portion of the "S" shaped curve approaches the curve labeled "Main Distribution" as a limit. The lower portion of the "S" shaped curve approaches the line labeled "Freak Distribution" as a limit. If the two straight lines are added graphically, the result will be the "S" shape of the combined distribution curve.

Once the failure distribution in time is determined for a type of stress at several temperatures, the failure distribution under unaccelerated or low temperature conditions may be projected.⁴

Evaluation of SA2211 Transistor Reliability

Four experimental subgroups, which were assembled with the same technique (pre-seal vacuum bake), were tested at three HTRB temperatures and one HTS temperature. The curves of Figure 3 show the percentage failing versus time on HTRB or HTS. Little consistency is present in the data. For example, HTRB at increasing temperatures on homogeneous subgroups would be expected to produce higher failure rates at higher temperatures, assuming that a temperature-dependent failure mode subject to the Arrhenius equation⁴ is present. In addition, HTS at a particular temperature would be expected to cause fewer failures than HTRB at the same temperature if the expected surface degradation failure mode were present. Figure 3 shows, however, that for times up to 20 hours, 300°C HTRB produced fewer failures than 225°C HTRB. Furthermore, 300°C HTS produced about the same number of failures as 300°C HTRB. Another inconsistency is the failure of the 175°C and 225°C curves to confirm the shape of the 300°C HTRB curve.

These inconsistencies in the results show that the predominant failure mode is not temperature dependent nor is it clearly accelerated by the bias conditions of HTRB.

Examination of failures which occurred early in the process revealed that the primary failure mode was the breakdown of the thin insulating layer of silicon dioxide between either the base or emitter metallization on the chip and the underlying bulk silicon which forms the collector. The phenomena is enhanced by performing breakdown voltage tests and possibly by static electric discharge due to handling. Appendix C contains a complete description of the failure mode. A chip design change which leaves thick oxide under the base and emitter metallization has since eliminated this failure mode.

Figure 3. Comparison of Four Vacuum-Baked SA2211 Subgroups at Three HTRB Temperatures and One HTS Temperature

Evaluation of failures from the early endpoints of the various testing subgroups was not completed in time to eliminate the thin oxide-breakdown failure mode. Breakdown voltage tests were eventually eliminated from the test sequence of Appendix A, but not before many failures were observed. The slash marks on the curves of Figure 4 indicate when breakdown voltage tests were discontinued on each group.

The thin oxide breakdown failure mode should occur randomly and is independent of temperature, which explains why the expected HTRB and HTS results did not materialize. This breakdown problem has unfortunately made quantitative estimates of long-term reliability impossible. However, some qualitative observations are possible.

Once the degrading breakdown voltage tests were discontinued, very few failures occurred in the 175°C and 225°C HTRB and in the 300°C HTS subgroups. These results suggest that once the thin oxide-breakdown failure mode was eliminated by chip design change, the reliability of the canned SA2211 should be high.

This observation is reinforced by the results of the ceramic-packaged SA2211 transistors. Only one device of the 175°C HTRB subgroup (A7) failed (at 168 hours). Only two devices of the 175°C HTS subgroup (A8) failed (both at 336 hours). These results tend to confirm the potentially high reliability of the SA2211 transistor.

A second observation made possible by these results and by past experience is that breakdown voltage testing of transistors is inherently dangerous to the device under test while yielding little useful information. Such tests cause the transistor to be biased or operated in a mode which is both unrealistic to transistor applications and potentially degrading. In this case useful information could have been generated by the experiments had not breakdown voltage tests caused degradation. Note that these tests caused degradation, but did not discover the degradation. Leakage current tests and gain tests did that. For example, at 48 hours for subgroup A3A4-3, the two breakdown voltage tests indicated one failing transistor in the group of 85. Other tests indicated 47 failures.

Evaluation of SA2212 Transistor Reliability

The two experimental subgroups of SA2212 were used for HTRB testing at 175°C and at 300°C. Figure 4 shows the percentage failing versus time on HTRB.

Early 300°C failures were analyzed for failure mode as described in Appendix D. As in the case of the SA2211, it was found that breakdown voltage testing caused the failures. Breakdown voltage

Figure 4. Comparison of Two Vacuum-Baked SA2212 Subgroups

testing was discontinued on the 175°C sample at 26 hours, but all 300°C endpoints had these tests. Thus the 300°C sample data is considered to be of little value, and, as with the SA2211, the only possible observation of the 175°C data is qualitative; very few failures were encountered after breakdown voltage testing was eliminated, which suggests that the canned SA2212 transistors have potentially high reliability.

Evaluation of Preferred Assembly Techniques

The experiments were designed so that a direct comparison could be made of the reliability of subgroups assembled with one of three different final processing steps:

- a DI water-alcohol wash prior to sealing (subgroup A1A2);
- a vacuum bake without washing prior to sealing (subgroup A3A4-1); or
- application of conformal coating to the chip without any pre-seal cleaning (subgroup A5A6).

The subgroups were otherwise identical, with the same wafer lot composition and the same assembly and test techniques.

HTRB at 175°C was chosen as the accelerated aging test which would identify the most reliable final assembly technique. Long-term storage of the SA2211 or SA2212 transistor under bias is required in a potential application at Bendix. The HTRB conditioning is a valid means of accelerating failure modes which might appear in such an application.

Figure 5 shows the percentage failing versus time on HTRB for the three subgroups. Only a qualitative interpretation of these results is possible since so few devices failed (ranging from 4.8 to 7.7 percent failures after 1344 hours), and since the thin oxide-breakdown failure mode colored all results up to 26 hours. Despite these problems, the following conclusions can be inferred from the data.

- Early failures population is judged to be nonexistent or at most very small. Note that the maximum percent failing in any subgroup after 26 hours at 175°C HTRB is 2.6 percent. Even those failures could have been influenced by the thin oxide-breakdown failure mode, as breakdown voltage testing was not eliminated until the 26 hour endpoint.
- The curve for each subgroup approaches a straight line, indicating a log-normal distribution. Median life and standard deviation of the log-normal distribution cannot be

Figure 5. Comparison of the Three Assembly Process Technique Subgroups

estimated quantitatively, as noted above. Qualitatively, however, it is clear that each subgroup is composed of transistors with very long median lives.

- Data for all three subgroups are within a very narrow range of values, i.e., the curves are nearly indistinguishable. This result shows that no one of the processing techniques under study exhibits a clear superiority over the others. Any could be used to build reliable transistors.

ACCOMPLISHMENTS

Unfortunately, the use of damaging breakdown voltage tests prevented a thorough quantitative analysis of SA2211 and SA2212 reliability. However, the few failures observed during 175°C and 225°C HTRB and 300°C HTS once breakdown voltage tests were discontinued suggests qualitatively that reliability of both is high. The results of the ceramic-canned SA2211 transistors reinforce this conclusion.

Since the three homogeneous SA2211 subgroups with different assembly techniques were all tested identically and all produced similar failure-in-time curves, it is concluded that none of the techniques is preferable, and that any may be used to assemble canned beam-lead transistors of high reliability.

Breakdown voltage tests should not be a routine part of any evaluation test sequence, especially on automatic testers. Experience on this and on other projects indicates that such tests provide little useful information, while being potentially damaging to the device under test. Operation in breakdown is not a normal transistor application or design criteria and should, therefore, not be routinely expected of a transistor.

REFERENCES

¹J. P. Gracey, High Temperature Reverse Bias and Power Burn-In at Transistor Junction Temperatures from 150° to 300°C (Topical Report). UNCLASSIFIED. Bendix Kansas City: BDX-613-1038, April 1978 (Available From NTIS).

²A. P. Kemeny, "Experiments Concerning the Life Testing of Transistors - I," Microelectronics and Reliability, 1971, Volume 10, pp 169-194.

³A. P. Kemeny, "Experiments Concerning the Life Testing of Transistors - II," Microelectronics and Reliability, 1971, Volume 10, pp 75-93.

⁴D. S. Peck, "The Analysis of Data from Accelerated Stress Test," Proc. of 1971 Annual Symposium on Reliability Physics. Las Vegas: IEEE Catalog No. 71C9PHY.

⁵W. J. Kirk and others, Control of Electrostatic Damage to Solid State Devices. UNCLASSIFIED. Bendix Kansas City: BDX-613-1080, March, 1974 (Available from NTIS).

Appendix A

ELECTRICAL TESTS

The tests shown in Table A-1 were performed on each transistor initially and thereafter at selected points for each testing group. The tests were always performed in the order listed.

All tests were performed by an automatic tester. Data generated by the tester were collected by a computerized data acquisition system.

A failure was defined as a device which failed one or more of the tests. The concept of "once a failure, always a failure" was used throughout. Thus, if a particular device failed at one endpoint step but passed at a later step, it was counted as a failure at the original failing point and at all subsequent points.

Table A-1. Electrical Endpoint Tests

Test Number	Test Type	Test Conditions	Limits	
			Minimum	Maximum
1	I_{CBO}	$V_{CB} = 45 \text{ V}$		20 nA
2	I_{EBO}	$V_{EB} = 5 \text{ V}$		10 nA
3	h_{FE}	$V_{CE} = 5 \text{ V}, I_C = 10 \text{ } \mu\text{A}$	100	
4	h_{FE}	$V_{CE} = 5 \text{ V}, I_C = 1 \text{ mA}$	250	
5	$V_{BE(ON)}$	$V_{CE} = 5 \text{ V}, I_C = 100 \text{ } \mu\text{A}$		0.70 V
6	$V_{CE(SAT)}$	$I_B = 0.1 \text{ mA}, I_C = 1 \text{ mA}$		0.35 V
7	BV_{CBO}	$I_C = 10 \text{ } \mu\text{A}$	60V	
8	BV_{CEO}	$I_C = 10 \text{ mA}$	60V	
9*	I_{CBO}	$V_{CB} = 45 \text{ V}$		20 nA
10*	I_{EBO}	$V_{EB} = 5 \text{ V}$		10 nA
11	h_{FE}	$V_{CB} = 5 \text{ V}, I_C = 100 \text{ } \mu\text{A}$	100	

*Tests 9 and 10 are identical to tests 1 and 2; they were performed to ensure that the transistors were not damaged during testing.

Appendix B

TEST CONDITIONS

HTRB or HTS was performed on each processing group as indicated in Table B-1. The groups were removed at various time intervals for the electrical tests (Appendix A) at room temperature.

HTRB bias was maintained on each device while cooling to room temperature and until ready for testing. When ready, a tray of devices was attached to a 6 V battery (applying reverse bias to the C-B junction) for transportation to and from the tester. Thus, C-B reverse bias was interrupted only while a device was actually being tested electrically. While mounted in an HTRB tray, a 70,000 Ω current limiting resistor was in series with each transistor junction.

No similar precautions were required with HTS groups, since no bias voltage was applied.

Bias voltage for HTRB was determined by monitoring the actual voltage across the collector-base junction of a representative transistor, rather than the power supply voltage. A reverse bias of 28 V was used for all HTRB groups.

Table B-1. Test Conditions for HTRB and HTS

Process Group*	HTRB or HTS	Temperature (°C)	Starting Quantity	Removal Times for Electrical Tests (Hours)
A1A2	HTRB	175	80	1, 4, 10, 26, 48, 96, 168, 336, 672, 1008, 1344
A3A4-1	HTRB	175	85	1, 4, 10, 26, 48, 96, 168, 336, 672, 1008, 1344
A3A4-2	HTRB	225	85	1, 2, 6, 10, 18, 26, 48, 96, 168, 336, 672
A3A4-3	HTRB	300	86	0.5, 1, 3, 5, 12, 20, 48, 72, 96, 168, 336
A3A4-4	HTS	300	87	0.5, 1, 3, 5, 12, 20, 48, 72, 96, 168, 336
A5A6	HTRB	175	84	1, 4, 10, 26, 48, 96, 168, 336, 672, 1008, 1344
A7	HTRB	175	100	1, 4, 10, 26, 48, 96, 168, 336, 672, 1008, 1344
A8	HTS	175	100	1, 4, 10, 26, 48, 96, 168, 336, 672, 1008, 1344
B1B2-1	HTRB	175	103	1, 4, 10, 26, 48, 96, 168, 336, 672, 1008, 1344
B1B2-2	HTRB	300	104	0.5, 1, 3, 5, 12, 20, 48, 72

*Groups with Designation A are SA2211 transistors; Groups with Designation B are SA2212 transistors.

Appendix C

EVALUATION OF SA2211 FAILURES

All SA2211 failures examined failed because of breakdown of a region of thin oxide under either the emitter or base metallization. This breakdown caused a leakage path between the metallization and the underlying collector region.

Figure C-1 illustrates the chip design of both SA2211 lots used in this study. Emitter and base metallization each cross a region of the collector which is insulated by only a very thin (200 to 300 nm) silicon dioxide layer. A cross section of this region is shown in Figure C-2. It was found that BV_{CBO} or BV_{CEO} (Tests 7 and 8 in the sequence of Appendix A) induced breakdown of this thin oxide region, causing high leakage currents which could range from a few nanoamperes above the I_{CBO} limit of 20 nA to greater than 10 mA. Values of 20 to 300 μA were common.

Many devices were decanned and observed visually. Figures C-3 through C-6 show examples of the type of burned spots observed over thin oxide under both base and emitter metallization from both SA2211 lots (53024 and 39489). The oxide punch-through was caused primarily by the voltages applied during breakdown voltage testing (approximately 88 to 105 V), although it is also conceivable that static electric voltages could cause similar degradation. Static voltages as high as 1000 to 1500 V can be produced during normal handling.⁵ Such voltages are capable of punching through a thin oxide layer.

However, it is noteworthy that the elimination of breakdown voltage tests from the electrical endpoint test sequence coincided with a drastically decreased failure rate in all experimental subgroups.

The thin oxide under the metallization was eliminated in a later design, illustrated in Figure C-7. Thicker oxide was left in the area under the base and emitter metallization.

While it may be argued that the failures occurred because of a chip design problem (thin oxide), the presence of this failure mode in the experimental subgroups depended primarily on performing breakdown voltage tests, and not clearly on any conditions foreseeable in any application. Thus it can be concluded that the performing of the breakdown voltage tests introduced an unrealistic failure mode which hampered a true reliability assessment of the SA2211 transistor.

Figure C-1. Chip Design of Both SA2211 Lots (53024 and 39489) Used in This Study, 150X

LOT 53024

BASE
METALLIZATION (GOLD)

THIN OXIDE REGION
(APPROX. 3000 Å)

LOT 39489

BASE
METALLIZATION
(GOLD)

THIN OXIDE REGION
(APPROX. 2000 Å)

Figure C-2. Cross Sections of the Thin Oxide Regions Under the Base Metallization, 750X, Lapped at an Angle of 11°

Figure C-3. Oxide Punchthrough on a Transistor From Group A4, 300X

Figure C-4. Collector-Base Shorted Area on a Transistor From Group A1, 500X

Figure C-5. Shorted Area in the Base Metallization of a Device From Group A3, 750X

Figure C-6. Short at the Edge of Emitter Metallization on a Group A1 Device, 500X

AREAS OF INCREASED
OXIDE THICKNESS
(ARROWS)

150X

AREA OF INCREASED
OXIDE THICKNESS

500X

Figure C-7. Redesigned SA2211 Chip (Lot 26326) With Thick Oxide Under Base and Emitter Metallization (Compare with Figures C-1 and C-2.)

Appendix D

EVALUATION OF SA2212 FAILURES

The first SA2212 transistors tested at early endpoints in the 300°C HTRB subgroup (B1B2-2) exhibited failure rates much higher than expected. A failure analysis effort was subsequently undertaken to determine the failure modes present in the subgroup.

Procedures

Seven 0.5-hour endpoint failures and one 3-hour endpoint failure were removed from the 300°C HTRB group and categorized.

Category I

Devices which appeared acceptable during the tester pass up to the BV_{CBO} test, and then failed breakdown voltage and a subsequent test. These devices had passed an identical leakage test earlier in the same tester pass. Two units in this category were evaluated, serial numbers 15 and 16. The samples were baked for 6 hours at 250°C, with no improvement noted. The chips were then removed from the headers and the front side metal was removed. Cracks were found in the passivation beneath the base and emitter anchor pads. One device (Number 15) was probed and found good, confirming the passivation cracks as the source of the leakage.

Category II

Devices which exhibited high emitter-base leakage and low h_{FE} but were acceptable on I_{CBO} . Four devices in this category were evaluated: Serial Numbers 20, 25, 45, and 56. Interestingly, two of these, Numbers 20 and 45, were acceptable during the first I_{EBO} and h_{FE} tests of the tester pass, but failed an identical I_{EBO} and subsequent h_{FE} later in the same tester pass.

Sample 25 did not improve during bake, and was then opened and the metal removed. The emitter-base leakage was still high, and an overstress mark could be seen between emitter and base. The overstress mark is characteristic of excessive emitter-base reverse voltages.

The remaining three devices in this category improved to near normal during bake and were replaced on HTRB at 300°C for 2 hours. Immediately following HTRB (during the first part of the tester pass), they displayed slight h_{FE} degradation. Following BV_{CBO} testing, however, all three exhibited degradation ranging from a 50 percent loss of gain to catastrophic E-B and C-B damage. Two

devices, Numbers 45 and 56, were opened and the metal was removed, and both exhibited E-B overstress marks similar to Number 25.

Category III

Devices which failed I_{CBO} testing at the first of the tester pass, with consistent data through the complete pass. Two devices in this category were analyzed: Serial Numbers 2 and 14. Both recovered on baking, and were then replaced on HTRB for 0.5 hour at 300°C (the original time to failure). Both were still good after 0.5 hour (Number 2 exhibited 11.9 percent h_{FE} degradation at 100 μ A current level while Number 14 exhibited none), but Number 14 became an E-B short following BV_{CBO} testing. (Subsequent analysis showed an overstress mark between emitter and base similar to previous samples.) Sample 2 was replaced on HTRB for two additional hours at 300°C, after which it exhibited another 9.2 percent in h_{FE} . It was then baked and again exhibited considerable recovery on h_{FE} .

Conclusions

Category I

It appears that the almost inevitable passivation cracks which occur during bonding were breaking down during the breakdown voltage testing, a phenomenon which has been known to occur in the past on beam-lead devices which have BV_{CBO} exceeding 100 V.

Category II

A device-tester incompatibility on BV_{CBO} , probably resulting in oscillation, and undoubtedly causing excessive emitter-base avalanche current, was the cause of failure in this category.

Category III

Sample 2 exhibited mild symptoms of passivation contamination, while Number 14 appeared to be external package contamination. The loss of Number 14 to the BV_{CBO} failure mode of Category II precluded further analysis, and a strong possibility exists that some or all of the initial degradation noted on Number 2 was also related to the BV_{CBO} failure mode.

Summary

Ionic passivation contamination appears to exist only slightly, if at all, as a failure mode on the SA2212. The main failure modes are testing incompatibilities related to breakdown voltage measurements. This testing was eliminated from both the SA2211 and SA2212 portions of the study, but the usefulness of the 300°C HTRB sample on the SA2212, which had breakdown voltage testing at all endpoints, has been severely hampered.

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