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**ANALYSIS AND EVALUATION IN THE PRODUCTION PROCESS AND
EQUIPMENT AREA OF THE LOW-COST SOLAR ARRAY PROJECT**

Metallization Pattern Design and Solar Cell Efficiency

Quarterly Report, January—April, 1980

By
M. Wolf

November 1980

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ANALYSIS AND EVALUATION
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LOW-COST SOLAR ARRAY PROJECT

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Quarterly Report January to April 1980
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Subject: Metallization Pattern Design and Solar
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November 1980

M. Wolf

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Summary

1. The analysis of the solar cell performance implications of the front metallization design for large area solar cells has led to a set of definitive Design Rules, contained in this report.
2. Some of the metallization processes used in solar cell production are not capable of yielding low losses. Worst seem to be the print-on thick film processes, which are limited to line widths of 127 μm or greater, and which yield only a fraction of the bulk conductance of the deposited metal.
3. While in general an optimum value exists only for the grid line and bus line shading ratios, with monotonously decreasing losses found for grid and bus line spacing tending towards zero (with the shading ratios maintained at their optimum values), this rule does not hold, when the bus line is a round or square wire, or the choice of grid line width is limited by technological requirements. In these cases, optimum values can be found for the bus line spacing and wire diameter separately, or for the grid line spacing in dependence on the minimum practical line width.
4. When it is not possible to apply bus lines of substantially lower sheet resistance than the grid lines, a pattern with grid lines only (no bus lines) will give a better performance (less shading for equal voltage drop!).
5. Grid lines arranged normal to the bus lines give better performance than obliquely arranged grid lines.

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I. INTRODUCTION

The analyses of the front metallization design methods and their impacts on solar cell performance, particularly for large area cells, which were started in the preceding quarterly report, have been continued and completed herein. The influence of line shape on the effective voltage drop, which was treated before for the uniform width lines and the fully tapered lines, has now been generalized to include any taper.

The second section of this report investigates the potential merits of an oblique arrangement of the grid lines with respect to the bus lines. It is found that the arrangement of the grid lines normal to the bus lines gives the best performance. However, the performance penalty for oblique arrangement at relatively small inclination angles against the normal to the bus line is rather small.

Finally, the ways of optimizing the front metallization pattern, consisting of grid and bus lines, with respect to lowest total performance loss, due both to shading by metal coverage and to voltage drops in the various elements of the current path, was re-investigated. It was determined that it is essential that each level in the hierarchy of conductors have a substantially lower sheet resistance, by at least an order of magnitude, than the preceding level. These levels are the front layer, usually a semiconducting sheet generated by diffusion or ion implantation, the deposited metal grid lines, and the bus lines, at times also referred to as the

current collectors. In view of this requirement, it was found that bus lines of deposited metal, similar in sheet resistance to the grid lines, are not only ineffective, but even detrimental. Thus, wire overlays are required for the bus lines in order to keep the combined shading and series resistance losses on, e.g. 10 cm x 10 cm cells, to near 5%. Without such bus lines, the combined losses amount to at least 12% of the ideal power output.

The findings of these analyses were combined into a set of Design Rules for the front metallization design for large area solar cells, which should be of general usefulness.

In addition, the groundwork has been laid for economic trade-off studies in the evaluation of the various metallization process options, which have differing pattern resolution and metal conductivity limitations and consequently result in differing cell efficiencies.

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FIG. 1 Explanation of nomenclature used in the analysis of the general tapered grid line

II. The General Tapered Grid Line Problem

In the preceding quarterly report, the end point voltage drops $V(W)$ and the effective voltage drops were investigated for uniform width and fully tapered grid lines. Since then, N. Mardesich of Spectrolab showed an integration method for partially tapered grid lines (Ref. 1). While the solutions resulting from that method appear to be singular at both end points of the range of possible tapers, which are the uniform width and the fully tapered grid line, it can be shown that the solution really is well behaved in those two cases and yields the same results as given in our preceding report. It seems therefore useful to generalize this approach to the methodology applied in our preceding quarterly report.

Figure 1 explains the nomenclature used to describe the geometry of the general tapered grid line. The width of the base of the grid line is $F \cdot T_{GL}$, while the width of the grid line at its end is $f \cdot T_{GL}$, with the length of the grid line being given by W as before. Thus, the area covered by the grid line is given by:

$$A = \frac{1}{2}(F + f) T_{GL} W ; \quad (1)$$

Since the area covered by the grid line shall be the same for all grid shapes, and equal to $T_{GL} \cdot W$, the condition:

$$\frac{1}{2}(F + f) = 1 ; \quad (2)$$

has to be fulfilled, which means that:

$$F = 2 - f ; \quad (2a)$$

The grid line width in dependence on position along the grid line is then given by:

$$T_{GL}(\ell) = fT_{GL} + (F - f) \frac{W-\ell}{W} T_{GL} ; \quad (3)$$

or, expressing $T_{GL}(\ell)$ exclusively in terms of the taper parameter f , after making use of eq. (2a) in eq. (3):

$$T_{GL}(\ell) = T_{GL} \left[f + 2(1-f) \frac{W-\ell}{W} \right] ; \quad 0 \leq f \leq 1 \quad (3a)$$

$f = 1$ describes the uniform width grid line, and $f = 0$ the fully tapered grid line, ending in zero width.

The incremental voltage drop over a length element $d\ell$ at the position ℓ along the grid line is then given by:

$$dV = R_{sh} \frac{d\ell}{T_{GL}(\ell)} \cdot j_{mp} (W-\ell) S ; \quad (4)$$

where R_{sh} is the sheet resistance of the grid line, and S obtained from the center-to-center spacing $S + T_{GL}$ of the grid lines. After inserting eq. (3a), eq. (4) can be expressed as:

$$dV = R_{sh} j_{mp} \frac{SW}{T_{GL}} \frac{(W-\ell) d\ell}{fW + 2(1-f)(W-\ell)} ; \quad (4a)$$

Integration from the base of the grid line to its end yields the end point voltage drop $V(W)$:

$$V(W) = R_{sh} j_{mp} \frac{SW}{T_{GL}} \int_0^W \frac{(W-\ell) d\ell}{fW + 2(1-f)(W-\ell)} ; \quad (5)$$

The integral has the solution:

$$\int_0^W \frac{(W-l) dl}{fW + 2(1-f)(W-l)} = -\frac{W-l}{2(1-f)} - \frac{fW}{4(1-f)^2} + \frac{fW}{4(1-f)^2} \ln \left[fW + 2(1-f)(W-l) \right] \Big|_0^W ; \quad (6)$$

which yields the expression for the end point voltage drop:

$$V(W) = R_{sh} j_{mp} \frac{SW^2}{2T_{GL}} \cdot G(f) ; \quad (7)$$

where:

$$G(f) = \frac{1}{1-f} \left[1 + \frac{f}{2(1-f)} \ln \left(\frac{f}{2-f} \right) \right] ; \quad (7a)$$

For $f \rightarrow 0$, $\ln \left(\frac{f}{2-f} \right)$ would tend towards minus infinity. However it is:

$$\frac{f}{2(1-f)} \ln \left(\frac{f}{2-f} \right) = \frac{1}{2(1-f)} \ln \left(\frac{f}{2-f} \right)^f ; \quad (8)$$

so that this relationship tends to $\frac{1}{2} \ln 1 = 0$ for $f \rightarrow 0$.

Consequently, the end-point voltage multiplier $G(f)$ for the fully tapered grid line becomes:

$$\lim_{f \rightarrow 0} G(f) = 1 ; \quad (9)$$

to yield the value of $V(W)$ just as obtained in the preceding report.

When f approaches 1, it is useful to substitute $f = 1 - x$, so that:

$$\frac{1}{1-f} \left[1 + \frac{f}{2(1-f)} \ln \frac{f}{2-f} \right] = \frac{1}{x} \left[1 + \frac{1-x}{2x} \ln \frac{1-x}{1+x} \right] ; \quad (10)$$

The logarithm can be expressed by an infinite series, so that the right hand side of eq. (10) changes to:

$$= \frac{1}{x} \left[1 - \frac{1-x}{2x} \cdot 2 \left(x + \frac{x^3}{3} + \dots \right) \right] \quad (10a)$$

FIG. 2 The values of the voltage drop multipliers $G(f)$ and $H(f)$ as function of f

or:

$$= \frac{1}{x} \left[1 - 1 - \frac{x^2}{3} - \dots + x + \frac{x^3}{3} + \dots \right] \quad (10b)$$

which, for $x \rightarrow 0$, becomes unity. Thus, the end-point voltage multiplier for the uniform width grid line is:

$$\lim_{f \rightarrow 1} G(f) = 1 ; \quad (11)$$

The values of $G(f)$ for intermediate values of f are shown in Fig. 2.

The incremental power dissipation in the grid line length element $d\ell$, located at value ℓ of the grid line length coordinate, can in similarity to eq. (4), be expressed as:

$$dP = R_{sh} \frac{d\ell}{T_{GL}(\ell)} \left[j_{mp} (W-\ell) S \right]^2 \quad (12)$$

which leads to the total power dissipated in the grid line;

$$P = R_{sh} j_{mp}^2 \frac{S^2 W}{T_{GL}} \int_0^W \frac{(W-\ell)^2 d\ell}{fW + 2(1-f)(W-\ell)} ; \quad (13)$$

The integral has the solution:

$$\int_0^W \frac{(W-\ell)^2 d\ell}{fW + 2(1-f)(W-\ell)} = \frac{1}{8(1-f)^3} \left[\frac{3}{2} f^2 W^2 + 2fW(1-f)(W-\ell) - 2(1-f)^2 (W-\ell)^2 - f^2 W^2 \ln \left[fW + 2(1-f)(W-\ell) \right] \right] \Big|_0^W \quad (14)$$

which results in the total dissipated power in the grid line:

$$P = R_{sh} j_{mp}^2 \frac{S^2 W^3}{8T_{GL}} \frac{1}{(1-f)^3} \left[2 - 6f + 4f^2 + f^2 \ln \left(\frac{2-f}{f} \right) \right] ; \quad (15)$$

Since the dissipated power can also be expressed by the product of the total current flowing out of the grid line and an "effective voltage drop" $V_{\text{eff}}(f)$:

$$P = j_{\text{mp}} \cdot SW \cdot V_{\text{eff}}(f) ; \quad (16)$$

comparing this relationship with eq. (15) leads to the expression for $V_{\text{eff}}(f)$:

$$V_{\text{eff}}(f) = R_{\text{sh}} j_{\text{mp}} \frac{SW^2}{4T_{\text{GL}}} \cdot H(f) ; \quad (17)$$

with:

$$H(f) = \frac{1}{2(1-f)^3} \left[2 - 6f + 4f^2 + f^2 \ln \left(\frac{2-f}{f} \right) \right] ; \quad (17a)$$

When f goes towards zero, the third term in the bracket of eq. (17a) approaches zero, as shown in the discussion relating to eq. (8), and the effective voltage drop multiplier becomes:

$$\lim_{f \rightarrow 0} H(f) = 1 ; \quad (18)$$

When f approaches unity, $1-x$ is suitably substituted for f in eq. (17a), with $x > 0$, so that:

$$\lim_{f \rightarrow 1} H(f) = \lim_{x \rightarrow 0} \frac{1}{x^3} \left[2 - 6(1-x) + 4(1-x)^2 + (1-x)^2 \ln \left(\frac{1+x}{1-x} \right) \right] ; \quad (19)$$

Consolidating the first three terms in the bracket of eq. (19), and expressing the logarithm by an infinite series, yields:

$$\lim_{f \rightarrow 1} H(f) = \frac{1}{2} \lim_{x \rightarrow 0} \frac{1}{x} \left[-2x + 4x^2 + (1-2x+x^2) 2 \left(x + \frac{x^3}{3} + \frac{x^5}{5} + \dots \right) \right]; \quad (20)$$

Equation (20) reduces to:

$$\lim_{f \rightarrow 1} H(f) = \frac{1}{2} \lim_{x \rightarrow 0} \left[\frac{8}{3} - \frac{4}{3}x + \frac{4}{5}x^2 - \frac{4}{5}x^3 + \dots \right] = \frac{4}{3}; \quad (21)$$

Thus, the effective voltage drop for the fully tapered grid line is $\frac{1}{2}$ of the end-point voltage drop, that of the uniform width grid line $\frac{2}{3}$ of the end-point voltage drop. The end-point voltage drops are equal for these two cases, and it may be remembered that the grid lines have been made to shade equal areas.

Values for the effective voltage drop multiplier $H(f)$ for intermediate values of f are presented in Fig. 2. It is seen that $H(f)$ increases monotonically from $H(0) = 1$ to $H(1) = 1.333$.

FIG. 3 Oblique grid line arrangement on half of a unit field around a bus line. The grid line inclination angle is α , the bus line length $L - W \tan \alpha$.

III. Oblique versus Normal Grid Lines

A question which does not have an obvious answer concerns possible advantages which an oblique arrangement of the grid lines relative to the bus lines might have over a normal arrangement. The only way to answer this question is through an analytical evaluation. In this evaluation, the total performance losses incurred with either of the arrangements, that is the voltage drops incurred and the area covered by metal, are the quantities to be analyzed. The voltage drops of concern are those in the front layer, usually a diffused semiconductor sheet, in the grid lines, and in the bus lines.

The analysis shall be based on a unit field of the solar cell. This unit field is defined as the area of a solar cell from which current flows into a single bus line. The pattern of this unit field is repeated periodically on the cell. For the purposes of the considerations here, the size of the unit field is constant, having been determined in a separate design process. The inclination angle α of the grid lines (Fig. 3) is measured against the normal to the bus line. The voltage drop in the front layer which is caused by the charge carrier flow to the nearest grid line, is given by:

$$\Delta V_{FL} = j \cdot \frac{S}{2} \cdot W \frac{1}{\cos \alpha} \cdot \frac{1}{2} R_{sh, FL} \cdot \frac{S}{2} \cdot \frac{\cos \alpha}{W}; \quad (22)$$

where $R_{sh, FL}$ is the sheet resistance of the front layer, usually a semiconducting sheet generated by diffusion or ion implanatation.

FIG. 4 Illustration of the 4 end triangles on the unit field which contain the grid lines of less than full length

As evident, the angle dependence in this relationship falls out, so that eq. (22) reduces to the front layer voltage drop for any grid line arrangement:

$$\Delta V_{FL} = \frac{1}{8} j R_{sh,FL} S^2 ; \quad (23)$$

It may be noted that eq. (23) expresses the end-point voltage drop, and that the effective voltage drop will be two thirds of the value of the end-point voltage drop, in accordance with the discussions of the preceding section.

Next to be considered is the voltage drop in the grid lines, which is given by:

$$\Delta V_{GL} = j S W \frac{1}{\cos \alpha} \frac{1}{2} R_{sh,GL} \frac{W}{\cos \alpha} \cdot \frac{1}{T_{GL}} ; \quad (24)$$

This relationship, again expressing the end-point voltage drop, yields an inverse proportionality of the voltage drop to the square of the cosine of the inclination angle:

$$\Delta V_{GL} = \frac{1}{2} j R_{sh,GL} \cdot \frac{S}{T_{GL}} \cdot \frac{W^2}{\cos^2 \alpha} ; \quad (25)$$

Of final concern among the voltage drops is that in the bus line. Because of the oblique arrangement of the grid lines, it should not be necessary to extend the bus line over the whole length L of the cell (Fig. 4). In fact, it might be hoped that additional losses incurred by the oblique arrangement of the grid lines could be, at least in part, compensated through the reduced length of the bus line. Thus, this length is chosen so that the bus line extends just far enough to

FIG. 5 Sketch of one of the two triangels at the far end of the bus line, with explanation of the geometric relationships

connect with the last full-length grid line on the unit field. A separate arrangement will be made for connecting the remaining grid lines which have less than full length. The voltage drop in the bus line is given by the definite integral:

$$\Delta V_{BL} = j \frac{R_{sh,B}}{T_{BL}} \int_{L-W \tan \alpha}^0 (W^2 \tan \alpha + Wx) dx \quad (26)$$

Solving the integral and consolidating terms leads to the form:

$$\Delta V_{BL} = \frac{1}{2} R_{sh,BL} j \frac{L W}{T_{BL}} \frac{S}{S + T_{GL}} [L - W \tan \alpha] ; \quad (27)$$

For consideration of the grid lines in the triangular end portions of the unit field, only the grid lines of less than full length are of interest, which means of length less than given by $W/\cos \alpha$. Four triangles are of concern here, two each of which are symmetrically arranged around the center line of the unit field (Fig. 4). One of these pairs is located at the far end of the unit field, that is beyond the end of the bus line. The other pair is located near the base of the bus line where normally the interconnection to the next cell will be made.

For the far-end triangle, the length $\ell_{GL,n}$ of the n -th grid line is defined according Fig. 5 as:

$$\ell_{GL,n} = (W \tan \alpha - \ell_{VL,n}) \frac{1}{\sin \alpha} ; \quad (28)$$

with n counting from the last grid line of full length. The length $\ell_{VL,n}$ of the corresponding vertical connecting line

is given by:

$$\ell_{VL,n} = n(S + T_{GL}) \frac{1}{\cos \alpha} ; \quad (29)$$

The maximum number $n_{\max}$ of grid lines of less than full length in this triangle is then:

$$2n_{\max} + 1 = 2 \frac{W \tan \alpha \cos \alpha}{S + T_{GL}} ; \quad (30)$$

This relationship, however, would truly apply only if the right hand side were an integer. The proper value for $n_{\max}$ will be obtained by truncating to the next lower integer value from that given by one half of the right hand side of eq. (30):

$$n_{\max} = \left\lfloor \frac{W \sin \alpha}{S + T_{GL}} \right\rfloor \text{ truncate to integer} ; \quad (31)$$

Using this relationship, eq. (28) can be transformed into:

$$\ell_{GL,n} = (n_{\max} - n) \frac{S + T_{GL}}{\sin \alpha \cos \alpha} ; \quad (32)$$

The total current contributed by each grid line is then determined by:

$$I_n = S \cdot \ell_{GL,n} \cdot j ; \quad (33)$$

which, by use of eq. (32), takes the form:

$$I_n = (n_{\max} - n) \frac{S(S + T_{GL})}{\sin \alpha \cos \alpha} j ; \quad (34)$$

The grid lines of less than full length need to be connected to the bus line which ends at the distance $W \cdot \tan \alpha$ from the far end of the unit field. These connections shall be accomplished

by lines which form extensions of the bus line (running in the same direction as the bus line) and have the length $\ell_{VL,n}$ given by eq. (29), and the width $T_{VL,n}$. The voltage drop $\Delta V_{GL,FT}$ in the total grid line of the far triangle, including the inclined grid line portion and the connection to the bus line, is then given by:

$$\Delta V_{GL,FT} = j \frac{(n_{\max} - n) S(S + T_{GL})}{\sin \alpha \cos \alpha} \left\{ \frac{1}{2} \frac{R_{sh,GL}}{T_{GL}} \ell_{GL,n} + \frac{R_{sh,GL}}{T_{VL,n}} \ell_{VL,n} \right\}; \quad (35)$$

T_{GL} refers to the width of the inclined portions of the grid lines which has been maintained constant for all grid lines on the cell. By use of eq. (28) and (29), eq. (35) can be transformed into:

$$\Delta V_{GL,FT} = j R_{sh,GL} \frac{S(S + T_{GL})}{\sin \alpha \cos \alpha} (n_{\max} - n) \left\{ \frac{(n_{\max} - n)(S + T_{GL})}{2 T_{GL} \sin \alpha \cos \alpha} + \frac{n(S + T_{GL})}{T_{VL,n} \cos \alpha} \right\}; \quad (36)$$

Since all the grid lines of the far triangle are connected to the bus line at the same point, they shall be designed to have an identical voltage drop ΔV_{GL} , which shall be equal to that obtained from application of eq. (24). Equation (36) can then be solved for the width $T_{VL,n}$ of the connecting portion of the grid line:

$$T_{VL,n} = \frac{2 T_{GL} n (n_{\max} - n) \sin \alpha}{2 \Delta V_{GL,FT} T_{GL} \sin^2 \alpha \cos^2 \alpha - (n_{\max} - n)^2 j R_{sh,GL} S(S + T_{GL})^2}; \quad (37)$$

FIG. 6 Sketch of one of the two triangles at the near end of bus line, with explanations of the geometric relationships

Similar considerations are performed for the near-end triangle. In this triangle, there are $m_{\max} = n_{\max}$ inclined grid lines of less than full length. The length $\ell_{GL,m}$ of the m -th grid line is determined by:

$$\ell_{GL,m} = \frac{W - \ell_{HL,m}}{\cos \alpha} ; \quad (38)$$

These grid lines also do not meet the bus line, unless a special connection is made. Here, the connecting lines run normal to the bus line, along the near edge of the solar cell (Fig. 6). This connecting line has the length $\ell_{HL,m}$:

$$\ell_{HL,m} = m \frac{S + T_{GL}}{\sin \alpha} ; \quad (39)$$

Using eq. (38), (39), and (31), the grid line length can be expressed as:

$$\ell_{GL,m} = (m_{\max} - m) \frac{S + T_{GL}}{\sin \alpha \cos \alpha} ; \quad (40)$$

in complete analogy to $\ell_{GL,n}$ of eq. (32). Again, a voltage drop for the grid line plus the connecting line is obtained, and again the voltage drop is considered the independent variable, from which the width $T_{HL,m}$ of the connecting line is determined. Thus, for the connecting line between the m -th grid line and the bus line, the width is:

$$T_{HL,m} = \frac{2 T_{GL} m (m_{\max} - m) \cos \alpha}{2 \Delta V_{GL,NT} T_{GL} \sin^2 \alpha \cos^2 \alpha - (m_{\max} - m)^2 j R_{sh,GL} S (S + T_{GL})^2} ; \quad (41)$$

It should be noted, that the ΔV_{GL} values used in eq. (37) and (41) are the end-point voltage drops, which are obtainable from the desired effective voltage drops through the shape multiplier discussed in the preceding section.

With all the line dimensions determined, the question of the area coverage by metal can now be attacked. The total number k_{GL} of grid lines to be used, that is full-length lines and partial length lines added together to make full length, is:

$$k_{GL} = \frac{L}{(S + T_{GL})/\cos\alpha} ; \quad (42)$$

and the area of each of these k_{GL} grid lines is given by:

$$A_{GL,k} = T_{GL} \cdot l_{GL} = \frac{T_{GL} W}{\cos\alpha} ; \quad (43)$$

Thus, the total area covered by all grid lines is:

$$A_{GL} = \frac{2 L W T_{GL}}{(S + T_{GL})} ; \quad (44)$$

Equation (44) shows that the area covered is independent of the angle of the grid lines, as long as their width T_{GL} and their normal spacing S are maintained constant. However, constant width T_{GL} , independent of the grid line inclination angle α , results in a varying voltage drop according to eq. (24).

The area covered by the bus wire is expressed by:

$$A_{BL} = (L - W \tan\alpha) T_{BL} ; \quad (45)$$

and the total area covered by the connecting lines in the triangles is determined by:

$$A_{CL} = \sum_{n=1}^{n_{\max}} \left(T_{VL,n} \frac{S + T_{GL}}{\cos \alpha} \right) + \sum_{m=1}^{m_{\max}} \left(T_{HL,m} \frac{S + T_{GL}}{\sin \alpha} \right); \quad (46)$$

A numerical example shall be used to demonstrate the application of the relationships developed, and to illustrate the impact of oblique arrangements of the grid lines. The unit field shall have the width $W = 2$ cm, and may be a part of a square solar cell of dimension $L = 10$ cm. The grid line spacing shall be $S = 1.96$ mm, and the grid line width $T_{GL} = 40$ μm , so that the area coverage by grid lines is 0.80 cm^2 . The sheet resistance $R_{sh,FL}$ of the front layer shall be 35Ω , and that of the grid lines $R_{sh,GL} = 1.7 \cdot 10^{-3} \Omega$, corresponding to $10 \mu\text{m}$ thick copper conductors. The current density shall be $j = 0.03 \text{ A cm}^{-2}$. Applying eq. (23), the end-point voltage drop obtained for the front layer is 5.04 mV . Using eq. (25) yields an end-point voltage drop of 5 mV over the grid lines arranged normal to the bus line. For a grid line inclination angle of 30° , the grid line voltage drop would be 33% greater, or 6.67 mV . To maintain the voltage drop equal to that of the normal grid line case, the width of the grid lines could be corrected to $T_{GL} = 53.3 \mu\text{m}$, for an area coverage of 1.066 cm^2 .

The bus line voltage drop is obtained from eq. (27). In order to make this end-point voltage drop also 5 mV , a bus line width T_{BL} of 0.36 mm is obtained for the case of normally arranged grid lines, assuming that the bus line is a copper wire of circular cross section. The bus line area coverage is 0.36 cm^2 . To obtain the same voltage drop for the slightly shorter bus line to be used with the grid lines

of 30° inclination angle, the bus wire diameter needs to be only $T_{BL} = 0.34 \text{ mm}$, and the area coverage 0.30 cm^2 . Still needed is the determination of the lines in the triangles for the case of 30° inclination of the grid lines. Equation (44) includes the area coverage by the grid lines of less than full length, and application of eq. (29), (37), (39), (44), and (46) yields an area coverage of $0.88 \cdot 10^{-2} \text{ cm}^2$ and $2.66 \cdot 10^{-2} \text{ cm}^2$ for the connecting lines in the far and near triangles, respectively. Summing up the area coverage contributions for the normally arranged grid lines, the total area covered by metal is found to be 1.16 cm^2 , or 2.9% of the unit-field area. In contrast, for the grid lines inclined under a 30° angle to the bus line, the total area covered by metal amounts to 1.40 cm^2 , or 3.5% of the unit-field area, for the condition of equal total voltage drop from all contributions. This area coverage is 20% greater than that in the case of normally arranged grid lines. This additional area coverage amounts to a loss of 0.60% of the power output of the solar cell, or about one tenth of a percentage point in efficiency, incurred solely from the inclined arrangement of the grid lines.

The preceding result thus leads to the clear conclusion that normally arranged grid lines are to be used, if the power output from the solar cell is to be optimized. On the other hand, the loss of power output is not large for small inclination angles.

IV. Grid and Bus Line Pattern Optimization

The task of a grid and bus line pattern optimization is to minimize the power loss connected with the various series resistance elements of the front region (usually the diffused layer) and the front contact structure. These losses consist of the series resistance voltage drops as well as the partial shading of the frontal surface of the solar cell by metal which is used to reduce these series resistance losses. As was shown in the second section of the preceding quarterly report, the power output of a real solar cell, with series resistance, can be well approximated by the power output of the ideal cell without series resistance, minus the power dissipated in the various resistive elements. It had also been shown there that a higher power output can be obtained by rematching the cell to a slightly lower maximum power point current than found for the ideal cell, but that the improvement in power output is, for most practical purposes, negligibly small.

The power output for the ideal solar cell of total area A_{tot} and of light-sensitive area A_{eff} can be approximately described by:

$$P = j A_{\text{tot}} V_d = j_o A_{\text{tot}} (e^{\frac{qV_d}{kT}} - 1) V_d - j_L A_{\text{eff}} V_d ; \quad (47)$$

where V_d refers to the voltage appearing across the pn-junction itself ("diode voltage"!). The maximum power output available can be found from setting the derivative of the power output with respect to the junction voltage, equal to zero:

$$\frac{dP}{dV_d} = 0 = j_{Be} e^{BV_{d,mp}} V_{d,mp} + j_o (e^{BV_{d,mp}} - 1) - j_L \frac{A_{eff}}{A_{tot}} ; \quad (48)$$

The notation:

$$\frac{q}{kT} = B \quad (48a)$$

will be used here throughout. Equation (48) can be transformed into an expression for the exponential term as function of the light generated current j_L , the saturation current j_o , and the maximum power point voltage across the pn-junction $V_{d,mp}$:

$$e^{BV_{d,mp}} = \frac{j_L \frac{A_{eff}}{A_{tot}} + j_o}{j_o} \frac{1}{BV_{d,mp} + 1} ; \quad (49)$$

The maximum power point current j_{mp} can be approximately described by the commonly used solar cell equation:

$$j_{mp} A_{tot} = j_o A_{tot} (e^{BV_{d,mp}} - 1) - j_L A_{eff} ; \quad (50)$$

Equation (50), with the same approximation discussed in connection with eq. (47), gives the current which flows out of the solar cell when the voltage $V_{d,mp}$ appears across the pn-junction.

Equations (47) and (50) represent an idealized current-voltage characteristic which, however, adequately describes the real characteristics near the maximum power point in very well designed and fabricated solar cells in normal solar cell operation. For cells of lower quality, a second exponential term should be included to describe the depletion region recombination current. In addition, current flow through a shunt

resistance is often observed, and there can be other spurious current components, which all represent unnecessary losses. They are, however, usually omitted from maximum power calculations. In addition, under high-level injection conditions, deviations from the simple exponential characteristics of eq. (47) and (50) can occur.

Using eq. (49), eq. (50) can be transformed to:

$$j_{mp} = (j_L \frac{A_{eff}}{A_{tot}} + j_o) \frac{1}{BV_{d,mp} + 1} - j_o - j_L \frac{A_{eff}}{A_{tot}}; \quad (51)$$

which can be simplified to the form:

$$j_{mp} = - \frac{V_{d,mp}}{V_{d,mp} + \frac{1}{B}} (j_L \frac{A_{eff}}{A_{tot}} + j_o); \quad (52)$$

Since the saturation current density j_o is usually many orders of magnitude smaller than the light generated current density j_L , eq. (52) can be well approximated by:

$$j_{mp} \approx - \frac{V_{d,mp}}{V_{d,mp} + \frac{1}{B}} j_L \frac{A_{eff}}{A_{tot}}; \quad (52a)$$

Using eq. (52), the maximum power output of the solar cell with zero series resistance can be written as:

$$P_{d,mp} = V_{d,mp} j_{mp} A_{tot} = - V_{d,mp} \cdot \frac{V_{d,mp}}{V_{d,mp} + \frac{1}{B}} \cdot j_L \left(\frac{A_{eff}}{A_{tot}} + \frac{j_o}{j_L} \right) A_{tot}; \quad (53)$$

which can be approximated by:

$$P_{d,mp} \approx - j_L \frac{V_{d,mp}}{V_{d,mp} + \frac{1}{B}} A_{eff}; \quad (53a)$$

In a real solar cell which experiences voltage drops

due to finite resistance components, the terminal voltage V_t will differ from the voltage across the junction V_d by the total voltage drop ΔV_R :

$$V_t = V_d + \Delta V_R; \quad (54)$$

Rewriting this relationship for the maximum power point voltage yields:

$$V_{t,mp} = V_{d,mp} + \Delta V_{R,mp}; \quad (55)$$

The voltage drop $\Delta V_{R,mp}$ consists of a number of individual voltage drops across the various series resistance components which occur in the path of the current flow through the solar cell. In the ideal case, these voltage drops can be expressed according to Ohm's law by an equivalent series resistance value for each individual effect, multiplied by the total current flowing through the device:

$$\Delta V_{R,mp} = \sum_{i=1}^{N_R} \Delta V_{i,mp} = I_{mp} \sum_{i=1}^{N_R} R_{s,i}; \quad (56)$$

The maximum power output $V_{t,mp}$ from the terminals of the real solar cell with finite series resistance can then be expressed as:

$$P_{t,mp} = V_{t,mp} \cdot j_{mp} \cdot A_{tot}; \quad (57)$$

and, after inserting eq. (53) and (55), as:

$$P_{t,mp} = -(V_{d,mp} + V_{R,mp}) \frac{V_{d,mp}}{V_{d,mp} + \frac{1}{B}} j_L \left(\frac{A_{eff}}{A_{tot}} + \frac{j_o}{j_L} \right) A_{tot}; \quad (58)$$

Expressing the light-exposed area through the total area and the area covered by metal (shaded area) A_{shade} according to:

$$A_{\text{eff}} = A_{\text{tot}} - A_{\text{shade}} ; \quad (59)$$

permits writing eq. (58) as:

$$P_{t,mp} = P_{d,mp,id} + \frac{V_{d,mp}^2}{V_{d,mp} + \frac{1}{B}} j_L A_{\text{shade}} + \Delta V_{R,mp} j_{mp} A_{\text{eff}} ; \quad (60)$$

where $P_{d,mp,id}$ stands for the ideal maximum power output with $A_{\text{eff}} = A_{\text{tot}}$.

Equation (60) represents the form:

$$P_{t,mp} = P_{d,mp,id} + \Delta P_R = P_{d,mp,id} \left(1 + \frac{\Delta P_R}{P_{d,mp,id}} \right) ; \quad (61)$$

It may be noted that $P_{t,mp}$, $P_{d,mp,id}$, and $\Delta V_{R,mp}$ are negative quantities in solar cell operation, according to eq. (52), (53), (56), and (57). Equation (58) thus describes the power output of the real solar cell by the power output of the ideal solar cell reduced by the power losses related to series resistance, ΔP_R . Only the relative power loss $\frac{\Delta P_R}{P_{d,mp}}$ is of interest for the further discussions, which therefore concentrate on minimizing this relative power loss. This relative power loss is represented by:

$$\frac{\Delta P_R}{P_{d,mp,id}} = \frac{A_{\text{shade}}}{A_{\text{tot}}} \frac{1}{1 + \frac{j_o}{j_L}} - \frac{\Delta V_{R,mp}}{V_{d,mp}} \frac{\frac{A_{\text{eff}}}{A_{\text{tot}}} + \frac{j_o}{j_L}}{1 + \frac{j_o}{j_L}} ; \quad (62)$$

which is derived from eq. (60) by use of eq. (53). Neglecting second or higher order terms in the small quantities, eq. (62) is readily re-expressed as:

$$\frac{\Delta P_R}{P_{d,mp,id}} \approx \frac{A_{shade}}{A_{tot}} - \frac{\Delta V_{R,mp}}{V_{d,mp}} ; \quad (63)$$

which contains one term each representing the relative voltage loss and the relative area loss.

Following the nomenclature of Fig. 7, the total area can be expressed as:

$$A_{tot} = L_1 L_2 ; \quad (64)$$

and the shaded area as:

$$A_{shade} = n_{GL} T_{GL} W \cdot 2n_{BL} + n_{BL} T_{BL} L_1 ; \quad (65)$$

where the number of grid lines n_{GL} is given by:

$$n_{GL} = \frac{L_1}{S + T_{GL}} ; \quad (66)$$

and the number of bus lines n_{BL} by:

$$n_{BL} = \frac{L_2}{2W + T_{BL}} ; \quad (67)$$

Thus, the shaded area according to eq. (65) can be expressed as:

$$A_{shade} = L_1 L_2 \frac{2W}{2W + T_{BL}} \left(\frac{S}{S + T_{GL}} \frac{T_{GL}}{S} + \frac{T_{BL}}{2W} \right) ; \quad (68)$$

Since, for a well designed solar cell, the effective area differs from the total area only by a few percent, the second

order terms in eq. (68) can be neglected, as they have been in eq. (62), so that the shaded area can be approximated by:

$$A_{\text{shade}} \approx L_1 L_2 \left(\frac{T_{\text{GL}}}{S} + \frac{T_{\text{BL}}}{2W} \right); \quad (68a)$$

The contribution $\Delta V_{R,mp,F}$ of the front layer and the front contact structure to the $\Delta V_{R,mp}$ consists of the effective voltage drops (see section "Oblique versus normal grid lines" of this report) in the three major elements through which the current flows:

$$\begin{aligned} \Delta V_{R,mp,F} = j_{mp} \left\{ \begin{array}{l} R_{\text{sh},FL} \frac{\frac{S}{2}}{W} \cdot \frac{1}{2} \frac{S}{2} W \cdot G_{FL}(f) \frac{1}{2} H_{FL}(f) \\ \text{Front Layer} \\ + R_{\text{sh},GL} \cdot \frac{W}{T_{GL}} \cdot \frac{1}{2} \cdot SW \cdot G_{GL}(f) \frac{1}{2} H_{GL}(f) \\ \text{Grid Line} \\ + R_{\text{sh},BL} \cdot \frac{L_1}{T_{BL}} \cdot \frac{1}{2} \cdot 2n_{GL} \cdot SW \cdot G_{BL}(f) \frac{1}{2} H_{BL}(f) \end{array} \right\} \\ \text{Bus Line} \end{aligned} \quad (69)$$

As the front layer is, for all parallel-grid line systems, of uniform width, it is practical to express $\Delta V_{R,mp,F}$ relative to uniform width elements by use of a "shape factor" δ . This factor is unity for uniform width elements and decreases monotonically to $\frac{3}{4}$ for increasingly tapered elements covering equal area. δ is thus defined as:

$$\delta = \frac{G(f) H(f)}{G(1) H(1)} = \frac{3}{4} G(f) H(f); \quad (70)$$

Equation (69) then reduces to:

$$\Delta V_{R,mp,F} = \frac{1}{3} j_{mp} \left\{ R_{sh,FL} \left(\frac{S}{2} \right)^2 \delta_{FL} + R_{sh,GL} \frac{S}{T_{GL}} W^2 \delta_{GL} + R_{sh,BL} \frac{S}{S + T_{GL}} \frac{2W}{T_{BL}} L_1^2 \delta_{BL} \right\}; \quad (71)$$

Again neglecting terms expressing second order effects, and introducing:

$$x = \frac{T_{GL}}{S}; \quad (72a)$$

$$y = \frac{T_{BL}}{2W}; \quad (72b)$$

gives, from eq. (63), (71), and (72 a and b):

$$\frac{\Delta P_R}{P_{d,mp}} \approx x + y - \frac{1}{3} \frac{j_{mp}}{V_{d,mp}} \left\{ R_{sh,FL} \left(\frac{S}{2} \right)^2 \delta_{FL} + R_{sh,GL} \frac{1}{x} W^2 \delta_{GL} + R_{sh,BL} \frac{1}{y} L_1^2 \delta_{BL} \right\}; \quad (73)$$

Differentiating eq. (73) with respect to x and setting equal to zero to find the extrema, yields:

$$\frac{d}{dx} \frac{\Delta P_R}{P_{d,mp}} = 0 = 1 + \frac{1}{x^2} \frac{1}{3} \frac{j_{mp}}{V_{d,mp}} R_{sh,GL} W^2 \delta_{GL}; \quad (74)$$

or:

$$\frac{T_{GL}}{S} = W \left(\frac{1}{3} \frac{|j_{mp}|}{V_{d,mp}} R_{sh,GL} \delta_{GL} \right)^{\frac{1}{2}}; \quad (75)$$

Carrying the derivation out from the full relationships yields practically the same result as given in eq. (75), since the second order terms cancel each other in the process, so that only the higher order terms would enter the final relationship.

Taking the derivative of eq. (73) with respect to y yields the corresponding relationship:

$$\frac{T_{BL}}{2W} = L_1 \left(\frac{1}{3} \frac{|j_{mp}|}{V_{d,mp}} R_{sh,BL} \delta_{BL} \right)^{1/2}; \quad (76)$$

Equations (75) and (76) give the optimum grid line width and bus line width, but expressed relative to the spacing S between adjacent grid lines and $2W$ between adjacent bus lines, respectively. These expressions are valid when the grid and bus lines are metal layers of given sheet resistances $R_{sh,GL}$ and $R_{sh,BL}$, respectively.

It is important to note that eq. (75) and (76) represent only an expression of the optimum design compromise between shading and voltage drop for the grid lines alone and the bus lines alone, respectively, as eq. (73) and (74) indicate. The optimum design is still dependent on the grid line spacing, which determines the voltage drop from current flow within the semiconducting front layer, as described by the first term in the brackets of eq. (73). Clearly, the total voltage drop and shading are minimized for $S=0$, with the grid line shading T_{GL}/S held constant according to eq. (75). Similarly, the grid line voltage drop (second term in brackets in eq. (73)) is minimized

when the bus line spacing $2W$ approaches zero, again holding the bus line shading $T_{BL}/2W$ constant. In reality, there is no need to go this far in reducing the spacings, as other losses, such as the shadings and the bus line voltage drops, remain constant. Thus, it is adequate to reduce S and W to the level at which the losses controlled by these two quantities become insignificant relative to the constant losses.

For the grid lines, this approach may still result in a grid line width T_{GL} , which is difficult to produce. Then, in practice, the metallization designer will select the smallest grid line width $T_{GL,pract}$ which can be cost-effectively produced, considering process costs and yields as well as differences in solar cell value consequent to the efficiency differences, which result from the metallization design variations.

When such a lower limit is set on the grid line width, the determination of an optimum shading ratio according to eq. (75) is no longer appropriate. By using a grid line shading ratio larger than the optimal value obtained from eq. (75), the relative front layer sheet voltage drop can be considerably reduced, since it is proportional to S^2 . In fact, when the grid line width is held constant, eq. (73) can be optimized with respect to the grid line spacing S . Setting the derivative of eq. (73) with respect to S equal to zero, yields:

$$S^3 + 2 \frac{R_{sh,GL}}{R_{sh,FL}} \frac{W^2}{T_{GL,pract}} S^2 - \frac{6 V_{d,mp}}{|j_{mp}|} \frac{T_{GL,pract}}{R_{sh,FL}} = 0; \quad (77)$$

The solution of a cubic equation is generally cumbersome.

However, if:

$$\frac{R_{sh,FL}^3}{R_{sh,FL}^2} \ll \frac{|j_{mp}|}{V_{d,mp}} \frac{T_{GL,pract}^4}{3^4 (2W)^6}; \quad (78)$$

the following approximate solution is valid:

$$S_{opt} = \left(\frac{6 V_{d,mp}}{|j_{mp}|} \frac{T_{GL,pract}}{R_{sh,FL}} \right)^{1/3} - \frac{2^{4/3}}{3} \frac{R_{sh,GL}}{R_{sh,FL}} \frac{W^2}{T_{GL,pract}}; \quad (79)$$

In many cases, the second term of eq. (79) is small compared to the first.

It may also be noted that the application of bus lines is only indicated when their sheet resistance is significantly lower than that of the grid lines. When the sheet resistances of the two types of lines are equal ($R_{sh,Lines}$), assuming the shape factor δ to be unity, then, with use of the optimum shading ratios T_{GL}/S and $T_{BL}/2W$ according to eq. (75) and (76), respectively, eq. (73) becomes:

$$\frac{\Delta P_{R,mp}}{P_{d,mp}} = \left(\frac{|j_{mp}|}{3 V_{d,mp}} R_{sh,Lines} \right)^{1/2} 2 (L_1 + W) + \frac{|j_{mp}|}{3 V_{d,mp} R_{sh,FL}} \left(\frac{S}{2} \right)^2; \quad (80)$$

It is readily shown that, for a structure containing only grid lines, this time of length L_1 , the same relationship as in eq. (80) is obtained, except that W does not appear. Thus, the addition of bus lines is, in this case, detrimental.

Numerical Examples:

For a 10 cm x 10 cm cell with $|j_{mp}| = 0.03 \text{ mA cm}^{-2}$ and $V_{d,mp} = 0.5V$, and a grid line sheet resistance $R_{sh,GL} = 1.7 \cdot 10^{-3} \Omega$, corresponding to 10 μm thick lines of copper with bulk resistivity, and without bus lines, the optimum shading ratio T_{GL}/S is 5.83%. At a grid line spacing of 2 mm, and a line width of 117 μm according to the shading ratio, the total series-resistance-connected losses of the front structure amount then to 12.4% of the ideal solar cell output. In this number are contained, outside of the shading, relative voltage drops of 5.83% in the grid lines and 0.7% in the front layer itself. Reducing the grid line width and spacing further, while keeping the shading ratio at its optimum value, would not yield a significant improvement, since the total losses could at most be reduced by 0.7 percentage points, or 5.6% of the total losses.

For a system with bus lines of the same sheet resistance as the grid lines, and all data equal to those of the preceding example, eq. (76) yields a bus line shading ratio of 5.83%. With this, the relative bus line voltage drop according to the fifth term on the right hand side of eq. (73) also becomes 5.83%. Choosing a bus line spacing $2W = 1 \text{ cm}$, the

optimum bus line width is thus 583 μm . With this bus line spacing, the optimum grid line shading would then be, according to eq. (75), 0.29%. With the minimum practical line width taken, for this example, as 20 μm , the grid line spacing S_{opt} would be 6.86 mm. The relative grid line voltage drop, according to the fourth term of eq. (73), is then also 0.29%, and the relative front layer sheet voltage drop, according to the third term of that equation, 8.2%. Thus, the total series-resistance-connected front structure losses are 20.4% of the ideal power output, compared to 12.4% for the grid-line-only structure.

This design, while giving the lowest possible bus line and grid line losses, does not provide the lowest total loss, since a lower practical limit was set for the grid line width. It is readily seen that increasing the shading ratio by a factor of four, that is to 1.17%, which means reducing S to 1.72 mm, decreases the relative front layer sheet voltage drop by a factor of 16, so that the sum of all losses becomes 13.4%, still more than in the grid-line-only case. It may be noted that eq. (79) gives 1.738 mm for the optimum value of S with the chosen value of $T_{\text{GL,pract}}$.

End of Numerical Examples.

As it has been found that the application of bus lines of the same sheet resistance as the grid lines is of no use, and as the front structure losses, even with the lowest practically achievable sheet resistance in deposited metal layers, are near 12% in 10 cm x 10 cm solar cells, the attention will necessarily shift to thicker bus lines, which can yield at

least an order of magnitude lower sheet resistance. This means an overlay of a bulk conductor, such as a copper wire. In this case, T_{BL} becomes equal to the wire diameter, and the "effective sheet resistance" is then:

$$R_{sh,BL} = \rho_{BL} \frac{4}{\pi T_{BL}} ; \quad (81)$$

where ρ_{BL} is the resistivity of the bus line (wire) material. Introducing eq. (81) into the fifth term of the right hand side of eq. (73) yields:

$$\begin{aligned} \frac{\Delta P_{R,mp}}{P_{d,mp}} = & \frac{T_{GL}}{S} + \frac{T_{BL}}{2W} + \frac{|j_{mp}|}{3 V_{d,mp}} \left\{ R_{sh,FL} \left(\frac{S}{2} \right)^2 \delta_{FL} \right. \\ & \left. + R_{sh,GL} \frac{S}{T_{GL}} W^2 \delta_{GL} + \frac{4}{\pi} \rho_{BL} \frac{2W}{T_{BL}} L_1^2 \delta_{BL} \right\}; \quad (82) \end{aligned}$$

It may be noted that the use of a wire with constant diameter along its length leads to $\delta_{BL} = 1$, just as a parallel grid line system entails $\delta_{FL} = 1$.

Equation (82) can, in contrast to eq. (73), be optimized for T_{BL} alone, rather than the shading ratio $\frac{T_{BL}}{2W}$, since the bus line sheet resistance is now also a function of T_{BL} . Thus:

$$\frac{d \left(\frac{\Delta P_{R,mp}}{P_{d,mp}} \right)}{d T_{BL}} = 0 = \frac{1}{2W} - \frac{|j_{mp}|}{3 V_{d,mp}} \frac{16}{\pi} \rho_{BL} \frac{W L_1^2}{T_{BL}^3}; \quad (83)$$

which resolves to:

$$T_{BL} = \left(\frac{32}{3\pi} \frac{|j_{mp}| \rho_{BL}}{V_{d,mp}} W^2 L_1^2 \right)^{1/3}; \quad (84)$$

TABLE I

DESIGN		OPTIMUM	NEAR OPTIMUM	THIN Cu	Ni	PLATED BUS LINES	NEAR OPTIMUM	SCREEN PRINTED Ag
NO. OF BUS LINES (SPACING)	- (CM)	7 (1.428)				→	3 (3.333)	→
BUS LINE WIDTH (DIAMETER)	MM	0.255 DIA		→		0.75	0.361 DIA	→
BUS LINE THICKNESS (GAUGE)	μM (B&S)	(30 GA.)		→		10 (Cu)	(27 GA.)	→
NO. OF GRID LINES (SPACING)	- (MM)	65 (1.53)				→	40 (2.50)	→
GRID LINE WIDTH	μM	12.5	25				→	127
GRID LINE THICKNESS	μM	5	10	2	10		→	10 (FIRED)
GRID MATERIAL	-	Cu		→	Ni	Cu	→	SINTERED Ag
BUS SHADING	%	1.79	1.79	1.79		5.25	1.08	1.08
BUS LOSS	%	0.96	0.94	0.94		4.46	1.12	1.03
GRID SHADING	%	0.82	1.63	1.63		1.55	1.00	5.08
GRID LOSS	%	0.42	0.10	0.51		0.09	0.94	0.49
FRONT LAYER LOSS	%	0.41	0.41	0.41		0.39	1.11	0.98
BASE LOSS (200 μM 10CM; 10 μM Cu)	%	0.46	0.46	0.48	1.82	0.44	0.49	0.47
TOTAL POWER LOSS	%	4.9	5.3	5.8	7.1	12.2	5.7	9.1
CELL EFFICIENCY	%	16.36	16.29	16.20	15.98	15.10	16.22	15.63
MODULE EFFICIENCY	%	15.34	15.27	15.19	14.98	14.16	15.21	14.65
CELL VALUE	\$/M ²	86.31	85.46	84.49	81.93	71.94	84.73	77.91
	¢/W(PK)	56.3	56.0	55.6	54.7	50.8	55.7	53.2
DIFFERENCE IN VALUE	\$/M ²	REFERENCE	-0.85 REF.	-	-	-	-1.58 REFERENCE	-
				-0.97	-3.53	-13.52		-6.82

Inserting the optimum grid line shading ratio from eq. (75) and the optimum bus line width T_{BL} from eq. (84) into eq. (82) permits determination of the actual relative power loss experienced in the front structure:

$$\frac{\Delta P_{R,mp}}{P_{d,mp}} = \frac{|j_{mp}|}{3 V_{d,mp}} R_{sh,FL} \left(\frac{S}{2}\right)^2 + 2W \left(\frac{|j_{mp}|}{3 V_{d,mp}} R_{sh,GL} \delta_{GL} \right)^{1/2} + \left(\frac{9 |j_{mp}| \rho_{BL}}{2\pi V_{d,mp}} L_1^2 \right)^{1/3} \cdot \frac{1}{W^{1/3}} ; \quad (85)$$

The first term on the right hand side of eq. (85) describes the relative voltage drop in the front layer sheet, the second term the sum of the equal shading and voltage drop losses from the grid lines, and the third term the shading and voltage drop losses from the bus lines. Equation (85) is a function of the bus line spacing W , which exhibits a definite minimum in the sum of the grid line and bus line losses for the appropriate value of W . This optimum bus line spacing, for the use of round wires for the bus lines, is given by:

$$2W = \left(\frac{3 \rho_{BL}^2 V_{d,mp}}{\pi^2 R_{sh,GL}^3 \delta_{GL}^3 |j_{mp}|} \right)^{1/8} L_1^{1/2} ; \quad (86)$$

With such use of round wires as bus line overlay, the losses connected with the front structure in 10 cm x 10 cm solar cells can be reduced to under 5%, from about 12% with grid lines only, or with grid lines plus plated bus lines.

The sensitivity of the performance of large area solar cells to the grid and bus line design is illustrated in Table I.

In the computations for this table, it was assumed that deposited metal layers can be produced only with a 2.5:1 aspect ratio, that is, that the width of the line has to be at least 2.5 times its thickness. The first column shows the data for the optimum design, based on deposited grid lines of 5 μm thickness and bulk conductivity of copper. The bus lines are copper wires of circular crosssection. The semiconducting base region and the metal base contact, assumed to cover the entire back surface with 10 μm thick copper of bulk conductivity, contribute together a loss due to voltage drop of 0.46%. All contact resistances have been assumed to be zero. Including this loss from the base, the total shading and voltage drop loss is 4.9% of the ideal power output.

In the second column, a grid line width of 25 μm has been used instead of the 12.5 μm width in the optimum design. Simultaneously, the grid line thickness has been increased to 10 μm . The consequence is, that this "near optimum design" has 0.4 percentage points higher loss than the optimum design, for a total loss of 5.3%.

The third column is split, showing equal sheet resistances by use of either a 2 μm thick copper deposit or 10 μm of nickel for the grid lines. In the latter case, the base contact was also assumed to be of 10 μm thick nickel. While the former case has only a small influence, the latter results in total losses of 7.1%.

The fourth column displays data on a case with plated bus

lines, similar to some discussed above.

While the bus structure in these first four columns contained seven bus lines with 1.43 cm spacing, column 5 shows another "near optimum design" with three bus lines of somewhat heavier gauge wire, and a reduced number of grid lines, namely forty. This design shows a total power loss of 5.7%.

Column 6 uses the same design as column 5, but applies printed thick film silver at the projected minimum line width of 127 μm for the grid lines. The line thickness is 10 μm after sintering, about the maximum achievable with a single printing. The conductivity is approximately one third that of bulk silver, as generally experienced with sintered thick film silver layers. The disadvantage of the use of the thick film silver lies primarily in the large shading resulting from the increased line width, which leads to a total relative power loss of 9.1%.

The line marked "cell efficiency" in Table I shows the efficiency which would be obtained by use of the various metallization designs on an otherwise identical cell. The following line below, labelled "module efficiency", is obtained from the cell efficiency by multiplying with 0.96 and 0.975 to account for packing factor and assembly losses. Using an area related BOS price of $\$60/\text{m}^2$ as an example, and a module materials and assembly price of $\$28/\text{m}^2$, an economical "cell value" can be established for which the complete system can deliver power at an equal price. This cell value is a function of the efficiency. These cell values, expressed both in $\$/\text{m}^2$

and in $\$/W(\text{peak})$, are given in the two lines below the module efficiency. The last two lines, finally, show the differences in the economic value resulting from the efficiency differences due to the design variations in the various columns. The second to last line uses the cell value of the "optimum design" of column 1 as the reference, and lists the value differences of the two "near optimum designs" of column 2 and 5. In the last line, the values of the cells with "near optimum design" have been taken as reference, and the value differences of the cells with design variations from these given. It is seen that the differences in cell value form a substantial part of the entire metallization process cost and are therefore very worthwhile investigating. It has, however, also to be observed that these cell values are based on the $\$60/m^2$ area related BOS price assumption, and that the differences will be larger or smaller for higher or lower BOS prices, respectively.

The use of "high" bus lines, such as round wires, while extremely beneficial from the efficiency viewpoint, can cause some problems. The first is that of thermal expansion, which leads to the need for longitudinally periodic, rather than continuous attachment of the bus wire to the solar cell, with provision for stress relief between the attachment points. Next, the high bus lines will require changes in module assembly procedure, requiring either preformed cover glass to avoid too thick a gap to be filled with potting material, or a conformal coating.

V. Design Rules for Front Metallization for Large Area Solar Cells

From the preceding analysis, a definitive set of design rules for the front metallization of large area solar cells has been derived (Table II). Their observation should help cell designers to avoid many of the previously experienced pitfalls and to utilize the most cost-effective contact design and metallization system.

It should be noted that these design rules are not concerned with the problem of contact resistance which still seems to be in need of adequate explanation and reduction to engineering design principles.

TABLE II

DESIGN RULES
for Front Metallization for Large Area Solar Cells

1. Observe: Careless metallization design is costly.
2. Select conductor metal of the highest practical conductivity.
3. Select deposition processes which approach bulk conductivity as closely as practical.
4. Each higher level in the hierarchy of conductors needs a much lower sheet resistance than the preceding level. This leads to the "sky scraper rule" for the bus lines: Build high rather than wide.
5. If the bus lines cannot have a sheet resistance small compared to the grid lines, omit the bus lines. Proceed directly to 10.
6. Select the bus line spacing, for bus lines of round wire, according to:

$$2W = \left(\frac{3}{\pi^2} \frac{\rho_{BL}^2}{R_{sh,GL}^3 \delta_{GL}^3} \frac{V_{mp}}{|j_{mp}|} \right)^{1/8} L_1^{1/2}$$

7. Select bus line wire diameter according to:

$$T_{BL} = \left(\frac{32}{3\pi} \frac{|j_{mp}| \rho_{BL}}{V_{mp}} L_1^2 W^2 \right)^{1/3}$$

8. For rectangular bus wires of height-to-width ratio k , multiply each π by $4k/\pi$.
9. For bus lines of constant sheet resistance $R_{sh,BL}$, rather than thickness directly proportional $R_{sh,BL}$ to width, as in round or rectangular wires, the relationship:

$$\frac{T_{BL}}{2W} = L_1 \left(\frac{|j_{mp}|}{3 V_{mp}} R_{sh,BL} \delta_{BL} \right)^{1/2}$$

applies, instead of 6.) and 7.). Choose W then as small as practical, considering 13.) and 14.).

10. Arrange grid lines normal to bus lines, and parallel to each other.

(Continued on next page)

11. Select grid line width as small as practical, commensurate with acceptable production costs and yields and solar cell value differences resulting from the consequent efficiency differences.

12. Select grid line spacing S according to:

$$S = \left(\frac{6 V_{mp}}{|j_{mp}|} \frac{T_{GL}}{R_{sh,FL}} \right)^{1/3} - \frac{2^{4/3}}{3} \frac{R_{sh,GL} \delta_{GL}}{R_{sh,FL}} \frac{W^2}{T_{GL}}$$

13. Check that

$$\frac{T_{GL}}{S} \approx \left(\frac{1}{3} R_{sh,GL} \delta_{GL} \frac{|j_{mp}|}{V_{mp}} \right)^{1/2} W$$

14. Check that

$$S \leq 2 \cdot \left[\frac{(R_{sh,GL} \delta_{GL})^{1/2}}{R_{sh,FL}} \left(\frac{3 V_{mp}}{|j_{mp}|} \right)^{1/2} W \right]^{1/2}$$

15. If checks 13.) and 14.) are negative, select S as small as possible in view of 11.), but not significantly larger than given by 14.). If T_{GL}/S is large compared to right hand side of 13.), use the smallest practical value for T_{GL} , if pattern resolution is limiting. If grid line width-to-thickness ratio is limiting, reduce thickness (increase $R_{sh,GL}$), to find T_{GL} and $R_{sh,GL}$ values for least power loss.
16. The "shape factor" δ varies from 0.75 for fully tapered grid lines to unity for uniform width lines of equal shading.

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VI. Conclusions

The analysis of the metallization design has provided considerable insight into the requirements to be fulfilled in a low-loss design for large area solar cells. These requirements have been listed together in a set of Design Rules, contained in Table II. It has been shown that the total shading and voltage drop losses can be held to about 5% in 10 cm x 10 cm solar cells, but that not every metallization process is capable of meeting the requirements of the low-loss design. Without close observation of the design rules, the combined series resistance related losses can easily increase to 10 and even 20% of the ideal power output.

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VII. References

- 1) Mardesich, N., DOE/JPL contract 955725, Quarterly Report in preparation.