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THIN-FILM RESISTIVE-GATE GaAs CHARGE COUPLED DEVICES

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Simulation, Design, and Fabrication of Thin-Film Resistive-Gate GaAs Charge Coupled Devices

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Computer simulation of high-speed Gallium Arsenide Charge Coupled Devices is performed using the two-dimensional semiconductor device simulation program BAMBI (Basic Analyzer for Mos and Bipolar devices). The effect of active layer thickness and doping concentration on the Charge Transfer Efficiency (CTE) and the dynamic range is investigated using different active layers. Also, different gate architectures are compared for optimum dynamic range and compatibility with GaAs MESFET technology. Both Capacitive Gate CCD (CGCCD) and Resistive Gate CCD (RGCCD) are considered. The measured performance of the fabricated GaAs CCD is compared with modelled results.

We are developing high speed GaAs CCD's for capture of single-event electro/photo transients in scientific experiments. We have adapted the two dimensional device simulation program BAMBI [1] for GaAs devices. The formation of potential wells under the biased gate is observed. The generation and collection of electrons into these potential wells are then simulated in transient mode. The transfer of the charge packet is then observed under various clocking conditions. The active layer thickness is varied to determine the effect of layer thickness on CTE and the maximum speed of operation. Both CGCCD and RGCCD [2] configurations are considered. For the case of resistive gate CCD's, the cermet (a thin skin of resistive alloy of Cr/SiO₂, forming Schottky contacts with GaAs) layer is simulated using a series of gates having distributed potentials. An example of device cross-section, clock sequence, and simulated charge transfer is shown in Figure 1. After successful simulation of charge transfer, the output sensing gate and reset gate are added with the basic cell of the GaAs CCD. The simulation results compare favorably with the measured performance of a fabricated GaAs CCD.

The simulation results of a 0.2 μm active layer GaAs RGCCD with a doping level of $3 \times 10^{17} \text{cm}^{-3}$ show that the maximum clock speed for charge transfer with reasonable CTE is about 100MHz for our particular structure. The experimental measurements of the fabricated GaAs CCD generally agree with this value. Experimentally, quick degradation of CTE is observed at higher clock frequencies; Figure 2 shows measured charge transfer in the fabricated CCD demonstrating this effect. This correlation of simulation results (obtained using a CAD tool originally intended for silicon device design) provides a powerful means to optimize the architecture of the CCD cell for maximum CTE and dynamic range. For example, the speed of charge transfer is found to be much faster for the 1.0 μm CGCCD with a doping level of $1 \times 10^{16} \text{cm}^{-3}$ than if the 0.2 μm , higher-doped thin layer is used. This is due to the higher fringing field in the thicker active layer device. Several other examples of such design optimizations will also be shown.

- [1] W. Kausel, et al., *NUPAD II Workshop*, San Diego, CA, Digest No. 105/106, (1988)
- [2] C. K. Kim, et al., *Appl.phys.lett.* vol. 20, 514 (1972)

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0.2μm Active layer GaAs RGCCD

Clock Pulses For 0.2 μm 3-Phase RGCCD

Electron concentration at time t=1.5ns

Electrostatic Potential at time t=7.0ns

Electron concentration at time t=7.0ns

Electron concentration at time t=13.0ns

Fig.1 Simulation results of a 0.2μm channel GaAs CCD showing the transfer of charge packet.

Measured electrical input and
delayed output signal at 20 MHz.

Measured electrical input and
delayed output signal at 290 MHz

Fig. 2 Photographs of measured charge transfer at two different frequencies.

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