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PHASE 2 OF THE ARRAY AUTOMATED ASSEMBLY TASK FOR THE
LOW COST SILICON SOLAR ARRAY PROJECT

Second Quarterly Report

By
Manfred Wihl

April 1978

Work Performed Under Contract No. NAS-7-100-954854

MASTER

Solarex Corporation
Rockville, Maryland

U.S. Department of Energy

Solar Energy

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MANFRED WIHL

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I. Introduction

Automation is the key factor in reaching the LSSA Project goal of 500 megawatts annual production at 50¢ per watt. Solarex is currently analyzing the potential for automating a particular process sequence. Assessment of the cell making steps for this sequence is nearly complete. Some verification work is still in progress on metallization of the cell after which we shall review and verify the module fabrication steps.

For the steps analyzed so far there seems to be no technological barrier to reaching the LSSA Project goals. The cell making steps are reviewed individually in either this report or our first quarterly report. It is appropriate at this point to review the process sequence as a whole. The costs of cell making can be divided into four categories: a) materials, b) equipment, c) utilities, and d) labor and overhead.

Labor and equipment were found to be only a small fraction of the cell making cost. This can be understood by considering a production line of equipment that processes 1/10th the Project Goal. Operating twenty hours a day for 350 days per year means a rate of 120 4" wafers per minute. Two wafers per second is an impressive flow yet in general each step can be handled by a single machine. To cite two examples, to etch wafers at this rate requires a tank volume of only about nine cubic feet and to silkscreen in groups of twelve wafers requires an easily obtained six second printing cycle. Now suppose an average machine costs \$100,000. and suppose ten different machines were required to process a raw wafer into a cell. Assuming a three year machine life the cost is \$1,000,000./150 million wafer, i.e., .67¢ per wafer for the entire process. An analysis of individual

process steps indicates that \$100,000. is surely an upper bound for most machine costs.

The sophisticated level of process control offered by microprocessor electronics assures that labor will only be required for monitoring and maintenance. Employing several persons per machine will incur a cost per wafer as small as that found for equipment costs.

In choosing between technological alternatives the quantity of energy needed and the cost of materials are the two most important factors. The process sequence chosen for verification by Solarex is an attempt to minimize the use of inherently expensive materials, e.g., by eliminating the use of silver; and to reduce energy consumption by eliminating energy intensive steps such as those requiring vacuum systems. The particular sequence analyzed by Solarex is only one possible approach to automation but since the materials and utilities cost is shown to be within the 50¢ per watt budget the sequence serves as an important example to the solar cell manufacturing community.

II. Junction Formation

A) Review and Assessment

A silicon wafer becomes a solar cell when the junction is formed. In the manufacture of optimum performance cells this step requires precise control of time, temperature, and dopant concentration. An experimental verification program was required to determine how these apparently critical parameters could be controlled in a low cost, high throughput automated production line. During this reporting period we have verified junction formation techniques that are well suited to large scale automation and yield cells with good electrical performance.

The process parameters of junction formation turn out to be much less critical than was generally believed. For example, the doping source can be applied to the wafer in various ways. We have examined the methods listed in Table 1 and find similar resulting cell characteristics independent of the method used.

The thickness gradient of the dopant is visible on the oxide layer formed after the diffusion process. However, there is no impact upon the resulting sheet resistance.

Application	
Method	Comment
dip only	relatively thick coat.
spin	thin coat, layer thickness exhibits a gradient, not harmful.
dip + spin	thin layer, better thickness control, small gradient, not harmful.
dip + dip	thick coat.
spray	excellent layer control, might consume time.
brush on	thin, uneven coat, mechanical impact to cell possible.
roll on	thin, even coat, mechanical impact to cell possible.

TABLE 1 ,DOPANT APPLICATION METHODS

Certainly the quality of the junction depends on the doping source used. Among the liquid dopants for which experiments were reported last quarter only three made suitable junctions during the short times and low temperatures needed for mass production of solar cells. These were:

Emulsitone N-250
Allied Chemical PX-10
Solarex SX-101

The commercial dopants N-250 and PX-10 are a factor of ten more expensive than SX-101, which costs about 2¢ per wafer.

Solarex's experiments verify that a cost barrier has been surmounted. An economic analysis made later in this report documents that the entire junction formation process can cost less than 5¢ per wafer.

Diffusing a junction from a doping source that has been applied as a liquid is only the first step in the junction formation sequence. After the junction is formed one terminal of our device is completely inside the other terminal. That is, the p-type material is surrounded by an n-type diffused layer. By alloying metal to one side of the cell a back contact is formed that eliminates the junction and forms an electrical connection to the bulk silicon.

The complete junction formation sequence is as follows. A 4" diameter textured wafer is sprayed or dipped with dopant. The wafer is then spun for a few seconds to remove excess liquid. The application of dopant can be done while the wafers

are in a standard wafer basket or cassette. The wafers are then unloaded onto a belt and carried through a low temperature furnace to dry the dopant. After drying, the wafers move through a high temperature zone, about 950°C , for six minutes. When the wafers have cooled to room temperature the oxide is removed with a buffered HF solution.

The side of the wafer contacting the belt during diffusion is faced upward and sprayed with aluminum powder suspended in an organic fluid. The wafers are then alloyed at about 650°C for five minutes.

B. Junction Formation Verification Experiments.

The first step in analyzing liquid dopants was to spin on dopants and look at sheet resistance after diffusion.

In the first quarterly report we reported experiments with a great variety of spin-on doping sources. As a result of the experiments the field of inquiry was narrowed to three dopants, namely, Emulsitone's N-250, Allied Chemical's PX-10, and Solarex's SX-101. Experiments were then completed in which the quantity of dopant and wafer spinning speed were varied. For each quantity of dopant and wafer spinning speed several batches were created and diffused at different temperatures. For the most part, the diffusion time was held constant at nine minutes. In order to investigate accurately the five parameter system of dopant type, dopant quantity, spin speed, diffusion temperatures, and wafer surface texture, over 75 separate experiments were required. Most experiments were not done in the belt furnace since it was not installed until mid-February. It has been found since, that a good correlation of sheet resistance exists between belt furnace and non-belt furnace diffusions.

Tables 2 to 7 show the resulting sheet resistances from the above mentioned experiments. The asterisk indicates sheet resistances that fall within the range, 50-150 $\Omega/\square$, that produces good cells.

Table 2

-8-

Dopant: Solarex SX-101
 Surface: Pillowed, 1-0-0
 Silicon: 2 Ω -cm

<u>Temperature</u>	<u>$\Omega / \square$</u>	<u>Amount</u>	<u>RPM of spinner</u>
1050°C	78.	1. cc	3,000
1050°C	20.	.6cc	3,000
1050°C	26.	.4cc	10,000
1000°C	18.	1. cc	3,000
950°C	57.*	1. cc	3,000
950°C	63.*	.6cc	3,000
950°C	122.*	.4cc	10,000
920°C	244.	.6cc	3,000
920°C	249.	.4cc	10,000
900°C	152.	1. cc	3,000
850°C	392.	1. cc	3,000

Table 3

Dopant: Solarex SX-101
 Surface: Textured, 1-0-0
 Silicon: 2 Ω -cm

<u>Temperature</u>	<u>$\Omega / \square$</u>	<u>Amount</u>	<u>RPM of spinner</u>
1050°C	6.	1. cc	3,000
1050°C	8.	.7cc	3,000
1050°C	12.	.7cc	10,000
1000°C	13.	1. cc	3,000
950°C	36.	1. cc	3,000
950°C	36.	.7cc	3,000
950°C	38.	.7cc	10,000
920°C	88.*	.7cc	3,000
920°C	83.*	.7cc	10,000
900°C	43.	1. cc	3,000
850°C	178.	1. cc	3,000

*Preferred sheet resistance.

Table 4

-9-

Dopant: Emulsitone N-250
 Surface: Pillowed, 1-0-0
 Silicon: 2 μ -cm

<u>Temperature</u>	<u>$\Omega/\square$</u>	<u>Amount</u>	<u>RPM of spinner</u>
1050°C	19.	1. cc	3,000
1050°C	15.	.3cc	3,000
1050°C	25.	.3cc	10,000
1000°C	30.	1. cc	3,000
950°C	91*	1. cc	3,000
950°C	74*	.3cc	3,000
950°C	102*	.3cc	10,000
920°C	1120.	1. cc	3,000
920°C	286.	.3cc	3,000
920°C	325.	.3cc	10,000
900°C	234.	1. cc	3,000
850°C	766	1. cc	3,000

Table 5

Dopant: Emulsitone N-250
 Surface: Textured, 1-0-0
 Silicon: 2 μ -cm

<u>Temperature</u>	<u>$\Omega/\square$</u>	<u>Amount</u>	<u>RPM of spinner</u>
1050°C	15.	1. cc	3,000
1050°C	17.	.3cc	3,000
1050°C	21.	.3cc	10,000
1000°C	20.	1. cc	3,000
950°C	38.	1. cc	3,000
950°C	59.*	.3cc	3,000
950°C	139.*	.3cc	10,000
920°C	225.	.3cc	3,000
920°C	296.	.3cc	10,000
850°C	579.	1. cc	3,000

Table 6

-10-

Dopant: Allied Chemical PX-10
Surface: Textured, 1-0-0
Silicon: 2 Ω -cm

<u>Temperature</u>	<u>$\Omega/\square$</u>	<u>Amount</u>	<u>RPM of spinner</u>
1050°C	8.	1. cc	3,000
1050°C	9.	.6cc	3,000
1050°C	8.	.3cc	10,000
1000°C	16.	1. cc	3,000
950°C	51.*	1. cc	3,000
950°C	87.*	.6cc	3,000
950°C	119.*	.3cc	10,000
920°C	206.	.6cc	3,000
920°C	613.	.3cc	10,000
850°C	541.	1. cc	3,000

Table 7

Dopant: Allied Chemical PX-10
Surface: Pillowed, 1-0-0
Silicon: 2 Ω -cm

<u>Temperature</u>	<u>$\Omega/\square$</u>	<u>Amount</u>	<u>RPM of spinner</u>
1050°C	9.	1. cc	3,000
1050°C	9.	.6cc	3,000
1050°C	10.	.3cc	10,000
1000°C	17.	1. cc	3,000
950°C	82.*	1. cc	3,000
950°C	85.*	.6cc	3,000
950°C	101.*	.3cc	10,000
920°C	1120.	1. cc	3,000
920°C	283.	.6cc	3,000
920°C	918.	.3cc	10,000
900°C	223.	1. cc	3,000
850°C	485.	1. cc	3,000

The cells in Tables 2-7 were all diffused for nine minutes in order that the data be comparable. Shorter diffusion times were also tried. A sample quantity of diffused wafers from experiments with several diffusion times, diffusion temperatures and spin-on dopants were made into cells using conventional processing. A graph of sheet resistance versus cell maximum power, Figure 1, was made so that sheet resistance could be used as an immediate measure of success in diffusion experiments.

A good correlation between resulting peak power and initial sheet resistance exists independent of the doping source. The optimal power output occurs for both pillowed and textured surfaces at about $100 \Omega/\square \pm 50 \Omega/\square$. At higher sheet resistances the junction is too shallow and at lower sheet resistances it is believed that deep diffusion causes crystal damages.

We have also experimented with minimizing the quantity of dopant for two spin speeds, 3,000 RPM and 10,000 RPM. Tables 8 - 10 indicate the minimum quantity of dopant that will physically cover the wafer. This was done for three dopants. After spinning the wafers were split into several groups and diffused at various temperatures. The ones with sheet resistance between $50 \Omega/\square$ and $150 \Omega/\square$ were made into cells using conventional processing. The sheet resistances are shown in Tables 2 - 7. The electrical characteristics of the resulting cells are also shown in Tables 8 - 10.

All three dopants yield basically the same excellent results so that a choice can be made largely based upon economic consideration. As we point out in the economical analysis

Fig.1 Wafer Sheet Resistance vs. Cell Maximum Power

Table 8

Dopant: N-250
 Diffusion: 950°C, 9 minutes
 Surface: Pillowed, 1-0-0

<u>Amount</u>	<u>RPM</u>	<u>V_{oc}</u>	<u>I_{sc}</u> <u>(2 x 2cm)</u>	<u>Power_{max}</u> <u>(AM1)</u>
.3cc	10K	586 $\pm$ 2	99 $\pm$ 1	44 $\pm$ 1
.3cc	3K	592 $\pm$ 2	99 $\pm$ 1	45 $\pm$ 1

Dopant: N-250
 Diffusion: 950°C, 9 minutes
 Surface: Textured, 1-0-0

<u>Amount</u>	<u>RPM</u>	<u>V_{oc}</u>	<u>I_{sc}</u> <u>(2 x 2cm)</u>	<u>Power_{max}</u> <u>(AM1)</u>
.3cc	10K	575 $\pm$ 5	128 $\pm$ 3	56 $\pm$ 1
.3cc	3K	575 $\pm$ 5	125 $\pm$ 1	56 $\pm$ 2

Table 9

Dopant: PX -10
 Diffusion: 950°C, 9 minutes
 Surface: Pillowed, 1-0-0

<u>Amount</u>	<u>RPM</u>	<u>V_{oc}</u>	<u>I_{sc}</u> <u>(2 x 2cm)</u>	<u>Power_{max}</u> <u>(AM1)</u>
.3cc	10K	585 ± 5	100 ± .5	45 ± 2
.6cc	3K	587 ± 5	101 ± .5	45 ± 1

Dopant: PX -10
 Diffusion: 950°C, 9 minutes
 Surface: Textured, 1-0-0

<u>Amount</u>	<u>RPM</u>	<u>V_{oc}</u>	<u>I_{sc}</u> <u>(2 x 2cm)</u>	<u>Power_{max}</u> <u>(AM1)</u>
.3cc	10K	580 ± .5	128 ± 1	56 ± 2
.6cc	3K	582 ± .5	126 ± 1	57 ± .5

Table 10

Dopant: SX-101
 Diffusion: 950°C, 9 minutes
 Surface: Pillowed, 1-0-0

<u>Amount</u>	<u>RPM</u>	<u>V_{oc}</u>	<u>I_{sc}</u> <u>(2 x 2cm)</u>	<u>Power_{max}</u> <u>(AM1)</u>
.4cc	10K	580	98 ± 1	42 ± 1
.6cc	3K	585	99	44 ± .5

Dopant: SX-101
 Diffusion: 950°C, 9 minutes
 Surface: Textured, 1-0-0

<u>Amount</u>	<u>RPM</u>	<u>V_{oc}</u>	<u>I_{sc}</u> <u>(2 x 2cm)</u>	<u>Power_{max}</u> <u>(AM1)</u>
.7cc	10K	580	125 ± 2	54 ± 1
.7cc	3K	590 ± 2	127 ± 2	56 ± 2

SX-101 is by far the least expensive dopant and therefore remains the prime candidate for employment in an economical automated cell production line.

Soon after the belt furnace arrived we tried an experimental foray to the edge of technology, namely, a 1.6 minute diffusion using the greatest belt speed. The high sheet resistance obtained, greater than 200 ohms per square, indicates a junction too shallow to be useful but since the sheet resistance was only about a factor of two too high, one can assume that a time intermediate between 9 minutes and 1.6 minutes should give a useful cell. The fast diffusion was done at 1050°C. Certainly longer times would be needed to get the same sheet resistance at lower diffusion temperatures. The trade-off between time and temperature has been investigated.

The best results using SX-101 has been from a six minute diffusion at 950°C. It is recommended that an engineering effort in the next phase of automation experiment with a graded zone that has a peak region somewhat above 950°C. It is likely that the diffusion time can be reduced to less than six minutes with proper control of $\Delta\text{temp.}/\Delta\text{time}$.

Once the diffusion parameters were determined we began experimenting with techniques of dopant application that were suitable for automation. The two meanings of 'spinning' must be clarified. The wafer spinning discussed so far involves centering a wafer on a vacuum chuck and spinning around the axis perpendicular to the plane of the wafer. Spinning at speeds between 3,000 to 10,000 RPM spreads the dopant

into a thin uniform layer. This is the standard technique for applying liquid dopants. When the wafers are dipped or sprayed the wafer can be spun while in the holder in a manner similar to the spin cycle of a washing machine in which the axis of rotation does not go through the wafers. It is this latter form of spinning that seems most suited to an automated process.

We have found that contamination between front dopant and back alloy can be eliminated by using two belt furnace steps in which the wafer is diffused, cleaned, sprayed and then alloyed. After diffusion the oxide layer on the silicon is removed with hydrofluoric acid. One side of the wafer is then sprayed with aluminum powder suspended in an organic liquid. Acetone and ethanol have proven to be good carriers. Ethanol is preferable from the standpoint of safety. We have experimented with chromium powder as well. Though chromium adheres firmly to silicon when deposited in a vacuum the sprayed chromium does not adhere even after an alloy temperature as high as 1000°C.

Four inch diameter wafers with textured surfaces have been diffused and alloyed using the automation technology. Subsequent steps including metallization were performed with conventional technology. We expect to soon be able to metallize using automation technology as is reported in another section. The best of the cells were 9.7% efficient, significantly less than the 2x2 cm cells reported in Tables 8-10, the best of which were 14% efficient. We are now looking to see which steps do not occur evenly over the wafer surface.

Junction Formation

C. Economic Analysis

Junction formation can be divided into five sub-steps:

1. Cover wafer with dopant.
2. Diffuse in belt furnace.
3. Remove diffusion glass.
4. Spray back contact.
5. Alloy.

The materials, utilities, equipment, and labor will be identified for each sub-step. The analysis is based on a rate of 120 wafers per minute.

1. Without specifying the detailed nature of the wafer transport mechanism we can predict a process in which the wafers are dipped in dopant then spun for a moment to centrifugally remove the excess liquid. If held in baskets the entire basket could be spun for a few seconds. A single mechanical drive could process the entire flow of 120 wafers/minute so the equipment cost would be negligible. We have described several dopants that work well. In particular, SX-101 is of very low cost, about 2¢ per wafer. No utilities are required other than a small amount of electricity to run the transport mechanism. Aside from maintenance no personnel are required for this sub-step.

2. The diffusion requires a belt furnace with two zones. In the first zone the spray on dopant is solidified at low temperature, about 150°C , and in the second zone the junction is formed at about 950°C . The solidification requires about four minutes and the diffusion requires six minutes. The belt furnace cost estimate will be based on our present belt furnace. The cost is expected to be much less if a special purpose machine is built in which the wafers are spaced close together. Currently, the wafers are placed horizontally in a single row. Hence the 48" hot zone holds 12 wafers. A throughput of 120 wafers/minute and a ten minute resident time implies the need for 100 belt furnaces. At \$6,600 each the total cost is \$660,000. Since 50 million wafers would be processed each year a five year operating life implies a cost of .26¢/wafer. This 'off the shelf' approach indicates a maximum cost that could be reduced during pilot line engineering. No materials are needed. The heating of the belt furnace incurs an electric utility cost. Each furnace uses about 7.5kw continuously. At 7¢ per kw-hr the cost is .73¢ per wafer. Cooling water is also required, at negligible cost.
3. After diffusion the oxide layer is removed in an acid such as HF. It was shown in the first quarterly report that the cost is .22¢/wafer.
4. Metal powder mixed in ethanol is sprayed on one side of the wafer to prepare for back junction alloy. The equipment, a spray gun and wafer transport mechanism, would be of negligible cost. The materials

consist of a metal powder, aluminum or chromium @ 0.2gm/wafer and ethanol @ 4gm/wafer. In determining the cost aluminum powder will be used. At \$17.00/kgAl the cost is .34¢ per wafer. The ethanol costs about .2¢/wafer. An operator will be required to monitor this process.

2. The alloy step generates an ohmic contact on the back of the cell. The time required is about five minutes. Due to the lower-temperature, about 650°C, less electricity is used, about 5kw/furnace, than is the case for diffusion. The economic analysis is similar to the diffusion process. The results are given in the table II below:

BASED ON 120 WAFERS/MINUTE.

Substep	Materials	
1	SX-101	2.¢/wafer
3	Acid	.18¢/wafer
4	Metal (Aluminum)	.34¢/wafer
4	Ethanol	.2¢/wafer

Substep	Equipment	
All	Wafer transport	.03¢/wafer
2	Belt furnace	.26¢/wafer
3	Etch bath	.02¢/wafer
4	Spray gun	.02¢/wafer
5	Belt furnace	.13¢/wafer

Table II: Economic Analysis - Junction Formation

Substep	Utilities	
All	Electricity for wafer transport	.03¢/wafer
2	Electricity for belt furnace	.73¢/wafer
2	Cooling water (4 gal/minute)	.04¢/wafer
3	DI Water rinse (2 gal/minute)	.01¢/wafer
5	Electricity for belt furnace	.27¢/wafer
5	Cooling water	.02¢/wafer

Substep	Overhead and Labor	
All	Maintenance	.05¢/wafer
2	Operator	.04¢/wafer
3	1/2 Operator	.02¢/wafer
4	Operator	.04¢/wafer

Table II cont.

TOTAL: 4.14¢/wafer

III. Metallization

A. Review and Assessment

The metallization step of cell manufacture is composed of three substeps. The first substep is to apply a masking ink using silkscreening. The regions that are left free of ink form an interconnected grid of lines of bare silicon. In the second substep the bare silicon is plated with nickel using an electroless nickel plating solution. After plating the masking ink is removed. In the third substep the wafer is dipped in solder that adheres to the nickel. The solder enhances the conductivity of the lines by substantially increasing the thickness. Furthermore, the solder allows the cells to be interconnected in the panels.

In this section the technology required for metallization is reviewed and assessed, then the experimental verification results are discussed.

1. Negative silkscreening.

Metallization inks are expensive and require a carefully controlled high temperature sintering step. Solarex is investigating an alternative technique, called negative silkscreening, in which the areas that should not be metallized are covered with a low cost masking ink. The uncovered lines are nickel plated using an electroless nickel plating solution.

Before describing our verification work the 'art' of silkscreening will be surveyed. Silkscreening is basically an extrusion process whereby an ink is forced through a fine mesh screen using a rubber squeegee, as shown on the next page.

Figure 2 Silk Screening Process

The screen is positioned slightly above the substrate so that it only contacts the substrate when the squeegee passes over. Silk is no longer used as a screen material. Currently either synthetic fiber or stainless steel mesh is used.

The pattern is generated by covering certain areas of the screen in one of two distinct ways. One possibility is to photographically generate the pattern on a film that is subsequently adhered to the screen. The second possibility is to fill the mesh with a photosensitive liquid that is solidified, exposed to light then developed so that certain areas are washed clear.

Line definition is controlled by the screen mesh size, the viscosity of the ink, and the sharpness of the screen pattern. Printing is fastest when done with a thixotropic ink, that is, an ink that liquefies when under stress but becomes firm when the screen separates from the substrate. The stroke of the squeegee is very important and is best done by machine in order to assure constancy of blade angle, pressure and speed.

Silkscreening has a high throughput that is well suited to automation. A squeegee can move at 12"/sec and can cover an area 12" wide. That is, nine cells can be screened each second. Allowing three seconds for the operation, including

loading and unloading, the throughput can be 180 wafers per minute.

2. Electroless nickel plating.

Though the overall equation for virtually all electroless nickel plating solutions is,

there is a wide variety of chemical contents. For most solutions the two major ingredients are nickel chloride and sodium hypophosphite. The additional ingredients can be divided into those producing an acid bath and those that require ammonium hydroxide for activation. Typical acid baths employ either hydroxyacetic acid, sodium citrate, or lactic and propionic acids. The ammoniacal baths have such additives as sodium citrate or sodium pyrophosphate. Additional chemicals are added for stabilization, to enhance nickel adhesion, to control grain structure, and to increase plating speeds.

The ammoniacal baths were chosen for experimentation because plating speeds are generally higher than acid baths and because the precipitation of nickel phosphite is much less likely than it is in acid baths. Further advantages are that for the basic ammoniacal baths pH is automatically maintained as long as an excess of ammonia is present and that the depth of color can be used as a measure of nickel concentration in the solution.

3. Solder dipping.

Solder dipping is widely used in the manufacture of circuit boards. There are two major problems that must always be circumvented in solder dipping. The first is that an oxide layer forms on the top of the molten solder. If a wafer is simply dipped into the solder the first material to contact the nickel is an oxide that prevents the solder from covering evenly. The second problem is the formation of tails as the wafer separates from the solder. Machines are available that prevent both problems, for example, by moving the wafer through a standing wave of liquid solder.

There is a third problem unique to electroless nickel plating coatings. The high phosphorus content of the nickel can prevent adhesion of the solder.

B. Verification Experiments

1. Experimental results, silkscreening.

Initial experiments were done with a synthetic fiber screen of 100 mesh. The screen pattern was formed from a water base resist that withstands organic solvents. The finest line in the pattern was three mils wide. Standard silkscreening inks were found to wash off in the hot nickel plating solution. Epoxy, acrylic and urethane paints were also tried. Aside from washing off in the hot plating solution two other problems have been identified. One problem is that solvents in the paint migrate over the silicon surface and prevent plating. The other problem is that paints based on light solvents harden on the screen prematurely, that is, while the resist pattern is still usable. Over ninety percent of the inks and paints tried have proven unsuitable. A notable exception is urethane varnish made thixotropic with titanium dioxide powder which works well. More screens are on order with mesh sizes of 230, 325 and 400. The screen material will be stainless steel. Two emulsions will be tried, a 'microfilm' emulsion made for fine lines and a standard emulsion that is more durable.

2. Experimental results, nickel plating.

Various plating solutions were tried on diffused silicon that had been cleaned in hydrofluoric acid. Most plating solutions are catalyzed only by specific metals such as iron. A typical example is SEL-REX Lectorless Ni plating solution #11250. The full range of recommended temperatures and pH levels were tried, from 85°C to 95°C and pH from 5.5 to 6.0. Plating only occurred when the silicon surface was made cathodic with an electric current. This meant that the

thickness of plating depended on the pattern of current densities on the silicon surface, an unacceptable restraint in designing an automated facility.

After further search a very effective plating solution was found. It is produced by J. E. Halma Co. and is designated #139-500011-71. Plating onto diffused, cleaned wafers occurs as soon as the wafers are immersed. All subsequent testing has used this plating solution. The temperature and pH are self-regulating in this solution. Once the proper pH level of 8.0 - 8.2 is reached through the addition of ammonium hydroxide adding more ammonium hydroxide does not increase the pH. Also, once the proper temperature has been reached, 93°C - 95°C, additional heat input causes evolution of ammonia vapor that prevents the plating solution temperature from rising. The ammonia is condensed on the cover of the plating bath and returned to the plating solution.

3. Verification Experiments, Solder dipping.

After nickel plating the wafers are sintered to assure adhesion between the nickel and the silicon. After sintering we have dipped the wafers into solder with sporadic success. The solder often does not stick to the nickel. The problem can be attributed to two causes. The first is the oxide layer formed on the nickel during sintering and the second is the phosphorus content of the nickel. We will attempt to solve both problems by using hydrochloric acid to clean the nickel and by using an acid flux such as zinc chloride during the dipping. When a room temperature wafer is dipped into the solder bath it occasionally cracks due to the thermal shock. Preheating the wafer will solve this problem. In an automated operation it may be possible to sinter, flux clean and preheat in a single step.

C. Preliminary Economic Analysis of Metallization

1. Silkscreening.

The cost of an automatic silkscreening machine is from \$10,000. to \$20,000. There will be some additional cost for the wafer handling equipment that positions a number of wafers below the screen. The entire cost is expected to be less than \$50,000. which for a three year operating life implies a cost of .03¢/ per wafer. The greatest cost will be supplies, the silkscreen and the ink. A stainless steel screen costs about \$25. The screen can be used for several mask cycles, say five. The mask must be remade after a certain number of printings to maintain sharp lines. The number of printings varies considerably depending on mask material and ink composition. We shall assume 1,000 printings can be made with 12 wafers each printing. To develop a mask onto a screen costs about \$15. so the cost is .125¢/wafer for each mask re-make and .042¢/wafer for the screen.

Most of the wafer is covered with masking ink so that a low cost ink must be used. The urethane varnish that we are presently using costs about \$8./liter in small quantities. This implies a cost of .8¢/wafer.

2. Nickel plating.

The cost of equipment, primarily a plating tank and wafer holders, is very similar to surface preparation. It was demonstrated in the first quarterly report that the equipment cost

would be about .04¢/wafer. The nickel plating solution costs \$1.20/liter and one liter will plate 500 4" wafers. Hence the plating solution cost is .24¢/wafer. The acetone used to remove the masking ink costs about .1¢/wafer. This cost can be reduced if a cleaning fluid such as a chloroethane is used and recycled.

3. Solder dipping.

The solder dipping equipment is likely to cost less than \$50,000 for a cost of about .04¢/wafer. The solder costs 18¢/cc for 60-40 solder. The thickness on the wafer is about 10 μ m on the front and somewhat greater on the back, about 20 μ m on the average. Hence, the solder used per 4" wafer costs 3¢/wafer.

4. Summary.

The costs can be summarized as follows: Table 12

<u>Substep</u>	<u>Cost/Wafer</u>
<u>Equipment</u>	
Screen Printing Machine	.03¢/
Plating tank and wafer holders	.04¢
Solder dip station	.04¢
<u>Materials</u>	
Screen and screen resist	.167¢
Ink	.8¢
Plating solution	.24¢
Cleaning fluid	.1¢
Solder	3.¢
<u>Overhead and Labor</u>	
1 operator	.04¢
1 operator	.04¢
1 operator	.04¢
TOTAL	4.537¢/wafer

IV. Edge Removal

A. Review and Assessment

The topology of a solar cell after metallization is shown below.

Figure 3

(Not to scale)

The region circled in the drawing causes an electrical short between the front and back. The short is eliminated by removing silicon and metal as far as the dotted line, less than a thousandth of an inch.

The edge can be removed chemically, mechanically, or by laser scribing. Chemical removal requires that the face of the cell be protected. One way this is done is by compressing a stack of cells between layers of plastic. Chemical edge removal cannot easily be automated.

The mechanical removal of the edge can be done (with a grinding tool) at a rate of about one wafer per second. Alternatively, a laser scribe can be used. The laser does not cut through the silicon, it simply starts a cleavage as is done in glass cutting. A laser can convert circular cells into hexagons that can be closely packed into a panel.

The rate of edge removal by laser scribing is comparable to grinding. In both methods the silicon crystal is damaged somewhat yet neither method degrades cell performance significantly.

B. Economic Analysis

a) Mechanical grinding

The only supply needed for edge grinding is a grinding point such as tungsten carbide. Typically a grinding point must be replaced every 2,000 wafers because of wear. Points cost from two to four dollars, depending on size and composition.

Using a cost of \$3/point the materials cost is .5¢/wafer.

Grit must be removed from the silicon after grinding. A high speed jet of water can be used to transfer momentum with a very small volume of water.

The cost of an automatic grinding machine can be based on currently available edge beveling machines used on lenses. A typical machine costs \$10,000. Several machines will be needed for a throughput of 120 wafers/min. since the total grinding time, including cell placement and removal, is over one second.

Using a total machine cost of \$30,000. with a three year operating life incurs a cost of 0.2¢ per wafer.

While the machine can step through the grinding operation automatically an operator would be required to maintain the machine and judge when grinding points need replacement. The cost based on 120 wafers/minute is summarized below.

Materials		
Grinding point		.15¢/wafer
Cleaning water		.01¢/wafer
Equipment		
Edge grinder		.02¢/wafer
Overhead and labor		
Operator		<u>.04¢/wafer</u>
	TOTAL	.22¢/wafer

Table 13

b) Laser scribing.

The only supplies needed are replacement parts for the Yag laser. The major item, the krypton flash tube, has a 200 hour life and costs \$200. in quantity purchase. This implies a materials cost of .014¢ per machine. Utilities, namely, water and electricity are required.

A laser scribing machine with enough power to cut the perimeter of a single four inch wafer each second costs about \$75,000. It is assumed that cleaving the scribed lines will incur no additional cost since the operation can be done quickly while the wafer is being transported to the test station. As with grinding additional time is required to position the wafer on the laser table and to remove the wafer.

Having three machines in operation, each with an operational life of three years implies a cost of .15¢ per wafer.

An operator will be needed to monitor the process.

The cost based on 120 wafers per minute is summarized below.

Materials

Krypton flash tube

and other consumables

.02¢/wafer

Utilities

Cooling water

.01¢/wafer

Electricity (8kw per machine)

.02¢/wafer

Equipment

Laser scribe

.15¢/wafer

Overhead and labor

Operator

.04¢/wafer

TOTAL

.24¢/wafer

Table 14

A. Review and Assessment

Completed cells must be tested electrically and mechanically. Mechanical testing assures that the metal contacts adhere firmly to the cell. Electrical testing not only grades cells but can provide feedback on the performance of the production line. For example, the diode curve of the cell is a sum of exponential factors that indicate the quality of the bulk silicon, the defect density at the junction and the recombination velocity of charge carriers at the surface and edge. These measures, in turn, can be related to variations in specific process steps.

By utilizing a minicomputer a wide gamut of testing operations can be performed automatically. The silkscreen contact pattern can be used by a laser scanner or CCD optical matrix to align the cell for testing. After contact adhesion testing, with a brush for example, optical pattern processing can determine whether contacts have been removed or continue to adhere. Furthermore, the computer can drive a variable power supply to obtain the cell I-V curve. Continual calibration procedures can be made inherent in the computer program.

The speed of operation is not limited by the calculations performed by the computer but by the speed of mechanical manipulation. For example, the IV curve can be recorded electronically in a fraction of a second but the brushing of the cell surface to test contact adhesion may require several seconds. For the slower operation, contact brushing, the cells must split into parallel paths then recombine into a single line for the specialized operation of optical inspection by the computer.

The automation of egg handling and mechanical watch assembly are examples that show there are no physical limitations to testing at a rate of 120 wafers per minute.

B. Economic Analysis

A typical price for a microcircuit wafer testing machine is \$100,000. The cost can be divided roughly as \$25,000. for the electronics and \$75,000. for the mechanical aspect.

Microcircuits are contacted through small, closely spaced metal pads. Precise positioning and delicate application of contacting force is very important. Furthermore, the probes must step quickly through many circuits on the same wafer. This is in great contrast to solar cell testing in which electrical contact need be made only once onto a large contact area. We can take \$100,000. as an upper bound for a cell testing machine that processes 120 wafers/minute. A three year machine life implies a wafer cost of .07¢/wafer. Including .04¢ for overhead and labor the total cost for testing is 0.11¢/wafer.

VI. Conclusions

Our work to date on this contract has strengthened our beliefs that the process steps considered so far do lend themselves to automation and can be carried out economically so that the Project Goals can be reached. Certain problems within the junction formation and metalization step are considered mechanical in nature and should be overcome with properly designed machinery.