MECL DELAY AND WIRING TESTS FOR MECL 10000 *

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I. DELAY CIRCUIT A

This circuit is designed such that the delay between the input and the output signals can be determined by the value of the capacitor.

(All three gates are line receivers.)

Q_1 and Q_2 are the two output transistors of gate (1). When I is low, both transistors are in their linear region. V_{b1} is high, V_{b2} is low and the capacitor is charged to: $V_{OH} - V_{OL}$. When I goes high, the base of Q_1 shifts from 0 to -1 volt, and the base of Q_2 shifts from -1 to 0V.

* Work supported by the Department of Energy, contract DE-AC03-76SF00515.
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The potential V_{b1} being V_{OH} (-0.9 V), Q_1 is turned off. Q_2 is still in its linear region but drives a large current such that the potential V_{b2} rises from V_{OL} to V_{OH} almost instantaneously because of R_2 . The capacitor will then discharge through R_1 until V_{b1} reaches V_{OL} . At this point, Q_1 is in its linear region again and the discharge stops.

MASTER

$$V_{b1} = -2 + \left[2V_{OH} - V_{OL} + 2 \right] e^{-t/R_1 C}$$

The output of gate (2) will change when $V_{b1} = V_{b2}$:

$$V_{b1} = V_{b2} = V_{OH} = -2 + \left[2V_{OH} - V_{OL} + 2 \right] e^{-\Delta t/R_1 C}$$

This gives us a delay of Δt for the positive edge of I .

The rise times of V_{c1} and V_{c2} increase as the value of the capacitor increases (13 ns for 400 pF). Therefore gate (3) is added to the circuit such that the rise time of the output is constant and equal to 3 ns.

When I goes low, V_{b1} and V_{b2} are interchanged such that we get the same delay for both edges.

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II. DELAY CIRCUIT B.

$$R_1 = R_2 = 100 \, \Omega$$

CLOCK FREQUENCY: 300 kHz

Theoretical Slope: $-0.9 + 2 = [2(-0.9) + 1.78 + 2] e^{-\Delta C/100C}$

$$\Delta t = 58.78^\circ\text{C}$$

The line receivers are MC10114. The MC10101 gate provides ECL input levels.

C pF	0	12	36	75	100	175	200	236	300	375	400
Δt_1 nsec	7	8.5	11	13.5	15	19.5	21.5	23.5	28.5	33	35
Δt_2 nsec	7	8.5	11	13.5	15	19.5	21.5	23.5	28	32	34

With $C = 0$, the circuit delay is the delay of the chips, t_{nd} .

See Fig. 1.

This circuit is similar to the preceding circuit, but C_1 controls the delay of the positive edge while C_2 controls the delay of the negative edge.

Q_1 is the output transistor of gate (1). When I is low V_{b1} is equal to V_{OH} and C_1 is charged to $(V_{OH} + 2)$ volts. The base of Q_1 is at 0 volts. When I goes high, the base of Q_1 shifts to -1V and as a result Q_1 is off. The capacitor will then discharge through R_1 until V_{b1} reaches V_{OL} . At this point Q_1 is in its linear region again.

V_{B2} will change its level when V_{B1} reaches V_{BB} (-1.3 V). As a result, we have a delay of Δt_1 for the positive edge. When V_{B1} reaches V_{BB} , V_{B2} goes up almost simultaneously because the output transistor of Gate (2) is in its linear region and drives a large current. When I goes down again, V_{B1} and V_{B2} are interchanged and C_2 determines the delay Δt_2 of the negative edge.

$$V_{BB} = -2 + (V_{OH} + 2) e^{-\Delta t_1 / R_1 C_1}$$

Experimental Port

$$V_{OH} = -0.9 \text{ V}$$

$$R_1 = R_2 = 100 \Omega$$

$$V_{OL} = -1.78 \text{ V}$$

$$\text{CLOCK FREQUENCY: } 300 \text{ kHz}$$

$$\text{Theoretical Slope: } -1.3 + 2 = (-0.9 + 2) e^{-\Delta t / 100C}$$

$$\Delta t = 45.2C$$

The gate used is the MC10101.

C pF	0	12	36	75	100	160	200	270	300	331	390
Δt_1 nsec	7	8	10	12	13	16.5	18	21.5	22.5	24	27
Δt_2 nsec	7	8	10	13	14	18	20.5	25	26	28	31

See Fig. 2. To avoid increasing the output rise time as delay increases, another gate can be added to the circuit to standardize the output rise time.

III. WIRE WRAP TESTS

Tests were performed to evaluate the use of wire-wrap with MECL 10000. All tests were done using 30 Awg Kynar wire-wrap on an Augat ECL board, Part #8136-ECL1-60-2. This is a multilayer board with an internal plane (V_{TT}) for the termination resistors. 100 Ω DIP resistors were used for all termination resistors (Beckman 899-1-R100).

A schematic of the test setup for all tests is shown below.

The sections of the MC10101 were used to standardize the pulses. The actual transmission line under test was connected between 6 (sending end) and pin 10 (receiving end). Photographs of the positive signal edges are shown in Fig. 3, under varying conditions of termination and line lengths as described. Numbers on the photographs refer to indicated pin numbers on the schematic. Responses with negative edges were quite similar to the positive edges, and are consequently not shown.

Twisted pair experiments were done with one wire of the pair grounded, at each end, terminated at the receiving end.

IV. CONCLUSION

Both delay circuits evaluated—A and B—performed satisfactorily, but circuit A demonstrated better tracking between delay of positive and negative edges.

Wiring tests demonstrated that the MECL 10000 can be used quite successfully with limited length wire-wrap, due primarily to the measured 3 nsec edge speeds.

As expected, the shapes are considerably better with receiving end termination rather than sending end termination, even at a length of 5". One can estimate from the photographs the signal delay resulting from the length of the wire.

Concerning twisted pair, there is very little evidence from the experiments that this wiring technique is a significant improvement over conventional wiring, although some improvement in edge speed is noticeable.

For comments or questions on this work, please call Dale Horelick at ext. 2337, at SLAC.

LIST OF FIGURES

1. Delay Curve of Circuit A
2. Delay Curve of Circuit B.
3. 5" of wire, terminated at the sending end; 5" of wire, terminated at the receiving end; 5" of twisted pair, terminated at the receiving end; 10" of wire, terminated at the sending end; 10" of wire, terminated at the receiving end; 10" of twisted pair, terminated at the receiving end. 15" of wire, terminated at the sending end; 15" of wire terminated at the receiving end; 15" of twisted pair, terminated at the receiving end.

Fig. 1

Fig. 2

Fig. 3