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October, 1978

SC5150-20QR

DEVELOPMENT OF HIGH EFFICIENCY GaAs
POLYCRYSTAL SOLAR CELLS

Quarterly Technical and Topical Report No. 2

For period 04/24/78 through 07/23/78

Contract No. EG-77-C-03-1712

General Order No. 5150

Prepared for

Department of Energy
Division of Solar Energy
Energy R&D Administration
Washington, D.C. 20545

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ABSTRACT

This is the second quarterly technical report of a research program, "Development of High Efficiency GaAs Polycrystal Solar Cells". This program is being carried out jointly by the Rockwell International Science Center, Brown University, Howard University, North Carolina A&T State University, and Cornell University. The objectives of this program is to develop a thin film polycrystal GaAs solar cell technology with the potential of yielding cells with 12-15% efficiency and to develop thin film growth techniques which are compatible with the low cost production goal of \$100-300/KW peak.

During this quarter, techniques conceived and initiated during the first quarter have seen initial application for measurements and fabrication of solar cells. The scanning Auger potential profiling and cathode-conductivity measurements and scanning laser system are beginning to yield useful results. Transient capacitance measurement of minority carrier lifetimes, and Schottky barrier comparisons of LPE and MBE polycrystalline GaAs are described. Theoretical investigations of GaAs dislocations and polycrystalline solar cell modeling has begun. Oxidation of GaAs for MIS cell fabrication is described, and promising values reported for initial MIS single crystal solar cell performance.

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1.0 INTRODUCTION

Progress in the development of high efficiency single crystal GaAs solar cells has been phenomenal over the past three years. Over this period, GaAs cell efficiencies have gone from 16% up to nearly 25%, the highest value for any solar cell, and approaching the theoretical limit for a single cell structure. Numerous systems studies of various solar cell options suggest that the lowest, long term solar electric generating costs will be achieved by very low cost, polycrystal or amorphous thin film devices. The major difference between single and polycrystal materials is the occurrence of grain boundaries in the polycrystal material. Grain boundaries reduce the lifetime and diffusion lengths of minority carriers, thereby reducing efficiencies to ~6% compared to 25% for single crystal cells. Virtually nothing is known about the interface states generated at a grain boundary, the types of impurities which segregate there and their effect on electrical transport properties. Techniques for increasing grain size and minimizing the adverse effects of grain boundaries are essential to improving the efficiency of polycrystal solar cells. The successful reduction of the adverse effects of grain boundaries could lead to polycrystal solar cells with efficiencies of more than 15%. The realization of 12-15% conversion efficiency in a thin film polycrystal structure is the goal of this program.

The initial emphasis in this program is on developing new polycrystal growth techniques and fundamental studies of the physical mechanisms by which grain boundaries limit solar cell performance and techniques to minimize these effects. The key problem areas to be addressed are as follows:

1. Development of new polycrystal growth techniques which minimize the effects of grain boundaries on the electrical properties of polycrystal GaAs and are compatible with the processing of large area, low cost devices.

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2. Development of microscopic chemical, structural and electrical measurement techniques to characterize properties of grain boundaries. Development of a model of the physical mechanisms which degrade the electrical properties of polycrystal material which can in turn be applied to the development of growth and fabrication techniques which minimize the adverse effects of grain boundaries.
3. Development of optimized fabrication techniques for barrier formation and ohmic contacts.
4. Development of an accurate polycrystal solar cell model for optimization of the various solar cell parameters.

During the second quarter of this project, several techniques for the measurement of material properties and parameters associated with GaAs grain boundaries have reached the stage of development where useful results are emerging. These include the scanning Auger potential profiling/cathodo-conductivity experiments and the scanning laser photovoltage measurements. Other techniques currently under development are reported here, such as a transient capacitance method for measurement of minority carrier lifetimes. Techniques for the fabrication of polycrystalline solar cells, such as GaAs oxidation, are reported, as well as some initial measurements of GaAs MOS single crystal cells with promising efficiencies.

This report is organized by task from the proposal and contributions are identified by the institution performing the work.

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2.0 MATERIALS DEVELOPMENT

Materials growth at the participating institutions has been aimed at two goals. The first is to provide a continuing supply of material for ongoing characterization projects. To this end, conventional LPE and MBE have been used to grow layers on n^+ and semi-insulating (SI) substrates, both single crystal and polycrystalline, for various grain boundary measurements and solar cell process development. The second goal is to grow relatively large grained GaAs on foreign substrates. Both current-controlled LPE (CCLPE) and conventional LPE have been used to attempt growth of GaAs on graphite, and GaAs has been grown on polycrystalline aluminum by MBE.

2.1 MBE and LPE Layer Growth on GaAs Substrates (Science Center)

A majority of the epilayer growths during the past quarter have been n-type GaAs grown on n^+ substrates, both single crystal and polycrystalline. These growths are aimed at providing material for metal-semiconductor (M-S) and metal-insulator-semiconductor (MIS) solar cell structures. Material doped n-type was grown because metal Schottky contacts to n-type material have a higher barrier than to p-type material.

Liquid phase epitaxy (LPE) was used to grow a number of epilayers to be used in testing MIS barrier fabrication procedures, on both single crystal and polycrystalline material. LPE material was used as a standard for test structures because of the consistently high electronic quality obtainable. LPE growths of epilayers were also made on semi-insulating (SI) twinned material for scanning Auger potential profiling and cathodoconductivity experiments (Section 3.3). Difficulty was experienced in obtaining layers with uniform thickness over the twin boundary. SEM investigations of mesa stripes crossing twin boundaries often showed much thinner epilayers at the grain boundary, and in some places, the epilayer even appeared discontinuous. This growth morphology made experiments involving transport across the twin grain boundary difficult to perform with LPE material.

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MBE growths on twinned substrates provided much more consistent results as far as epilayer morphology. Growth on both sides of the twin boundary was smooth and flat, and the epilayer thickness appeared constant across the grain boundary. This was expected from known behavior of MBE growth, which follows substrate contours very closely and does not exhibit orientation dependent growth rates.

A number of MBE layers, both doped and undoped, were grown both for M-S contact measurements (see Sec. 3) and to characterize the growth capabilities of the modified source array incorporated in the MBE chamber last quarter. Undoped layers presently are n-type, with $N_D - N_A \approx 2 \times 10^{15} \text{cm}^{-3}$ and 77°K mobilities of about $2 \times 10^4 \text{cm}^2/\text{V-sec}$. The n-type layers of higher carrier concentration are produced using Sn doping, and typically have 77°K mobilities of about $9000 - 10,000 \text{cm}^2/\text{V-sec}$ at $n \approx 2 \times 10^{16} \text{cm}^{-3}$. These mobility values are higher than were obtained before the source array modifications, but are lower than can typically be obtained by LPE, and the minority carrier diffusion lengths are also expected to be smaller than in LPE material. Efforts are continuing both to develop the MBE growth chamber to obtain higher mobilities and diffusion lengths, and to determine the suitability of existing single crystal and polycrystalline MBE layers for solar cell applications.

2.2 MBE GaAs Growth on Polycrystalline Aluminum (Science Center)

Growth of GaAs on aluminum was given priority because of recent reports of epitaxial growth of single crystal Al on GaAs by MBE. It was hoped that the tendency toward epitaxy of GaAs on Al would be strong enough to lead to preferred orientation, columnar growth, and large grain size. Our results showed some larger grains than on graphite, although the hoped-for strong preferred orientation was not present.

The initial step in growth of GaAs on Al was to procure a suitable substrate and develop procedures for cleaning the surface. The substrate was in the form of a $1 \times 1 \times 0.050$ in. polycrystalline sheet. This was formed by

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rolling from an ingot cast from 4 N Al shot. After rolling, the sheet was annealed at 482°C for 30 min. to produce grains 25 to 100 μm across. These were lightly etched in aqua regia to remove surface contamination, then electropolished to remove about 0.002 in. of material. The electropolishing process smoothed the metal, leaving a shiny, undulating surface with barely discernable grain boundaries. Examination with an optical microscope showed smooth, featureless areas of about 5-10 μm across, between submicron specks of contamination not removed by the electropolishing.

The electropolishing process apparently left behind a relatively thick oxide layer, as indicated by Auger electron spectroscopy (AES). This oxide layer proved impossible to remove in a few hours by the sputter etching gun in the MBE chamber. GaAs subsequently grown on this oxide had extremely small grain sizes (generally 0.1 μm for a 2 μm thick layer). To remove the oxide, the Al was bombarded in a commercial high energy dc ion bombardment apparatus (Millatron) with 2 keV argon ions. No studies of oxide removal as a function of ion current, energy, or bombardment time have been done. Twenty minutes of bombardment were apparently enough to remove this oxide. This was evidenced by the fact that an Al sheet, which has been sputtered in the Millatron, was cleaned of remaining oxide and other contaminants as indicated by AES within a short time by the sputter-etching gun in the MBE chamber.

Growth of GaAs on the cleaned Al substrate was initiated at an indicated substrate temperature of 580°C under conditions identical to those for single crystal GaAs growth. Figure 1 shows a SEM photo of the resultant layer about 2 μm thick. The growth direction appears to be entirely random, with some grains 4-5 μm wide, separated by areas of submicron grain size. No difference was observed in the growth on Al crystallites with different orientations.

GaAs appears to nucleate on the highly reactive Al substrate without regard to crystallite orientation. An attempt to enhance nucleation with

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Fig. 1 SEM photograph of GaAs about $2\mu\text{m}$ thick grown by MBE on polycrystalline Al. The Al substrate grains were $25\mu\text{m}$ to $100\mu\text{m}$ across, with random orientation. The area shown in the photograph was all within the boundaries of one Al grain.

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preferred orientations was made by initially reacting the Al surface with As alone (under normal growth conditions) and then growing GaAs on top of the reacted surface. Although the As beam did react with the Al surface to produce a layer of AlAs of undetermined thickness, the GaAs layer grown on top of this appeared structurally identical to GaAs grown directly on the Al.

2.3 Epitaxial Growth of GaAs on Foreign Substrates by LPE (Cornell University)

During this quarter, we primarily investigated the growth of GaAs on foreign substrates by LPE. Growth on graphite was investigated using Carbone 5890 standard grade. This type of graphite was chosen because its thermal coefficient of expansion is close to the value of GaAs. This graphite is "pseudo-vitrified" with open porosity of about 5-8%. Because of this porosity, a mirror finish polish on the samples could not be obtained. However, some type of surface smoothness was obtained using mechanical lapping techniques. Growth on these substrates was attempted using the standard LPE technique of cooling a saturated melt over the substrate. Using these graphite substrates, no wetting was observed with 10-20°C of supercooling.

In order to promote wetting of the graphite, metal coatings were vacuum deposited. First, a pure Al coating of .5-1.5 μm thick was tried. With these coatings, large crystallites were formed by cooling the furnace. Using x-ray techniques the crystallites were shown to be $\text{Ga}_x\text{Al}_{1-x}\text{As}$ with a large concentration of Al. Using tweezers as a qualitative check, it was found that the crystallites adhered fairly well to the graphite.

In attempting to make a continuous film of this polycrystalline material, we are trying different metal coatings. Also, a brief attempt at current controlled growth on these Al coated substrates was made. In two runs, no crystallites were nucleated on the graphite. This is possibly due to convection in the melt.

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In summary, we have looked at growth on foreign substrates (particularly graphite) by LPE. There was no success growing on naked graphite, however, crystallites were obtained on Al coated graphite. We are now trying different coatings and substrates in order to obtain a continuous film.

2.4 Growth of Poly-GaAs Layers by LPE and CCLPE NCA&T

After a period of two months, during which the entire crystal growing facility at NCA&T was down, we are again back to normal operation.

Our main problem presently is getting good quality polycrystalline substrates from Morgan Semiconductor, Inc. We have found that most of the polished substrates obtained from the above company not only have very irregular thickness uniformity, but often they are not correctly labeled as to type of doping and carrier concentrations.

Several attempts have been made to grow polycrystalline GaAs on poly-GaAs and graphite substrates using normal LPE and current controlled LPE (CCLPE). Most of the attempts with graphite substrates have been unsuccessful due to difficulties in obtaining good wettability.

Table I presents a summary of the results obtained on the growth of GaAs on poly-GaAs substrates by LPE. Several of these substrates were supposed to be n-type, however, tests in our laboratory have shown them to be semi-insulating.

Table II gives a summary of growth experiments on poly-GaAs substrates using CCLPE. The grown layers indicated as undoped are n-type with carrier densities in the order of 10^{16} cm^{-3} . The grown layer thickness for the majority of these samples is about 7-10 μm . The substrate dimensions were 12 x 12 x 0.5 mm.

TABLE I: EXPERIMENTAL GROWTH DATA FOR GaAs USING THE LPE TECHNIQUE

SAMPLE #	SUBSTRATE	DOPANT	DOPING DENSITY $n_d(\text{cm}^{-3})$	RAMP RATE ($^{\circ}\text{C}/\text{min}$)	GROWTH TEMP ($^{\circ}\text{C}$)	GROWTH TIME (min)	ΔT ($^{\circ}\text{C}$)	EPILAYER THICKNESS (μm)	COMMENTS
LR015-1	SI(Cr)poly	u	--	0.25	752	60	15.25		Sample sent to Rockwell
LR015-2	$\text{N}^+(\text{Te})\text{poly}$	u	--	0.25	752	60	16.50		Sample sent to Rockwell
LR015-3	SI(Cr)poly	Ge	$\approx 10^{17}$	0.25	752	60	15	9	Surface turned gray when soaked in HCl
LR015-4	$\text{N}^+(\text{Te})\text{poly}$	Ge	$\approx 10^{17}$	0.25	752	60	15.5		Surface turned dark gray when soaked in HCl
LR015-5	$\text{N}^+(\text{Te})\text{poly}$	Ge	$\approx 10^{17}$	0.25	752	60	12.25		Sample sent to Rockwell
LR015-6	SI(Cr)poly	Ge	$\approx 10^{17}$	0.25	752	60	14.75		Surface was damaged during substrate preparation with caro etch
LR015-7	$\text{N}^+(\text{Te})\text{poly}$	Ge	$\approx 10^{17}$	0.25	752	60	15		good surface but epilayer turned dark gray when soaked in HCl
LR018-1	SI poly	u	--	0.25	752	35			*
LR018-2	SI poly	u	--	0.25	752	35		≈ 6	+

SAMPLE #	SUBSTRATE	DOPANT	DOPING DENSITY n_d (cm ⁻³)	RAMP RATE (°C/min)	GROWTH TEMP (°C)	GROWTH TIME (min)	ΔT (°C)	EPILAYER THICKNESS (μ m)	COMMENTS
LR018-3	SI poly	u	--	0.25	752	35		≈ 6	+
LR018-4	SI poly	u	--	0.25	752	35		5.5	*
LR018-1A	SI poly	u	--	0.25	769	35		≈ 6	+
LR018-2A	SI poly	u	--	0.25	769	35		≈ 6	+
LR018-3A	SI poly	u	--	0.25	769	30		≈ 6	+

SI Semi-insulating

* Sample not available for shipment, cleaved to determine epilayer thickness

+ Sample available for shipment

u Undoped

n_s Carrier concentration of substrate

n_d Doping concentration of epilayer

poly Polycrystalline

TABLE II. Growth Experiments on Poly-GaAs substrates by Current Controlled Liquid Phase Epitaxy (CCLPE) at constant furnace temperature of 750°C.

SAMPLE NO	SUBSTRATE TYPE	CURRENT DENSITY A/Cm ²	GROWN LAYER TYPE	GROWN TIME (min)	GROWN LAYER THICKNESS (μm)
CC101-P	SI (Cr)	5	U	60	*
CC102-P	SI (Cr)	5	U	60	*
CC103-P	SI (Cr)	5	N-10 ¹⁸ (Te)120		7
CC104-P	SI (Cr)	5	N-10 ¹⁸ (Te)120		*
CC105-P	SI (Cr)	5	N-10 ¹⁸ (Te)60		+
CC106-P	SI (Cr)	5	N-10 ¹⁸ (Te)60		+
CC107-P	N ⁺ (Si)	5	U	60	*
CC108-P	N ⁺ (Si)	5	U	90	10
CC109-P	N ⁺ (Si)	5	U	90	*
CC110-P	SI (Cr)	2	U	60	-
CC111-P	SI (Cr)	2	U	15	*
CC112-P	N ⁺ (Si)	2	U	90	-
CC114-P	N ⁺ (Si)	2	U	30	-
CC115-P	N ⁺ (Si)	10	U	60	*
CC116-P	N ⁺ (Si)	5	U	120	*

U Undoped (probably n-type, 10¹⁶cm⁻³)

* Samples were not cleaved - available for shipment

+ Growth did not take place due to excessive joule heating

- Partial Growth due to partial wetting of contact film between substrate and graphite electrode.

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Future experiments will be directed towards growth and characterization of GaAs layers on poly-GaAs and graphite substrates by CCLPE. A thin film of tungsten or other suitable metal will be deposited on the graphite surface to enhance wetting of the surface by the gallium melt. Hall measurements will be performed on polycrystalline GaAs layers grown on semi-insulating GaAs substrates and, on the basis of the results, attempts will be made to passivate the effect of grain boundaries as discussed in Sec. 3.7.

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3.0 INVESTIGATIONS OF GRAIN BOUNDARIES

Investigations of grain boundaries are in progress at all the contract institutions in various forms. Two measurement techniques included in this section (minority carrier lifetime and SIMS) do not yet deal directly with grain boundaries or polycrystalline material; however, they are under development and will be applied to polycrystalline material. Experiments using scanned electron beams (scanning Auger potential profiling, cathodoconductivity) and laser scanning photovoltage experiments are directly investigating majority and minority carrier properties near grain boundaries. Theoretical investigations of grain boundaries as modeled by clusters of dislocations are also in progress.

3.1 Measurements of Minority Carrier Lifetime in GaAs (Brown University)

Since the transient capacitance lifetime measurement has not been utilized previously we begin with a discussion of the principles underlying this measurement of lifetime in GaAs. This technique is under development for future application to polycrystalline material. This discussion is followed by a summary of experimental results obtained on MOS devices in which the native oxides are produced by plasma oxidation and by anodic oxidation.

3.1.1 Measurement of Lifetime by Transient Capacitance

For a MOS capacitor formed on a semiconductor with a stable oxide, the system behaves very much like a capacitor whose capacitance C changes as a function of the applied dc bias, V , as shown in Figs. 2a to c. This figure shows the energy band diagram and the C - V characteristic for various values of the applied voltage V to a p-type semiconductor. In Fig. 2a, V is negative on the metal with respect to the semiconductor. This causes holes to accumulate at the oxide-semiconductor interface. The capacitance, $C = C_{ox}$; when its value is given by $C_{ox} = \epsilon_{ox}A/W_{ox}$. In Fig. 2b, V is slightly positive and depletion layer is produced at the oxide-semiconductor interface. The

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Fig. 2 Energy band diagram and C-V characteristics for p-type MOS structure on GaAs. (Details are explained in the text.)

Fig. 3 Capacitance-voltage and capacitance-time plots for an MOS p-type structure switched from negative bias to strong positive bias.

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total capacitance C is given by C_{ox} in series with the depletion layer capacitance C_d ; the latter varies as $V^{-1/2}$ as in an abrupt p-n junction. In Fig. 2c, V is strongly positive. The intrinsic level E_i crosses the Fermi level E_F . In steady state, this condition implies that a layer close to the semiconductor surface is "inverted", i.e. the concentration of free minority carriers is high near the surface. Any further increase of the voltage leads to an increase in the population of minority carriers in the inverted layer, but does not increase the width of the depletion layer in the semiconductor. The capacitance in inversion, C_I , is constant and it is equal to C_{ox} in series with the capacitance of the depletion layer of maximum width C_{dI} .

The build-up of the inversion layer is a relatively slow process so that if an MOS capacitor is switched from negative (V_1) to strong positive bias (V_2), (shown in Fig. 3) the semiconductor initially gets deeply depleted and the total capacitance of the capacitor is much smaller than C_I . C increases toward C_I as the generation of minority carriers in the depletion layer increases the concentration of minority carriers in the inversion layer. This process occurs with a time constant

$$T = N\tau/n_i \quad (1)$$

n_i being the intrinsic carrier concentration, N the doping concentration, τ the minority carrier generation lifetime.

The advantage of this method for measuring the short lifetimes in the semiconductor like GaAs is apparent: since $n_i = 10^7/\text{cm}^3$, if $N = 10^{16}/\text{cm}^3$, T is nine orders of magnitude larger than the lifetime to be measured, thus greatly simplifying instrumentation problems.

A more detailed analysis of the inversion layer formation shows that it is influenced by the rate at which minority carriers recombine at the oxide-semiconductor interface. Thus, the analysis of the capacitance

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transient allows one to measure both τ and the interface recombination velocity, S .

3.1.2 Design of the MOS Capacitor

The choice of W_{ox} is related to the doping concentration of the semiconductor N because the semiconductor maximum depletion width in inversion W_M is a function of N . Now

$$W_M = \frac{\epsilon_{GaAs}}{\epsilon_{ox}} W_{ox} \left(\frac{C_{ox}}{C_1} - 1 \right) \quad (2)$$

Figure 4 in turn shows how W_M depends on N . Because the measurements are more accurate if $C_{ox}/C_1 \sim 2$, and because, for GaAs, $\epsilon_{GaAs}/\epsilon_{ox} \sim 1.85$, a reasonable choice is $W_{ox} = 0.55 W_M$. However, W_{ox} is not a critical parameter and usually it is sufficient to know only the order of magnitude of the doping to obtain an acceptable MOS device,

The curve showing W_M vs N , Fig. 4, gives the thickness of the depletion width in inversion. The epilayer must be thicker than W_M (at least twice W_M) in order to accommodate the deep depletion layer which occurs under non-equilibrium conditions during the capacitance transient. There is no absolute maximum thickness of the epilayer; however, there is no way to obtain a depletion width greater than that corresponding to the width which results in avalanche breakdown of the semiconductor, W_B (Fig. 4). Therefore, there is no reason to grow epilayers thicker than W_B which is a function of the doping concentration.

An optimum capacitor size is a function of the minimum capacitance which can be confidently measured experimentally. A reasonable choice is to set $C_{ox} \sim 1\text{pF}$. with a doping concentration of 10^{15} cm^{-3} . For an optimized oxide thickness, the minimum area is about 10^{-4} cm^2 .

Fig. 4 Depletion width as a function of doping concentration, for inversion and breakdown conditions of a p-type MOS GaAs device.

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3.1.3 Plasma Oxidation Process and the Fabrication of MOS Capacitors

The principle of plasma oxidation consists of producing a GaAs native oxide by bombarding the GaAs surface with low energy negatively charged oxygen atoms. The plasma reactor we use is sketched in Fig. 5.

The chamber is first evacuated to a pressure of 10^{-5} torr, then it is filled with oxygen at a pressure of 2×10^{-3} torr, and a plasma is formed with rf applied between electrodes A A'. The stage B holds the sample; it is biased positive with respect to the plasma. A stainless steel mask, C, defines the area to be oxidized. The window on this mask is 6 x 6 mm. The stage B also contains a heater and a thermocouple. The plasma is confined with a coil that surrounds the reactor; the confinement both increases the plasma density in the useful region and reduces the contamination from the reactor walls.

The fabrication process consists of the following major steps:

1. Evaporation onto the substrate of the alloys Ag-In-Zn (p-type substrates) or Ag-In-Ge (n-type substrates) 90-10-10 by weight.
2. Annealing in the plasma reactor at a pressure of 10^{-5} torr, at 350°C for 30 minutes. This bonds the alloy to the substrate thus forming an ohmic contact.
3. Oxidation at a bias between 50 and 90 volt for a time ranging between 5 and 30 minutes. Both bias and time control the thickness of the oxide.
4. Evaporation of an aluminum contact on the oxide through a shadow mask.

3.1.4 Method of Analysis of the Lifetime

The devices are tested by plotting the following quantities with a PAR model 410 C-V plotter:

A-A' R.F. ELECTRODES
 B SAMPLE HOLDER
 C MASK
 D COIL

Fig. 5 Reactor for the plasma oxidation of GaAs, at Brown University.
 (Parts are described in the text.)

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- capacitance voltage curve (C-V)
- conductance voltage curve (G-V)
- capacitance transient following switching from accumulation to deep depletion (C-T)

The oxide thickness and doping concentration of the semiconductor are obtained from the C-V curves. It is very important to measure the doping locally in the same volume where lifetime will be measured because this quantity defines the proportionality factor between capacitance transient and the lifetime.

Information about the quality of the oxide, in particular the breakdown field and the loss tangent $G/\omega C$, are obtained from the G-V curves.

The lifetime τ and the interface recombination velocity are calculated from the C-T curves.

Finally, we plot the "fast" capacitance-voltage curve, i.e. the C-V curve generated by a sweep rate too fast to allow an inversion layer to form. This results in a plot of the deep depletion C-V curve that can be used for obtaining the doping concentration and, in low doped materials, the profile of doping as a function of depth as is done by analyzing the C-V curves of a p-n junction.

3.1.5 Results on the Materials Supplied by Rockwell Science Center

(DOE-SC-12), Substrate #1291

This is p on p⁺ LPE grown, Ge doped material. The slice was about 3/4" x 1/2" and was cut into six, 1/4" squares. Most of this material has been used in an attempt to evaluate the technique suggested by R.P.H. Chang and J.J. Coleman (Appl. Phys. Lett. 32, 332, March 1978) who first reported an inversion condition in a GaAs MOS device. This technique consists of

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evaporating a thin (typically 50Å) Al layer onto the GaAs surface and obtaining a composite Ga-As-Al oxide with a plasma reactor.

Our results have not been satisfactory because of problems related to the control of the thickness of the Al layer and because the electrical properties of the composite oxide vary as the total thickness varies.

On the same material, after introducing some modifications in the MOS fabrication process that led to a substantial lowering of the maximum temperatures attained by the sample during plasma oxidation, we succeeded in obtaining a satisfactory inversion condition without the use of Al layer. This resulted in both a simpler and a more reliable process.

However, in our first attempts with this technique, we obtained oxide layers too thick (about 3000Å) to give reasonable quantitative results on this material.

DOE-SC-11, Substrate #1288

This material is also p on p⁺, LPE grown, Ge doped, GaAs. It has been divided into 6 squares 1/4" x 1/4". Part of this material has been used for growing a native oxide by anodic oxidation. The results have been quite poor, probably because of contamination from the chemicals used as electrolyte. In the samples processed with this method, we have not detected any reasonable capacitance transient.

Two samples have been plasma oxidized with suitable oxide thicknesses (450 and 700Å). This resulted in measurements more reliable than those obtained on the other material. A few results are reported in Table III. There, S_0 indicates the interface recombination velocity of the GaAs surface while S_{inv} is the value the interface recombination velocity assumes when the surface is "screened" by the inversion layer.

TABLE III

Device	Doping (cm^{-3})	Generation Lifetime (nsec)	Surface Recombination Velocity	
			S_o (cm/sec)	$S_{inv.}$ (cm/sec)
E2	2.9×10^{17}	2.6	3×10^5	9×10^3
E6	3×10^{17}	0.7	9×10^4	4.5×10^3
E9	2.8×10^{17}	1.2	1.1×10^5	1.5×10^3
F8	2.1×10^{17}	0.4	-	3×10^4
F10	2.3×10^{17}	0.6	5×10^5	2.5×10^3

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We did not attempt to build up a map of these quantities as a function of position on the epilayer because we made only a few MOS on each sample.

One sample has been oxidized, but no contacts were evaporated over it. This sample has been subjected to Auger analysis so that we could determine the composition of the oxide. The curves of As, Ga, and O contents as function of thickness are still being analyzed. The analysis is complicated by the fact that, as reported by R. P. H. Chang and co-workers (Appl. Phys. Lett. 30, 657 (1977)), the quantitative calibration of these data can not be carried out in the usual way.

DOE-SC-5, Substrate #1215

This is $\text{Ga}_{0.3}\text{Al}_{0.7}\text{As}$, p-type, Be doped, LPE grown on n^+ doped GaAs. We have contacted this material by evaporating Ag-In-Ge onto the substrate and Ag-In-Zn onto the epilayer and annealing the N_2 flow at 550°C for 30 minutes. Then we have etched mesa-style diodes in dilute nitric acid. The I-V characteristics show a breakdown voltage of 3 volt and an ideality diode factor $n = 1.8$. The $1/C^2$ vs V plot is nearly linear and indicates a doping concentration of $7.2 \times 10^{17}/\text{cm}^{-3}$. The minority carrier lifetime in the GaAlAs has been estimated with the Open Circuit Voltage Decay (OCVD) technique from the slope of the V - t curve near the origin. This measurement gives $\tau = 23$ ns. However, the absence of a well-defined straight line in the transient makes the accuracy of this measurement poor.

DOE-SC-6, Substrate #1216

This is $\text{Ga}_{0.7}\text{Al}_{0.3}\text{As}$, p-type, Be doped, LPE grown on n^+ Si doped GaAs. This material has been processed in the same way as DOE-SC-5 above. The breakdown voltage is 4.5 volts, the ideality diode factor $n = 1.5$. The $1/C^2$ vs V characteristic is linear up to 3 volts, the doping concentration is $1.2 \times 10^{18}/\text{cc}$. The minority carrier lifetime in the GaAlAs, estimated with OCVD technique $\tau = 69$ ns (an almost linear decay occurs for this device).

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DOE-SC-12, Substrate #1291

As pointed out above, most of this material has been used for making MOS devices. One piece has an epitaxial layer of CdS grown on it to form a heterojunction solar cell. The relevant parameters of this cell are: open circuit voltage = 300 mV, short circuit current = 8.7 mA/cm^2 , fill factor = 0.64, efficiency = 2.4%. More details are reported in the paper "Investigation of Potentially High Efficiency Photovoltaic Cells Consisting of Two Heterojunctions on a Common Wide Bandgap Semiconductor Base", by M. Arienzo and J. J. Loferski, presented at the 13th Photovoltaic Specialist Conference in Washington.

3.1.6. Anodic Oxidation of GaAs

As reported in the first quarterly report, anodic oxides grown on GaAs epilayers supplied by the Rockwell Science Center had good insulating properties and very promising C-V curves recorded by PAR model 410 C-V plotter.

In this quarter, attempts were made to use the capacitance transient technique to measure the minority carrier lifetime on a p on p⁺ GaAs epitaxial layer supplied by the Rockwell Science Center. Switching the MOS from accumulation to deep depletion resulted in a transient response of approximately 2 msec. The data supplied by Rockwell Science Center indicates that the carrier concentration in this sample was $\sim 10^{17} \text{ cm}^{-3}$. A crude approximation of the transient response yielded a bulk generation lifetime in the range of a picosecond. However, plasma oxidation on a piece cut from the same sample resulted in a bulk generation lifetime in the range of nanoseconds which is more nearly the expected lifetime for an epitaxially grown GaAs layer. After this result, lifetime measurements on GaAs samples supplied by different institutions were mainly made by oxidizing the samples in the plasma reactor. Activity on anodic oxidation has concentrated mainly on improving the system to make cleaner and better quality oxides. An anodic oxide

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prepared on a bulk p-GaAs sample will be analyzed by Auger spectroscopy to compare the composition of the oxide grown anodically to those grown by plasma oxidation.

It is assumed that the large discrepancy in the lifetime measurements is due to a large interface state density in the anodically grown oxides as compared to plasma grown oxides, and also due to some oxide charging current as suggested by Kohn and Hartnagel.¹ It is assumed the surface generation recombination process in anodic MOS structures on GaAs cannot be neglected as is the case in MOS structures on Si. The interface-state band model for GaAs MOS structures proposed by Hasegawa² predicts that the analysis developed for Si MOS structures cannot be applied in this case.

Attempts are being made not to use Al_2O_3 on top of anodic native oxide which presumably improves the interface properties of the native oxide-GaAs system, because the analysis is complicated by using two different insulating layers. Also, we are going to attempt to make anodic oxides in a cleaner environment and using purer chemicals to see if we can improve the quality of the interface.

We also intend to use this kind of oxide to make the insulating layer on a MIS solar cell. This type of solar cell requires an insulating layer of less than $20\text{\AA}$, and it is not obvious that the anodic oxides can be grown this thin. However, we are going to attempt it and investigate the MIS cell fabricated by this process.

3.2 SIMS Characterization of GaAs (Cornell University)

A major part of the SIMS solar cell program to date has been the study of ion implanted samples to provide standards. The SIMS technique is under development as a means to detect spatial variations in dopant or contaminant concentrations in single or polycrystalline GaAs epilayers. Figure 6 shows the negative secondary ion profile of ^{16}O , implanted into GaAs

04-JUL-78 AT 00:57:35
O IMPLANT IN GAAS (R010A)
SUN45.DAT

Fig. 6 SIMS ^{16}O secondary ion profile of an oxygen implant in GaAs, as a function of sputtering time.

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at an energy of 100 keV to a fluence of $1.9 \times 10^{12}/\text{cm}^2$. Argon was used for the primary ion sputter beam to eliminate primary beam interference. The signal observed for the estimated peak concentration of $10^{17}/\text{cm}^3$ suggests that a detection limit of about $5 \times 10^{14}/\text{cm}^3$ oxygen can be expected in GaAs.

Implants of this type will be used as external standards, analyzed under the same vacuum conditions as samples having unknown levels of the ion implanted species. This will apply to analyses for intentional dopants as well as for undesirable impurities such as oxygen and silicon. Practical application of this method of polycrystalline samples will begin in the coming quarter.

The interference of Al^{+3} in the analysis of Be in AlGaAs has been mentioned in previous reports. Since the increased mass resolution required to separate these two species is accompanied by a substantial loss in sensitivity, an alternate approach is being taken. An attempt will be made to determine the contribution of Al^{+3} to the secondary ion signal at mass 9, and then to subtract it from the total signal, leaving only the Be contribution. Preliminary results indicate that this is feasible, and confirmation is underway utilizing samples recently received from the Rockwell Science Center. Final results will also depend on a more accurate characterization of these samples, to be received in the near future.

3.3 Scanning Auger Spectroscopy and Cathodoconductivity Investigation of Carrier Transport Across a Twin Boundary in MBE GaAs (Science Center)

Effects of grain boundaries on the performance of polycrystal solar cells can be grouped into two major categories: 1) excess electron-hole recombination at grain boundaries, resulting in a decrease in the short circuit current and, 2) the introduction of a shunt resistance across the device junction, resulting in a decrease in the open circuit voltage. This section reports an experiment which attempts to measure some relevant parameters of such processes.

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The traditional method for determining the majority carrier transport properties in a single crystal semiconductor sample is through the measurement of the dc conductivity. The minority carrier transport properties are deduced from photoconductivity experiments. As a first effort to understand the problems involved in the fabrication of high efficiency polycrystalline solar cells, we have focused our attention on the measurement of the majority and minority carrier transport properties of a sample containing a single grain boundary. The sample configuration was described in the last quarterly report, but briefly consists of a 5 micron wide n-type GaAs mesa, 2 microns thick, grown on semi-insulating GaAs substrate which contained a single twin plane. The conducting layer was grown using MBE and its morphology reflects the twin boundary of the substrate. Ohmic contacts were then applied 20 microns apart spanning the grain boundary.

In order to measure the majority carrier transport properties on such a microscopic sample, we have used the Auger potential profiling method which was also described in last quarter's report. A potential is applied across the grain boundary and the Auger spectrum is measured as a function of location along the sample. The shift of the Auger spectrum can be used as a voltmeter with a voltage resolution of approximately a tenth of a volt and the spatial resolution of a half micron, which is the beam size. In Fig. 7, we have plotted the results of a measurement on a sample which did not contain a grain boundary. As can be seen, the applied potential appears across the contacts and the voltage between the contacts increases linearly with distance as would be expected from an ohmic sample. In Fig. 8, we have repeated the experiment on a sample which contained a grain boundary. Again, the contacts reflect the applied potential and as the electron beam was swept across the sample, the potential shift of the Auger spectrum was linear, indicating the ohmic resistivity of the material. A jump in the voltage was seen at the grain boundary; in this case, approximately a volt and a half and then the increase in potential again continued linearly until the second contact.

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Fig. 7 Voltage shift of the AES carbon line, as a function of distance across a mesa stripe epilayer without a grain boundary.

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Fig. 8 Voltage shift of the AES carbon line, as a function of distance across a mesa stripe epilayer with a grain boundary. (Doping density was $n \sim 2 \times 10^{15}/\text{cm}^3$.)

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The width of the jump in voltage is wider than the size of the measuring beam and must be understood in terms of the majority carrier transport properties of the sample. To model this behavior, we can consider the grain boundary to result in a potential barrier in the band structure which repels majority carriers and traps minority carriers. The band diagram is similar to back-to-back Schottky diodes. As a bias is applied to the sample, some of the voltage drop occurs due to the resistivity of the material on either side of the grain boundary, but one half of the grain boundary depletion region (or one of the back-to-back diodes) is reverse biased and the bulk of the voltage falls across the depletion region of the diode.

This experiment illustrates that the spatial extent of the effects of the grain boundary on the majority carrier flow extend a depletion width into the surrounding crystal sample. In the case of lightly doped material, this may be wider than the diffusion length. In order to measure the minority carrier transport flow, we have performed the microscopic spatially resolved analog of photoconductivity in a SEM. The experiment is illustrated in Fig. 9. A bias is applied across the sample and the resulting current is measured. The electron beam is focused on a spot on the sample inducing excess carriers, we then chop the electron beam and the resulting ac component of the current is detected with a lock-in amplifier. The beam is swept across the sample and X-Y recorder plots the induced ac component of the current as a function of the injection location on the sample. The electron beam used has a current of 2 nA at 20 keV. A 20 keV electron incident on the solid typically scatters elastically over a two micron diameter volume within the sample, and in the case of a semiconductor induces carriers throughout that volume. In this experiment, the spatial resolution is therefore limited to the blooming diameter of the electron beam, which is about two microns.

In Figs. 10 and 11, we plot the induced current as a function of injection location on samples with and without a grain boundary. The sample in Fig. 11 had a donor concentration of about $10^{17}/\text{cm}^3$ and that in Fig. 12 had

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Fig. 9 Schematic of the measuring circuit for cathodoconductivity measurements using the SEM.

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Fig. 10 Electron beam induced current in a mesa stripe epilayer with $n \sim 2 \times 10^{15}/\text{cm}^3$ without a grain boundary.

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Fig. 11 (a) Electron beam induced current in a mesa stripe epilayer with $n \sim 1 \times 10^{17}/\text{cm}^3$, containing a grain boundary.

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Fig. 11 (b) The same scan as in part (a), with bias voltage reversed.

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Fig. 12 (a) Electron beam induced current in a mesa stripe epilayer with $n \sim 2 \times 10^{15}$, containing a grain boundary.

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Fig. 12 (b) The same scan as in part (a), with bias voltage reversed.

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a concentration of about $2 \times 10^{15}/\text{cm}^3$. In Fig. 10, where we have no grain boundary, the induced current rises as the beam crosses the contact onto the sample, remains more or less steady across the width of the sample, and then falls off at the second ohmic contact. In the heavily doped sample of Fig. 11, induced current is such that only the minority carriers injected between the grain boundary and the collecting contacts are measured. Figures 11a and 11b are measurements on the same sample with the bias voltage reversed. In Fig. 12, the lightly doped sample, this effect is not evident. While the grain boundary can be seen, the comparison of Fig. 12a and 12b indicates that the minority carrier transport properties will be more difficult to extract.

This experiment is still in the preliminary stages and the results are not well understood. What is apparently happening in the heavily doped sample, where we are inducing a current of approximately a microamp in a sample with a majority carrier dc current of a milliamp, is that we are performing a true cathodoconductivity experiment, which is sensitive only to the minority carrier properties. In the lightly doped sample, however, we are again inducing a microamp in a sample whose dc current is only about 5 microamps. Thus, it is not clear that it is justified to define a minority carrier. In the coming quarter we intend to carry out continuing experiments both of Auger potential profiling and cathodoconductivity on n-type material, p-type material, lightly and heavily doped in order to devise a model which will allow us to extract both the majority and the minority carrier transport properties from the data.

3.4 Examination of GaAs Twin Boundary with the Laser Scanning System (Cornell University)

The intent of this experiment is to measure the effect of grain boundaries on photovoltage produced by a scanned laser. The sample was an MBE GaAs:Sn layer grown on twinned (100) semi-insulating substrate. In this study, the relative photovoltage of the twins was investigated.

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The unpolished side of the sample was silver painted onto an aluminum mount. This aluminum mount was one electrode. The other electrode was a point contact made at a Ga dot on the polished side. The photovoltage across these electrodes was monitored while scanning a laser beam across a twin. Results of this scan are shown in Fig. 13.

Both Figs. 13a and 13b were made with the 6328Å line of a He-Ne laser. The diameter of the laser spot was ~2 microns in Figs. 13a and 1 micron in Fig. 13b. Figure 13a shows a baseline, the photovoltage, and 3 calibrating dots spaced 100 microns apart (near top of figure). The photovoltage at the twin is greater than that away from the twin by a factor of 1000. Figure 13b shows a raster scan of the twin. Some sub-structure is observable in this scan.

Further investigation into the spatial structure of the twin's photo-voltage is shown in Fig. 14. At one end of the twin, the twin appears as a peak in the photovoltage, as in Fig. 14a. At the other end of the twin, the photovoltage is an abrupt step at the twin, as in Fig. 14c. The region of transition between a photovoltage peak and step is shown in Fig. 14b. The higher side of the photovoltage step in Figs. 14b and 14c is the side nearest the Ga point contact, as would be expected.

Preliminary diffusion length measurements were made both at the twin and away from it. The method used was the steady state photovoltage method.³ The 647 nm, 752 nm and 799 nm lines from a krypton ion laser were used. Results are inconclusive so far, most likely due to the high absorption of these lines in GaAs.

3.5 Measurement of Schottky Barrier Parameters on Polycrystalline MBE Material (Science Center)

In order to determine the effect of grain boundaries and different crystal orientations on Schottky barrier parameters, an array of Au Schottky

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(a)

(b)

Fig. 13 (a) Photovoltage across a twin boundary in GaAs. (The calibrating dots are $100\mu\text{m}$ apart.) (b) Rastered photovoltage scan of the same twin boundary as in part (a).

(a)

(b)

(c)

Fig. 14 Photovoltage of a twin boundary region at the top (a), center (b) and bottom (c) of the sample, showing the transition between a stepped and peaked structure.

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contacts were evaporated onto an n-type MBE epilayer with $n \sim 10^{17} \text{ cm}^{-3}$ on a polycrystalline n^+ substrate. These diodes were then measured to determine their current voltage and capacitance-voltage characteristics, to determine whether or not the metal-semiconductor barrier height, diode saturation current, and diode ideality factor depended on the diode location, e.g. on or off a grain boundary.

The surface morphology of the epilayer is shown in Fig. 15, which is an optical phase-contrast micrograph showing the intersection of several grains. The substrate consisted of randomly oriented crystallites ranging from sub-millimeter to about one centimeter across. These had been polished with Cabosil and clorox, and then etched lightly with $\text{NH}_3\text{OH}/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (10:1:1) to leave a smooth surface, except for very light delineation of the grain boundaries. (This procedure was discussed in more detail in the first quarterly technical report.) MBE growth occurred on all crystallites, but as seen in the photograph, there is a strong preferred growth direction which resulted in an uneven surface for most of the crystallites. The characteristics of thirteen diodes were measured; six straddled grain boundaries and seven did not. Barrier height, as extrapolated from plots of $1/C^2$ vs V , ranged from 0.87 eV to 0.98 eV, averaging 0.92 eV. Diode ideality factors ranged from 1.13 to 1.51, averaging 1.26. Saturation current, extrapolated from plots of $\ln I$ vs V in forward bias, ranged from $7 \times 10^{-10} \text{ a/cm}^2$ to $1.6 \times 10^{-7} \text{ a/cm}^2$. Some of this variation could be attributed to difficulty in extrapolating non-ideal I-V characteristics.

The most surprising finding of this study is that there was no correlation between the positioning of the diode (grain boundary or not; surface roughness or crystallite orientation) and any of the measured characteristics. Large barrier heights or small barrier heights tended to cluster together in the same areas of the crystal, but these areas spanned several different grains, suggesting this effect was more due to diode fabrication or substrate variations other than grains than to the actual grain

Fig. 15 Optical macrograph, phase contrast enhanced,
of an MBE GaAs epilayer on polycrystalline
GaAs. (Several grains are visible.)

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boundaries. This experiment will be repeated with different doping densities and SIMS analysis will be done of the entire substrate to look for impurity variations across the substrate as well as at the grain boundaries.

3.6 Theoretical Investigations of Grain Boundaries (NCA&T)

During this quarter, a model has emerged which can be used to describe the electronic properties of dislocations in GaAs with a relatively small number of parameters. These parameters will be determined from experiments proposed to be conducted at A&T. The dislocation model can be adapted to grain boundary modeling with minor modifications.

The edge dislocations in III-V semiconductor compounds are of two major classifications: type A (a Ga core dislocation) and type B (an As core dislocation). Primary emphasis here is given to the edge dislocation due to its production of a dangling bond whose energy levels lie deep in the forbidden band gap. Screw dislocations will be discussed under a separate section.

Shown in Fig. 16 is a single dangling bond associated with A or B dislocations. A single dangling bond can accommodate up to 2 electrons. The first electron can be added more easily than the second due to the screening of the parent nucleus and the electrostatic repulsion of the two added electrons. Thus, there are at least two energy levels associated with a single dangling bond. These levels are referred to as the one and two electron flaw levels and will be denoted by energies E_1 and E_2 , respectively. Adjacent atoms on the dislocation core interact causing a broadening of the one and two electron flaw levels into bands. The flaw band models for A and B are shown in Fig. 17. This band scheme is similar to that proposed by Mueller and Jacobson⁴ for InSb. The one electron band for the A type dislocation is shown 3/4 filled in its neutral state, while for B, the one and two levels are 5/4 filled in the neutral state.

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Fig. 16 A representation of dangling bonds associated with A or B type dislocations.

E_c

NEUTRAL GA-LIKE
DISLOCATION BANDS

NEUTRAL AS-LIKE
DISLOCATION BANDS

Fig. 17 Dislocation band structure used for A and B dislocation types.

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With such a flaw band scheme, the Fermi level position can dictate the charging properties of the dislocation core. For example, with the Fermi level above the neutrality level, the dislocation core will accept electrons and become negatively charged. If the Fermi level is below the neutrality level, the core loses electrons and become positively charged. In n-type InSb, the A dislocations charge negatively, while the B do not charge, but in p-type material both A and B charge positively. A negative core charging in n-type material or a positive core charging in p-type material, and the resulting space charging around each, greatly increases the recombination rate at the dislocation due to the core acting as a sink for the minority carriers.

Schockley and Last⁵ have shown that a flaw will continue to accept electrons if the net change in free energy ΔF is negative, where

$$\Delta F = E_{i+1,i} - E_F \quad (1)$$

where $E_{i+1,i}$ is the total free energy change associated with the flaw going from the charge state i to the $i+1$ state. This is seen to be the case if $E_F > E_{i+1,i}$. Even though a given electronic energy level of a flaw is below E_F , it may not change charge state if the total free energy due to the charging is greater than E_F .

Either the theory of Shockley and Last⁵ for localized flaw levels or the theory of Read⁶ for dislocations in Ge, can be adopted for the occupational statistics of dislocations in GaAs. In fact, it can be shown that the two theories are equivalent in the limit that the number of dangling bonds $N \rightarrow \infty$. It is assumed here that edge dislocations are of sufficient length that the theory of Read may be used.

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In n-type material, the total change in free energy per added electron associated with an electron taking up residence on the dislocation core at $T = 0^\circ\text{K}$ is

$$\Delta F = E_1 - E_F + E_S(f) \quad (2)$$

where E_1 is the neutrality level, E_F is the Fermi level, and E_S is the total electrostatic energy associated with the space charge field of the dislocation assuming a uniform distribution of excess negative charge along the core. E_S depends on the occupational probability of the core. It is noted that $E_S(f)$ has the effect of pushing the electronic energy level E_1 higher in energy so that eventually a f value is reached such that $(E_1 + E_S(f))$ will be above the Fermi level and charging will cease. For $T > 0$, the electrons on the dislocation core acquire enough thermal energy that deviations from uniformity along the core occur. This leads to an additional term in the free energy

$$\delta F_S = E_S - TS. \quad (3)$$

The entropy of a uniform distribution of charge along the core is zero since there is only one way to achieve this. Any deviation from uniformity raises the entropy and lowers the free energy for $T > 0$.

The total free energy of a dislocation with N dangling bonds and with occupational probability, f , is

$$\Delta F = NfF = Nf(E_1 - E_F + E_S - TS) \quad (4)$$

The thermal equilibrium occupational parameter f is that value which minimizes the free energy.

$$f = \left[- \frac{E_1 - E_F + E_S + \delta E_S - TS}{\frac{\partial}{\partial f}(E_S + \delta E_S - TS)} \right] \quad (5)$$

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Analytic expressions for each of the terms as a function of f are given in the Appendix. Details of the numerical solution of the transcendental Eq.(5) are described in the Appendix.

The space-charge radius of the cylinder around an edge dislocation can be written from the charge neutrality condition giving,

$$R = [f/\pi cN_D]^{1/2} \quad (6)$$

where N_D is the donor density and C is the distance between dangling bonds on the core,

$$C = \frac{b \sin 60^\circ}{\sin \alpha}$$

where α is the angle between the Burger vector $b(=4.00A)$ and the slip direction.

3.6.1 Results of the Numerical Calculation

To ascertain the charging properties of A and B dislocations, the charging characteristics have been investigated for arbitrary placement of the flaw energy levels. In Fig. 17 are shown the unknown parameters used in the theory. E_1^A is defined as the neutrality level for the A dislocation. E_2^B is the bottom of the two electron flaw band of A and E_2^B is the neutrality level in the two electron flaw of the B dislocation. The broadening parameter b_1 is assumed to be approximately the same for all flaw levels (a value of $b_1 = .1$ eV is used in these calculations).

Figure 18 shows the space charge radius of the A dislocation assuming E_2^A is in the conduction band (thus playing no role in localized core charging) and with $E_1^A = .3$ eV. The space charge radius R is given by

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Fig. 18 Space charge radius R^A as a function of the Fermi level E_F (on the top scale) and the donor density N_D (on the lower scale).
($E_1^A = .3$ eV, $E_2^A > E_c$, and $T = 300^\circ\text{K}$.)

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Eq. (6). The maximum change in free energy, $\Delta F_{\max} = .25$, occurs for $N_D = 2 \times 10^{13} \text{ (cm}^{-3}\text{)}$. With a fixed $f_{\max}$ in the numerator of Eq.(6), the radius R must necessarily decrease as $(N_D)^{1/2}$ when N_D increases.

Figure 19 shows a similar plot for the space charge radius for B dislocations with $E_2^B = .3$. The maximum $\Delta F_{\max} = .75$ occurs only for $N_D \geq 3 \times 10^{18} \text{ (cm}^{-3}\text{)}$. The reduction in R as N_D increases can be understood as follows. As N_D increases from 10^{14} , the Fermi level rises and uncovers free energy levels that can contribute to core charging; this increases f . However, the small increase in f was accomplished only at the expense of a large increase in N_D . The denominator in Eq.(6) dominates and R reduces with increasing N_D .

Figures 20 and 21 are analogous to Figs. 18 and 20, except that $E_1^A = .5$ and $E_2^B = .5$, respectively. In this case, $f_{\max} = .25$ occurs at $N_D \geq 2 \times 10^{14}$ and $f_{\max} (= .75)$ cannot be achieved. The fact that $f^B < .75$ is because some of the free energy levels for core charging are now above the conduction band.

Figures 22 through 27 show the results of pushing E_1^A and E_2^B even higher in energy. It is noted that there is a reduction in R over the entire N_D range as E_1^A and E_2^B are raised higher. This reduction persists because more free energy levels are being driven higher in energy and are becoming inaccessible to uncovering by the Fermi level. Since more levels remain frozen out for all values of N_D , f in general reduces as E_1^A and E_2^B are raised for all values of N_D .

Figures 17 through 27 demonstrate that the smallest space charge region occurs for high values of N_D regardless of flaw level position. With this in mind, our attention is focused on space charging in heavily doped samples $10^{18} \text{ (cm}^{-3}\text{)}$. Figure 28 shows the effects of E_1^A level on the space charge radius with $E_2^A > E_c$ and $N_D = 10^{18} \text{ (cm}^{-3}\text{)}$. The radius remains constant

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Fig. 19 Space charge radius R^B as a function of the Fermi level E_F (on the top scale) and the donor density N_D (on the lower scale).
($E_2^B = .3$ eV and $T = 300^\circ\text{K}$.)

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Fig. 20 Same as Fig. 18 except $E_1^A = .5 \text{ eV}$.

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Fig. 21 Same as Fig. 19 except $E_2^B = .5$ eV.

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Fig. 22 Same as Fig. 18 except $E_1^A = .9$ eV.

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Fig. 23 Same as Fig. 19 except $E_2^B = .9$ eV.

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Fig. 24 Same as Fig. 18 except $E_1^A = 1.1 \text{ eV}$.

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Fig. 25 Same as Fig. 19 except $E_2^B = 1.1$ eV.

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Fig. 26 Same as Fig. 18 except $E_1^A = 1.3$ eV.

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Fig. 27 Same as Fig. 19 except $E_2^B = 1.3$ eV.

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Fig. 28 Space charge radius R^A as a function of E_1^A . ($N_D = 10^{18} \text{ cm}^{-3}$, $T = 300^\circ\text{K}$, and $E_2^A > E_c$.)

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($f = f_{\max}^A = .25$) over much of the range of E_1^A . The constant value is 1.186×10^{-6} cm. For $E_1^A > 1.2$ eV, there is sharp reduction in R as E_1^A increases. This is because the free energy levels for core charging are initially frozen out.

In Fig. 29, $E_1^A = .3$ is fixed, $N_d = 10^{18}$ (cm^{-3}), and R is investigated as function of E_2^A . Finally, E_2^A is pushed so high in energy that it does not contribute to f and R again assumes the constant value of 1.186×10^{-6} cm. Figure 30, likewise shows the reduction in R as E_2^B is raised in energy (again $N_D = 10^{18}$ cm^{-3}).

3.6.2 Screw Dislocations

Screw dislocations, without an edge component, produce no dangling bonds. This can be seen from the equation for spacing between dangling bonds,

$$C = \frac{b \sin 60^\circ}{\sin \alpha}$$

For a pure edge dislocation, $\alpha = 90^\circ$ and $C = b \sin 60^\circ$. For a pure screw dislocation, $\alpha = 0^\circ$ and $C \rightarrow \infty$. The distance between dangling bonds in a screw dislocation is infinite, or stated differently, there are no dangling bonds. However, even though no dangling bonds exist in a pure screw dislocation, bonds are severely stretched, i.e. there are regions of compression and dilatation in the crystal associated with such a dislocation. In regions of compression or dilatation, the local atomic density increases or decreases respectively. As Heine⁷ has shown, a local density excess tends to pull states into the bandgap from the valence band while regions of lower density tend to pull states out of the conduction band.

In the experiments proposed here to be conducted at A&T, edge or screw dislocations can be selectively introduced into a sample by simple bending or twisting such that each can be studied separately. In this way,

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Fig. 29 Space charge radius R^A as a function of E_2^A . ($N_D = 10^{18} \text{ cm}^{-3}$, $T = 300^\circ\text{K}$, and $E_1^A = .3 \text{ eV}$.)

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Fig. 30 Space charge radius R^B as a function of E_2^B . ($N_D = 10^{18}$ cm $^{-3}$ and $T = 300$ K.)

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one can understand the relative importance of the edge and screw dislocations in the recombination process.

3.6.3 Summary of Theoretical Investigations

This theoretical research has shown that the space charge radius associated with core charging of dislocations is lowered as the donor density N_D is increased ($N_D \geq 10^{14}$). The space charge radius reduction is of vital importance since the region serves as a sink for minority carriers. The largest space charge radius (with $N_D = 10^{18} \text{ cm}^{-3}$) that one must be concerned with is $R_{\max} < 2 \times 10^{-6} \text{ cm}$. This means that tilt grain boundaries such as shown in Fig. 31 can be treated as a collection of non-interacting (non-overlapping) dislocation space charge cylinders provided

$$\theta < \theta_{\max} = 2 \sin^{-1} \left(\frac{C}{4R_{\max}} \right) = .81^\circ$$

It is also noted from Eq. (6),

$$R = [f/(\pi C N_D)]^{1/2},$$

which was derived from charge neutrality within the cylinder, that it may be possible to reduce the space charge region to essentially zero by increasing the local density of donors at the site of the dislocation. In the calculations presented here, N_D around a dislocation core was assumed to be the same as the bulk donor density. However, Eq. (6) remains valid for a local donor density $N_D(\text{loc})$ different from the bulk value. Since the bulk donor density controls the Fermi level, f will not change appreciably by a local increase in N_D . Such a local increase may be achieved by impurity diffusion.

It is well known that impurity diffusion and segregation occur at dislocations (grain boundaries). Simple annealing of a polycrystalline sample

Fig. 31 Dislocation model of a tilt grain boundary.

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will cause this to occur. However, it must be cautioned, simple annealing a polycrystalline sample may not necessarily decrease the space charge region at the grain boundary. An impurity which acts as a donor at a substitutional site in GaAs may, in fact, act as an acceptor when placed in the free space region of a dislocation core.

Intentional diffusion using impurities with known molecular donor characteristics (instead of known crystalline donor characteristics) seems to be a better approach. Examples of these are the alkali metals: Li, Na, K, etc.

The future theoretical work is toward extending the dislocation model of grain boundaries to include tilt grain boundaries where $\theta > 1^\circ$. In this case, overlap of the dislocation cylinders occurs. The dislocation interaction term must be included into the free energy before an occupational parameter f can be calculated for the dislocations at the grain boundary. The proposed experimental work in the next section, when matched with the theoretical curves, will help to locate the unknown parameters in the theory presented here. In this way, a comprehensive study of a GaAs grain boundary can be achieved.

3.7 Experimental Investigations of GaAs Dislocations (NCA&T)

This experimental work is based on the assumption that an understanding of the grain boundary in GaAs, at least initially, can be extrapolated from an understanding of the single dislocation; that is, the dislocation is the basic unit of the grain boundary from which various models will be assembled.

3.7.1 Crystallography of GaAs

The structure of GaAs is that of diamond except for the alternation of the elements in successive sites. As a result, this structure, unlike diamond, does not possess a center of inversion. This creates geometric

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anisotropy in which opposite directions are not necessarily equivalent. Figure 32, which is an expanded view of the (011) plane, shows that there is a distinction in the composition of the (111) and ($\bar{1}\bar{1}\bar{1}$) faces. This structural peculiarity has several consequences.

The geometry of dislocations in diamond structures is well known and the most probable structures have been determined;^{8,9} in GaAs the complication of lattice polarity makes it probable that most exist in two forms. The easiest to depict (and also probably the most mobile) is the 60° dislocation shown in Fig. 33. The solid lines represent the covalent bonds, the extra half plane ending on a row of Ga or As atoms; called A and B dislocations, respectively. These dislocations are primarily edge type, with a small screw component. There are actually two classes of 60° dislocation, the type shown in Fig. 33, the "shuffle" type,⁸ and the "glide type".⁹ The glide is not expected to be mobile.

Consideration of the rules of dislocation motion in ionic solids, i.e. conservation of Burger's vector and charge opposition, results in the expectation that the 60° dislocation is the most mobile in GaAs.⁶ TEM observations have confirmed that the predominant slip system in GaAs is (111)($\bar{1}\bar{1}\bar{0}$),¹⁰ and that the majority of mobile dislocations have the vector $b = a/2(110)$.¹¹ The dislocations lie mainly along (110) and (112) directions, the subgrain boundary being (110).

If a single crystal is bent, as in Fig. 34, excess edge dislocations form as shown to accommodate the curvature. In GaAs, due to the polarity restriction, these dislocations have to be either all A or all B type, or at least a majority of any one type.

We must also consider the stress state on the slip plane. The maximum shear occurs at 45° to the neutral axis, and the shear forces acting on dislocations on shear planes are as shown in Fig. 35. Thus, dislocations of

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Fig. 32 Polar nature of GaAs.

Fig. 33 The 60° dislocation in GaAs.

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Fig. 34 Formation of excess edge dislocations to accommodate bending.

Fig. 35 Shear forces on two arbitrary slip planes.

Fig. 36 Orientation of bending sample.

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one type are driven toward the outer surfaces, and the other type toward the neutral axis; on annealing, these excess dislocations will tend to be distributed uniformly along the cross section.¹²

If the above facts are used, the optimal sample orientation would be a bend axis on (111), with the crystal axis (321) and the neutral axis (145). This would yield single glide on (111) and (101), and have the (111) surface available for etching.¹³ This would, unfortunately, require a special grown and prepared crystal.

Working within the confines of standard crystal geometries, there are two alternatives. Considering wafers with an (001) orientation, results in a sample configuration shown in Fig. 36. For this orientation, the (111) and $(\bar{1}\bar{1}\bar{1})$ planes are favorably oriented for slip, with the intersection of these planes, the (110) direction, as the bend axis, giving four sets of mobile 60° dislocations; $a/2$ (101), $a/2$ (011), $a/2$ (011), $a/2$ (101).

There is an alternative crystal geometry with interesting possibilities. A (111) sample cleaved such that the (110) is the bend axis would have the (112) direction intersecting the front sample surface. As the (112) direction is the theoretical direction for formation of low-angle grain boundaries,¹⁴ it may be possible to polygonize such a boundary into the sample. If possible, such an effort will be made.

Various investigations have shown that (111) surfaces formed of Ga atoms dissolve much more slowly in chemical reagents than those composed of As atoms.^{15,16} The difference in behavior can be explained by a simple model.¹⁷ The Ga and As surfaces are formed by ruptures between Ga and As atoms. The electron pair forming this bond passes to the As atom, since it is pentavalent in the free state, and results in a high activity of the As face due to excess electrons. In addition to this specific chemical behavior, the

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dislocations which terminate at the two types of faces have different reactions to etching reagents.¹³

Although the number of dislocations generated in a bent sample can be calculated by Nye's formula,¹⁸ the identification (and counting) of dislocations is less ambiguous if chemical etchant techniques are used. A number of etchants have been devised which distinguish between Ga and As dislocations.^{12,13,19} Since they were developed for optical counting of etch pits, and we intend to use SEM, we will have to experiment to see which produces the most satisfactory results.

There is an additional complication in that different etchants must be used on (111) and (110) faces.¹³ As our sample will have the (110) face perpendicular to the bend axis, we will have to correct our dislocation count for the (111) surface, or alternately, cleave or grind the sample to expose the (111) face.

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4.0 POLYCRYSTAL SOLAR CELL DEVELOPMENT

This task is beginning with development of MS and MIS barrier cells from n-type material. Oxidation processes are under development at several institutions to allow production of the more efficient MIS type cell. Equipment procurement is underway at Howard and Brown which will allow them greater versatility and capacity to produce cells. Actual fabrication of single crystal cells with promising efficiencies has been done, and modeling of polycrystalline cells is underway.

4.1 Plasma Oxidation of GaAs (Brown University)

We have continued the analysis of the oxides obtained on p-type LPE material supplied by Rockwell Science Center. The Auger analysis combined with ion milling has shown, after the proper corrections, a composition very close to Ga_2O_3 and As_2O_3 in the oxide bulk while As accumulates near the surface.

Attempts to obtain MOS devices on n-type MBE material resulted in devices that do not show either inversion or a definite accumulation. The reasons of the different behavior of n-type samples are under investigation.

Some oxides have been grown on n-type bulk material supplied by Howard University and sent back to that institution for analysis. We are attempting to improve the uniformity of the oxide thickness across the area to be oxidized. This is being done with the help of a wire mesh biased at the anode potential and put very close to the surface of the crystal in order to make the oxygen bombardment more uniform.

4.2 Water Vapor Oxidation and Oxide Experiments (Science Center)

Recent experimental work has shown that the presence of a thin oxide layer between the metal and the semiconductor of a Schottky barrier can increase considerably the open circuit voltage, and thus the energy conversion

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efficiency of this type of solar cell. This potential for GaAs MOS type solar cells for both single and polycrystalline materials has been demonstrated at JPL and Southern Methodist University. A wide variety of oxidation techniques was investigated by Stirn and Yeh. It was found that oxide growth at room temperature by exposure to water-vapor saturated oxygen (H_2O/O_2) was most effective with respect to V_{oc} and reproducibility.

During this period, effort has concentrated on constructing a system for water vapor oxidation and oxide experiments. The basic configuration of the wet oxidation setup is shown in Fig. 37. A metering valve is used for controlling the flow rate of oxygen which bubbles through deionized water and passes over the substrate in a glass chamber.

Chromium-doped semi-insulating GaAs single crystal was used as the sample for doing the oxide experiment. The purpose of this experiment was to determine the dependence of oxide thickness and V_{oc} of solar cells on the length of time of oxidation process, flow rate of oxygen, method of surface treatment, as well as the relationship between oxide thickness and V_{oc} .

The first stage of experiment was to fix the flow rate of oxygen and surface treatment method, then measure the oxide thickness by changing the time required for oxidation. So far, we have measured oxide thickness of several samples. The substrates were prepared in hydrochloric acid at room temperature for half an hour, in an attempt to remove the original oxide and contaminants, before being placed in the oxidation chamber. The oxide thickness was measured by using an ellipsometer with a laser beam of $6328\text{\AA}$ in wavelength. This method, however, was complicated by the existence of a native oxide of unknown thickness which existed on the cleaned substrates. Since the ellipsometric technique relies on a very accurate knowledge of the substrate index of refraction, the presence of the native oxide has so far frustrated attempts to obtain accurate oxide thickness.

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Fig. 37 System for water vapor oxidation of GaAs.

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4.3 Fabrication of GaAs Solar Cells (Howard University)

During this quarter, work was performed basically on two solar cell structures, the GaAs single crystal p-n junction cell and the GaAs single crystal metal-insulator-semiconductor (MIS) cell. First, the p-n junction cell will be considered, including relevant process details. Second, the MIS structure will be discussed, which includes several methods of forming the insulation layer. The methods are anodic oxidation, spin-on liquid glass, and thermal oxidation using water saturated oxygen. Third, the photoresponse of the various cells will be examined using a GE tungsten halogen lamp to illuminate the samples. Finally, plans for increasing the efficiency of the various cells in the next quarter will be discussed, with particular emphasis on GaAs polycrystalline MIS structures.

4.3.1 Fabrication of Solar Cells

4.3.1.1 p-n Junction Cell

Preliminary work on GaAs single crystal homojunction (p-n junction) cells was begun by the fabrication of a number of these cells on an in-house grown epitaxial layer. The first step was to grow an n-type epitaxial layer ($T = 1.46 \mu\text{m}$, $N_D - N_A = 1.5 \times 10^{16}$) on a zinc doped p-type substrate ($N_A - N_D = 7 \times 10^{17}$) to form the junctions. Next, $1500\text{\AA}$ of Au/AuGe (12% Ge) dots were E-beam evaporated on the epi surface to form ohmic contacts to the epilayer; the contacts were then sintered at 450°C for 5 minutes in forming gas. Following this step, ohmic contacts to the p-substrate were formed by the evaporation of $1500\text{\AA}$ of Ag-In-Zn metals, and alloying for 30 minutes in forming gas. The substrate was then waxed to a graphite chuck and sawed up into cell chips, with the area of each chip approximately 0.01 cm^2 . A quick etch in 5:1:1 mixture of $\text{H}_2\text{SO}_4:\text{H}_2\text{O}:\text{H}_2\text{O}_2$ to reduce leakage currents at the edges of the cell completed the process. Results of the photoresponse are discussed in a later section.

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4.3.1.2 MIS Cells

A considerable amount of work has been performed during this quarter in examining various techniques for forming metal-insulator-semiconductor (MIS) structures and MIS solar cells. A drawing of the basic MIS cell is seen in Fig. 38. In this structure, the substrate is n^+ GaAs ($N_D - N_A = 10^{17}$), the n-type epilayer is relatively thin, between 1 and 10 μm , the insulator is approximately 20-40 $\text{\AA}$, the metal barrier film is approximately 50-60 $\text{\AA}$, and the contact fingers are between 1.0 and 0.2 μm .

Several different methods of forming the insulator film have been investigated including: 1) anodic oxidation of GaAs using an aqueous solution of ethylene glycol, citric acid and water 2) various spin-on glasses, and 3) thermal oxidation of GaAs. The results of each approach will be discussed in the following section.

4.3.1.3 Anodic Oxidation

Anodic oxides on GaAs were grown on numerous samples in order to optimize and control the anodization process by using an aqueous solution of ethylene glycol. By utilizing an aluminum platform, which contacted most of the bottom of the substrate, it was possible to obtain uniform oxide coverage over the sample with oxide thickness from 300 to 7000 $\text{\AA}$. It was found that the aluminum platform eliminated the non-uniform coverage usually obtained with the aluminum point contact. However, attempts to obtain thinner oxides with thickness below 100 $\text{\AA}$ were unsuccessful. Apparently the current densities needed for very thin anodic oxides are so small that control of the process is difficult, and the resulting oxide film is not uniform. Thus, anodic oxidation does not appear to be a viable method for making MIS cells.

4.3.1.4 Spin-on Oxides

In this approach, a commercially available spin-on (glass) oxide was used to form the insulator. By varying the composition of the product, it was possible to obtain fairly reproducible oxides at both 30 and 60 $\text{\AA}$ thicknesses,

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Fig. 38 Basic structure of a GaAs single crystal MIS solar cell.

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as measured by an ellipsometer. In addition, to determine the degree of coverage of GaAs surface by the oxide, an etch pit experiment was conducted in which one GaAs sample with 60Å of spin-on glass and one unpassivated GaAs sample were immersed in a 1:1 solution of hot H_2SO_4 and deionized water for one minute. At the end of this test, the unpassivated GaAs sample had many etch pits, while the glass passivated surface had a negligible number of pits. Thus, the glass oxide appears to cover the GaAs surface with a uniform layer.

The above results are preliminary and it is premature to predict the usefulness of spun-on oxides in MIS cell fabrication. Work in fabricating cells using this approach is continuing to examine the interface properties and cell performance.

4.3.1.5 Thermal Oxidation

This process involves growing native oxides on GaAs using water saturated oxygen (O_2/H_2O) at room temperature for growth times ranging from 16 to 25 hours. Ellipsometer measurements on oxides grown about 25 hours indicated that the oxide thicknesses were in the 20 to 30Å range. These oxides were grown in a reactor which is not set aside specifically for this purpose.

4.3.2 Solar Cell Fabrication

As mentioned earlier, the oxide is grown on a GaAs single crystal n-type epilayer/ n^+ substrate. First, Au-Ge ohmic contacts are E-beam evaporated on the samples and alloyed for five minutes at 450°C in forming gas. Before starting the oxide growth, the sample is immersed in hot hydrochloric acid (HCl) for five minutes to remove any residual oxide. The acid is displaced with methanol, and the methanol is displaced with propanol. After drying with N_2 gas, the clean sample is placed in the reactor, which has a constant flow of oxygen saturated with water, and the oxide grown for the appropriate time. It must be noted that the native oxide of GaAs is fragile and is attacked by many solutions, including some photoresist developers. This fact

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Fig. 39 Current-voltage characteristics of a homojunction GaAs solar cell under GE 58 tungsten halogen lamps.

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Fig. 40 Current-voltage characteristics of a MIS solar cell on 5.3 μ m GaAs LPE layer under Ge 58 tungsten halogen lamps.

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Fig. 41 Current-voltage characteristics of a MIS solar cell on 2.0 μ m GaAs LPE layer under GE 58 tungsten halogen lamp.

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was observed when an earlier photolithographic process was used to fabricate cells on samples containing the native oxide.

After the oxide growth is terminated, the samples are removed and are given a 50 to 60Å E-beam evaporated Au layer. Au contact fingers of 1500Å are then evaporated through a metal mask. (It must be noted that the metal mask technique eliminated the need for photoresist and its developer.) The isolation of individual cells is begun by coating the top surface with positive photoresist, and drying the resist for 20 minutes at 85°C. Then, using a microscope slide as a straight edge, a narrow line is scribed through the photoresist such that the underlying Au layer is exposed. A saturated solution of potassium iodide (KI_3) is used to etch the thin Au layer between cells, effectively isolating each cell. Finally, the resist is removed using acetone, the sample is dried and then tested.

4.3.3 Solar Cell Test Results

Although a number of cells have been fabricated, this report will detail the results of the best cells produced so far. Results will be given on the light I-V of the one GaAs single crystal homojunction cell and on two GaAs MIS single crystal cells with native oxide grown by thermal oxidation. The light source is a GE58 tungsten halogen lamp with input power in the range of 330 mW/cm².

The light I-V curve for the p-n junction cell is shown in Fig. 39. This small cell has an area of approximately 0.01 cm², with $V_{OC} = 700$ mV, $J_{SC} = 64$ mA/cm², fill factor = 0.71, and efficiency $\eta = 9.6\%$.

Figures 40 and 41 display the light I-V curves for cells made, using Rockwell supplied single crystal epitaxial material. Each cell has an area of approximately 0.023 cm² and experienced the same processing conditions, with the exception that each has a different epilayer thickness. Figure 40 shows the light I-V on a cell which had an epi thickness of 5.3 μm. For this cell,

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$V_{oc} = 620$ mV, $J_{sc} = 83$ mA/cm². FF = .77, and efficiency $\eta = 11.96\%$. The light I-V in Fig. 41 shows that $V_{oc} = 595$ mV, $J_{sc} = 76$ mA/cm², FF = 0.72, and $\eta = 9.7\%$.

The p-n junction cell was the result of a "one shot" attempt at a homojunction device. It is expected that cells with higher efficiencies can be produced relatively easily by this method. Also, since the junction formation of the n-type epilayer on the p-type substrate occurs in the well controlled LPE environment, it is believed that larger area cells up to about 2.25 cm² can be made without due difficulty.

For these cells, several facts concerning substrate selection were learned. First, it was found that cells with epitaxial layers on highly conducting substrates (n-epi on n⁺ substrate) produced better cells than those fabricated solely on highly conducting substrates (n⁺ substrates). The former cells produce open circuit voltages approximately 100 mV higher than the latter. The reason this occurred is because the minority carrier lifetime in epi material is higher than that of n⁺ material. Also, n-n⁺ interface sets up the back surface field so that the carriers are concentrated in the epilayer.

4.4 Modeling of GaAs Photovoltaic Cells (Brown University)

In order to pursue detailed modeling of the polycrystalline GaAs SIS cell, we have found it necessary to examine the role of states localized at the insulator-semiconductor interface. The literature reveals that there are two roles for such states and that properties of GaAs devices can be strongly influenced by their presence. Interface states of particular interest are those which reside within the forbidden bandgap, thus acting as traps and recombination centers. As traps, they cause a fixed amount of charge to be localized, thus raising or lowering the effective barrier height. As recombination centers, they reduce transport through the interface. These states have a second role; they can support tunneling through the insulator. It is, therefore, of particular importance to model these roles adequately.

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The model which was described in the first quarterly technical report now incorporates interface states whose roles are as described above. Recombination is based on SRH statistics with the assumption of independent levels; the interface states communicate much more quickly with the bands than with each other. In addition, an interface state tunnel current is derived which allows the states to exchange carriers with the degenerate semiconductor top contact (in this case, ITO) by tunneling through the insulator. Under particular bias conditions, these states can control the transport properties of the device.²⁰

The characterization of the polycrystalline SIS or MIS GaAs device requires detailed information specific to the particular insulator-semiconductor interface under scrutiny. We have chosen the Ga_2O_3 -GaAs interface as a starting point, although this combination may not be the most suitable for photovoltaic conversion. Other insulators such as As_2O_3 , Sb_2O_3 or $\text{As}_2\text{Ga}_2\text{O}_6$ may offer particular advantages and a study of these insulators is being pursued.

Although electron affinity, bandgap and permittivity also govern transport, the control of interface states appears to be crucial for the production of good devices. This number can be controlled by growth procedure and can vary over several orders of magnitude. One curious aspect is that the clean GaAs (110) surface has no states in the gap.²¹

In order to approach this problem, we have compared the surface state distributions of Zeisse, Mesnick and Lile with those of Shimano, Moritani and Nakai.²² These authors have reported the density of states in the gap as a function of energy for an anodic oxide ($\text{Si}_x\text{O}_y\text{N}_z$). This represents the best information available to us at this time and is characterized by a large peak at mid-gap. We have taken a representative distribution and scaled it down in such a way that the total number of states in a gap is a variable parameter. We have set this number equal to the number

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actually measured in our laboratory,²³ on an MIS device capable of surface inversion ($N_s = 2 \times 10^{12} \text{cm}^{-2}$). Our calculation predicts that such a distribution would result in a surface capable of inversion and that photovoltaic conversion is possible. This is consistent with current MIS solar cell work.²⁴

The accurate description of the insulator-semiconductor interface requires the knowledge of the density of interface states in the gap for the particular insulator and growth conditions. We will be able to continue in this direction when such information becomes available.

4.5 Modeling of Polycrystalline GaAs MIS Solar Cells (Howard University)

In a device such as polycrystalline MIS solar cells, it is difficult to know how to approach the electronic modeling problem. In order to make any headway, the problem of twin boundary will be solved initially. The grain boundaries represent a physical interruption to carrier transport in the semiconductor. The main effect of the grain boundary is to reduce the minority carrier lifetime of the carriers. Surface states at the grain boundary may be produced either by the lattice misfit or by a segregation of impurities. We will treat the surface states near the grain boundary in the same way as in the case of Schottky barrier diodes. The current conduction mechanism through the insulator will be considered tunneling. The tunneling will be described using the independent electron approach of Harrison.²⁵ It will be assumed that the potential barrier near the grain boundary has almost no effect on the "barrier height", which controls the open circuit voltage of the device.

Based on the above simplification, the simple equilibrium energy band diagram for an n-type polycrystalline MIS solar cell is shown in Fig. 42. This is a one-dimensional diagram. Of course, the barrier exists all around the three-dimensional surface of each crystallite, but for

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Fig. 42 Schematic equilibrium energy band diagram of a n-type polycrystalline MIS solar cell.

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discussion of the electron transport properties, it is sufficient to consider only one dimension. The "barrier height" ϕ_n of the device is given by

$$\phi_n = \phi_{mi} - \phi_{si} - V_i - q \left(\frac{Q_s + Q_i}{\epsilon_i} \right) \quad (1)$$

Here, ϕ_{mi} and ϕ_{si} represents the metal to insulator and metal to semiconductor work function and are given by

$$\phi_{mi} = w = x_i \quad (2a)$$

$$\phi_{si} = x_s - x_i \quad (2b)$$

where w is the work function of metal, x_s and x_i are the electron affinities of semiconductor and insulator, respectively. V_i is the potential drop across the insulator of thickness d . The charge stored in the surface states at the semiconductor-insulator interface is represented by Q_s . The fixed charge Q_i in the insulator may be positive or negative depending on the insulator. The dielectric constant of the insulator is represented by ϵ_i .

An inspection of Eq. (1) shows that in order to get maximum open circuit voltage from n-type MIS solar cells, the metal work function should be greater, or at least equal to the sum of the electron affinity and bandgap of the semiconductor. Similar reasoning for p-type MIS solar cells suggests that the metal work function should be smaller or equal to the electron affinity of the semiconductor. The possible metals for n-type GaAs polycrystalline MIS solar cells are Au, Ag, Cu, Pt and Ni. In case of p-type devices, Al, Cr, Ta, Ti and Mg may be used.

The dominant dark current in the device will be tunneling of carriers from the minority carrier band to the metal.²⁶ Depending upon the semiconductor doping, metal work function, and semiconductor-insulator interface parameters, the majority carrier band tunneling current and

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recombination through the interface may increase the dark current. Neglecting the effect of series and shunt resistance, the I-V of the device under illumination may be represented semi-empirically as

$$I = \sum_{i=1}^3 \left[I_{oi} \exp \frac{qv}{n_i kT} - 1 \right] - Q I_L \quad (3)$$

where Q is the collection efficiency depending upon the grain size of the crystallites in addition to other device parameters. I_L is the light generated current, depending upon the number of photons entering the device. As mentioned earlier, the expression for tunneling currents will be used as obtained by using Harrison's approach. The recombination current through the interface will be obtained using an expression similar to one used by Rothwarf²⁷ in heterojunction analysis. The open circuit voltage of the device is obtained by putting $I = 0$ in Eq. (3). This requires numerical solution of the transcendental equation.

$$\sum_{i=1}^3 I_{oi} + A I_L - \sum_{i=1}^3 e^{u_i} = 0 \quad (4)$$

where

$$u_i = \frac{q V_{oc}}{n_i kT} \quad (5)$$

It is expected that native oxides on polycrystalline GaAs may not have full potential as an insulator in the MIS solar cells. The behavior of a device with native oxide of GaAs will be intermediate to that of a true MIS cell and a Schottky barrier solar cell. A number of insulators shown in Table IV may be used for GaAs MIS solar cells. For this reason, we will do initial calculations on Au-SiO_x-(n-type) GaAs. The model will be valid for any combination of metal and semiconductor. The effect of native oxides and

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other oxides with various combination of metals will be considered in detail.

The outline described above will be used to develop a model for polycrystalline GaAs MIS solar cells. These results are in progress and will be reported in the next report.

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5.0 EQUIPMENT PROCUREMENT AND DEVELOPMENT

5.1 Howard University

To support the work of this subcontract, several major systems have been mandated. First, an ion beam coating and milling system has been ordered from Commonwealth Scientific Corporation of Alexandria, Va. The latest delivery date is September 29th. The vendor has had difficulties in purchasing the vacuum station parts.

Orders for a liquid phase epitaxial system have been placed with several vendors. We have received a number of component parts, however, there has been difficulty in obtaining the desired furnace and controller. It is expected that all components of this system will be secured by mid to late September, 1978. Finally, due to reduced funding and large price increases for the equipment referred to above, purchase of the light beam scanner and some materials and supplies is being delayed.

5.2 North Carolina A&T State University

The development of facilities and equipment procurement progress has moved along satisfactorily. In addition to the existing materials growth laboratory, two laboratories (Room 128 and 130 of Cherry Hall) are almost completed. Room 130 (photolithography room) will be used for processing devices and will house the existing E-beam evaporator and the recently ordered neutral ion beam sputtering system. Room 128 will be used for testing and evaluation of optoelectronic devices. This lab will house the data acquisition system to be used for the analysis and display of the experimental results in connection with the HP-1000 computer as well as all other testing equipment such as solar simulator, spectral response apparatus, photoluminescence apparatus, substrate cutting and polishing apparatus, etc.

The following equipment have been received in the last three months: Wire saw (Laser Technology, Inc.), Mazur lapping polishing system,

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power supply for current LPE system, Keithly multimeters, data acquisition equipment (scanner, power supply programmer, CRT terminal, CCI modules, HP xy plotter).

A new current controlled LPE growth apparatus using a heat pipe is about ready to be placed in the materials growth laboratory. It is anticipated that the new system will be ready to grow layers in about 30 to 45 days. This facility will relieve some of the load that is presently placed on the existing CCLPE apparatus.

TABLE IV

Insulator	Band Gap (eV)
SiO_2	8.1
Sb_2O_3	~ 4.2
MgO	7.3
CaO	6-7
Yb_2O_3	~ 5.2
BeO	~ 5.2
Cr_2O_3	~ 4.0
Al_2O_3	$\sim 8-10$

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6.0 PLANNED ACTIVITIES

6.1 Task 1 - Growth of Polycrystalline Material

Major efforts are planned in three growth areas. First, both MBE and LPE (conventional and current controlled) will continue to be used to grow GaAs epilayers on polycrystalline GaAs substrates, to be used in ongoing experiments. These include grain boundary investigations and polycrystal solar cell fabrication. Since polycrystal solar cell fabrication is planned to be a major undertaking during the coming quarter, it is anticipated that large amounts of material will need to be grown and distributed to the various institutions. Development of MBE will continue, aimed at providing material with minority carrier diffusion length closer to values obtained with LPE.

The second major growth task will be to continue experiments with LPE and CCLPE growth of GaAs on metal-coated graphite. A variety of metal coatings will be investigated, and nucleation studied.

The third major growth task will be to return to the study of MBE growth of GaAs on graphite. In particular, studies of crystallite size and nucleation will be made as a function of growth rate, substrate temperature, and doping. Methods of providing ohmic contact to the substrate will be investigated.

6.2 Task 2 - Grain Boundary Investigations

A wide variety of techniques for investigating and characterizing grain boundaries has been utilized so far, and in the coming quarter, will continue to be developed and applied to structures of interest to this program.

For measurements of the characteristics of the epitaxial GaAs layers, transient capacitance lifetime measurements will be attempted on

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polycrystalline LPE and MBE material. SIMS measurement of the oxygen content of MBE material will also be attempted.

More accurate characterization of grain boundaries is anticipated from several experiments. The use of the scanning Auger/cathodoconductivity apparatus on twinned MBE epitaxial layers with a range of doping densities should lead to a model for the potential profile near this type of grain boundary and to the extraction of majority and minority carrier transport parameters in the grain boundary region. The further application of the scanning laser system to polycrystalline material should lead to similar information.

Theoretical work on a dislocation model for GaAs grain boundaries will be done, and attempts will be made to produce GaAs samples with appropriate dislocation structures for experimental studies.

6.3 Task 3 - Polycrystalline Solar Cell Development

A large portion of the total effort during the next quarter will be expended in this task. Solar cells, both MS and MIS, will be prepared on both single crystal and polycrystalline MBE and LPE layers grown on GaAs substrates. By measuring the I-V characteristics, photoresponse, and efficiency at these cells, the fabrication processes will proceed towards the optimum. It is particularly important to develop the oxidation techniques for MIS cells so that high efficiency single crystal cells can be made reproducibly. This will allow comparisons between different types of material for solar cell use.

Modeling of MIS cells and ITO (SIS) cells will continue. As fabrication of actual cells progresses, the interaction between modeling and experiments is expected to increase.

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APPENDIX TO SECTION 3.5
CALCULATION OF VARIOUS FREE ENERGY TERMS ASSOCIATED WITH DISLOCATIONS

The free energy associated with the charging of a dislocation can be written as³

$$F = Nf [E_1 - E_F + E_S(f) + \delta F_S(f)] \quad (1.1)$$

where N is the number of dangling bonds on the core, f is the occupational probability, E_1 the neutrality level, E_F the Fermi level, and E_S the total electrostatic energy of the space charge cylinder around the dislocation core

$$E_S = f \epsilon_0 [3/2 \ln(f/f_c) - .866] \quad (1.2)$$

In the above expression

$$\epsilon_0 = \left(\frac{1.321}{C \times 10^8} \right) \text{ev} \quad \text{and} \quad f_c = C (N_D)^{1/3} \quad (1.3)$$

where C is the distance between dangling bonds in centimeters,

$$C = \frac{b \sin 60^\circ}{\sin \alpha} \quad (1.4)$$

" b " is the Burger's vector and α is the angle between the slip direction and the Burger's vector. For 60° dislocations, which are assumed here, $c = b = 4.00 \times 10^{-8}$ cm.

In deriving Eq. (1.2) a uniform distribution of charge on the dislocation core was assumed. However, due to the overlap of the wave functions of adjacent dangling bond, movement along the core is possible giving rise to a non-uniformity term in the free energy for $T > 0$.

$$\delta F_S = \delta E_S - TS \quad (1.5)$$

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In the Einstein approximation, where each electron is assumed to move in the average field of all of the other electrons, such that the maximum displacement is small enough that the restoring forces are still linear, one has

$$\delta F_S = \delta E_S - TS = (\bar{n} + 1/2) h\nu - TS \quad (1.6)$$

where

$$\bar{n} = \frac{1}{e^{\frac{h\nu}{kT}} - 1} \quad (1.7)$$

$$h\nu = f^{3/2} \sqrt{9.60 b_1 \epsilon_0} \quad (1.8)$$

$$S = K [(1 + \bar{n}) \ln (1 + \bar{n}) - \bar{n} \ln \bar{n}] \quad (1.9)$$

and b_1 is the broadening parameter. In the tight binding approximation, the energy broadening is given by

$$E(k) = E_1 - 2b_1 \cos(kc) \quad (1.10)$$

where $kC = \frac{m\pi}{NC}$, $m = 0, 1, 2, \dots, N-1$

Minimizing F with respect to f gives the equilibrium value

$$f = - \frac{E_1 - E_F + E_S + \delta E_S - TS}{\frac{\partial}{\partial f} (E_S + \delta E_S - TS)} \quad (1.11)$$

the only remaining term to be defined is E_F . The Fermi level is found from the charge neutrality condition,

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$$p + N_D^+ = n + N_A^- \quad (1.12)$$

For an n-type semiconductor with parallel edge dislocations with an area density, N_S ,

$$p + N_D \left[\frac{1}{1 + 2e^{\frac{E_F - E_D}{RT}}} + \frac{N_S \pi R^2}{1 - N_S \pi R^2} \right] = n + \frac{N_S (f/c)}{1 - N_S \pi R^2} \quad (1.13)$$

where

$$p = N_V e^{\frac{(E_V - E_F)}{KT}} \quad \text{and} \quad n = N_C e^{\frac{(E_F - E_C)}{KT}}$$

with

$$N_V = 7.0 \times 10^{18} \text{ cm}^{-3} \quad \text{and} \quad N_C = 4.7 \times 10^{17} \text{ cm}^{-3}$$

It is seen from Eq.(1.13) that the Fermi level is little effected by the dislocations if either the area density of dislocations N_S is small or the space charge radius of each dislocation is small. In the numerical calculations carried out, at least one of the conditions is assumed to be met. Equations (1.11) and (1.13) were solved self-consistently using phlegmatic numerical methods.

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