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Theoretical Models of Efficiency for Polycrystalline Thin Film Solar Cells

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Quarterly Progress Report No. 1

September 1, 1979 - January 31, 1980

March 1980

INSTITUTE OF ENERGY CONVERSION
UNIVERSITY OF DELAWARE
NEWARK, DELAWARE 19711

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1. Abstract

The literature on Schottky and MIS diodes has been thoroughly reviewed. Underlying the accepted theoretical models for MIS devices we have identified a major weakness in the handling of current flow through the insulating layer. An alternate model, presently only partially developed quantitatively is presented.

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3. Introduction

The literature on Schottky diodes, metal insulator semiconductor (MIS) diodes and solar cells based upon these is quite extensive. A major task of this program is to critically evaluate the mechanisms which have been proposed to explain Schottky and MIS solar cell behavior to determine which mechanisms may apply to Zn_3P_2 solar cells. In the course of this study we have considered the proposed mechanisms that lead to high open circuit voltage (V_{OC}) with little or no loss in short circuit current (j_{SC}) and fill factor (FF). While interface charging and voltage drops across the insulating layer enter into various models, the key question in all the models is how the carriers pass through the insulator. Several authors have attempted to model the current flow through the insulator as a tunneling process. Others have avoided the issue by assuming that carriers can move freely through the insulator. They then make various assumptions about the pinning of the Fermi level or the equilibrium of the interface states i.e. the interface states are in equilibrium with 1) the metal 2) the majority carriers of the semiconductor 3) the minority carriers of the semiconductors. While models that neglect details of the transport of carriers through the insulator are useful for determining what properties could be attained if the various assumptions were true, they provide little insight as to how these conditions can be brought about. In order to have impact on actual devices the mechanism determining carrier flow through the insulator must be understood. We have accordingly concentrated our efforts on this aspect of the models. We find that the accepted picture of tunneling is not supported by the data.

4. Current Flow in Schottky and MIS Diodes

Figure 1 shows the band picture for a p-type MIS solar cell. The expression for the diode current is given by

$$j = A^* T^2 \exp[-\phi_{BP}/kT] \exp[-\chi_V^{\frac{1}{2}} \delta] [\exp(qV_S/kT) - 1] \quad (1)$$

where A^* is the Richardson constant for holes ($A^* = 120(m^*h/m_0) \text{ amp/cm}^2\text{K}^2$) and V_S the voltage drop across the semiconductor, with V the voltage across the cell, given by $V = V_S + V_i$, where V_i is the voltage drop across the insulator. In the limit that $\delta \rightarrow 0$ Eq. (1) is the expression for an ideal Schottky diode. We note that the tunneling factor $\exp[-\chi_V^{\frac{1}{2}} \delta]$, with χ in eV and δ in Å, simply reduces the current by a numerical factor from the Schottky value. While Eq. (1) is a plausible model for current transport across the insulator the experimental results indicate a current inconsistent with the values of χ_V and χ_C expected for the insulators used (χ_V and χ_C are the interfacial barrier heights below the valence band and above the conduction band respectively). Card and Rhoderick⁽¹⁾ in considering SiO_2 on Si find that although $\chi = 3.15$ eV for bulk SiO_2 , to fit the data to the model χ must be assumed to vary with δ , the thickness of the oxide. The variation of χ with δ is such that in the range of δ over which the short circuit current is observed not to decrease significantly (up to ~ 20 Å), χ remains below 0.25 eV. Card and Rhoderick offer two explanations for this discrepancy. First they argue that for a layer which is on the order of 10 atomic layers or less one should not expect to define a band structure in a conventional sense. Second they argue that if a potential barrier can be defined it will not be constant over the entire contact area.

Studies of superlattices⁽²⁾ suggest that nearly bulk band structure is attained within a few atomic layers. Hence the argument that failure to reach bulk properties accounts for the low $\chi_V^{\frac{1}{2}} \delta$ values has no strong theoretical or experimental basis. If this were so it would also mean that theoretical expressions were of little use unless $\chi_V^{\frac{1}{2}}$ vs δ could be determined by some means other than fitting the current voltage curves.

The second argument that the barrier height is not uniform is reasonable, in that layers less than 100 Å thick generally have "pinholes" or discontinuities which in the case of the usual fabrication of MIS devices would be filled with metal as the metal is deposited on the insulating layer. The metal semiconductor contacts at such regions would be true Schottky diodes. If we assume that the χ_V and χ_C values are near their bulk values for the insulator, then all the diode-current would be carried by flow through the "pinhole" Schottky regions until the pinhole density fell to nearly zero. Based upon such a picture one recovers Eq. (1) but with the factor $\exp -\chi_V^{\frac{1}{2}} \delta$ replaced by (A_p/A) , where A_p is the area of pinholes and A the total area of the junction. The empirical variation of $\chi_V^{\frac{1}{2}} \delta$ with δ is then a manifestation of the decreasing density of pinholes with insulator thickness. The insulator simply reduces the contact area through which current can flow.

5. Qualitative Features of the Pinhole Model of MIS Diodes

Based upon the analysis indicated in Section II the most likely current mechanism for flow through the interface appears to be Schottky contacts at pinholes in the insulating layer. The consequences of this picture can be given qualitatively:

1) Since the area of Schottky contact is reduced the total current through a given area for a given voltage is reduced.

2) For a solar cell if the short circuit current were undiminished from the Schottky value (see below) then the lower diode current cited in (1) would yield a higher open circuit voltage by $\Delta V_{oc} = \frac{kT}{q} \ln A/A_p$.

3) The short circuit current should not be reduced even when the diode current is substantially reduced due to a fundamental asymmetry between majority and minority current flow. This asymmetry can be seen easily in Figure 1. Majority carriers (holes) which reach the barrier in a region other than a pinhole will be reflected back from the insulator into the bulk semiconductor and this retreat is aided by the direction of the electric field i.e. the majority carriers are moving up hill and when they are reflected by the insulator barrier they go back down the hill. The minority carriers (electrons) on the other hand, after being reflected by the insulator are maintained by the field near the barrier until they diffuse to a pinhole and reach the metal i.e. the minority carrier is moving down hill and after reflection from the insulator cannot make it up the hill again and accumulate at the bottom eventually finding their way to a pinhole. If the density of pinholes becomes too low the current will no longer be

capable of being carried without the density of minority carriers reaching such high values that they begin to diffuse back into the bulk semiconductor where they recombine. An estimate of the ratio (A_p/A) at which j_{sc} should begin to diminish is obtained by noting that the minority current crossing the metal semiconductor contact is $j_{minority} \approx q \frac{v_{th}}{4} n_j$ where v_{th} is thermal velocity and n_j the density of minority carriers at the pinhole. For undiminished short circuit current flow over the whole device area the condition is:

$$j_{sc} = q \frac{v_{th}}{4} n_j \frac{A_p}{A}$$

The short circuit current is due to diffusion from the bulk and is given by:

$$j_{sc} \approx q \frac{L}{\tau} n_{bulk}$$

Hence

$$n_j = \frac{4}{v_{th}} \frac{L}{\tau} n_{bulk}$$

Since n_j is supplied by diffusion from regions around the pinhole and these in turn by diffusion from the bulk (aided by the space charge field) at some point minority carriers from the region around pinhole will begin to diffuse back to the bulk rather than to the pinhole or the space charge will become so large as to repel additional carriers. A rough estimate of when this should occur is $n_j = n_{bulk}$ or

$$\frac{A_p}{A} = \frac{4}{v_{th}} \frac{L_n}{n} = \frac{4}{v_{th}} \left(\frac{kT}{q} \frac{\mu_n}{\tau_n} \right)^{\frac{1}{2}}$$

For p-Si with $L_n \approx 2 \times 10^{-2}$ cm $\tau_n = 2 \times 10^{-5}$ sec and $v_{th} = 10^7$ cm/sec,

$A_p/A \approx 4 \times 10^{-4}$, $\Delta V_{oc} = 0.20$ V while for n-Si with $L_p = 2 \times 10^{-4}$, $\tau_p = 10^{-8}$ sec,

$v_{th} \approx 10^7$ cm/sec, $A_p/A \approx 8 \times 10^{-3}$, $\Delta V_{oc} = 0.125$ V. These increases are in the range observed in MIS solar cells at the value of δ at which j_{sc} begins to decrease. (3)

4) Since the variation in pinhole area with the thickness of the insulator will depend on how the insulator is formed, the sensitivity of V_{oc} to oxide formation technique in MIS structures is readily accounted for.

6. Conclusions and Discussion

Previously Green⁽⁴⁾ had considered the effects of pinholes on the series resistance of MIS solar cells, and very recently Rajkanan, Singh, and Shewchun⁽⁵⁾ have included pinholes in the treatment of the thickness variation of V_{oc} . In neither case do they treat the details of how the current crosses the insulator. They do not address the conditions leading to optimal solar cell efficiency nor do they seem to appreciate the fact that the pinhole density and area completely dominate the MIS behavior.

Based upon the outlined pinhole model that we report here it appears to be possible to produce a reliable easily controlled MIS device by growing a thick insulating layer (50 - 500 Å) with essentially no natural pinholes and then deliberately introducing through the layer Schottky contacts of the optimal density and area to achieve high efficiency solar cell behavior.

The previous theories of MIS solar cell behavior which relied upon uniform insulating layers and tunneling through such layers appear to be inappropriate for actual devices. They also invoke many assumptions (interface states, charging of the insulating layer) which may not have any real effect on the solar cell efficiency.

7. REFERENCES

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Equilibrium electron band diagram for p-MIS cell.

Figure 1