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DEVELOPMENT OF A COMPARATIVE ANALYZER FOR
MICROPROCESSOR

By E. J. Rolfe

Published October 1978

Topical Report

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E. J. Rolfe, Project Leader

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CONTENTS

Section	Page
SUMMARY.	5
DISCUSSION	6
SCOPE AND PURPOSE.	6
PRIOR WORK	6
ACTIVITY	6
ACCOMPLISHMENTS.	12
FUTURE WORK.	16
DISTRIBUTION	17

ILLUSTRATIONS

Figure		Page
1	Comparative Microprocessor Fault Detector Diagram.	7
2	Fault Detection Circuitry.	9
3	Fault Display.	10
4	Fetch Cycle Counter.	12
5	Possible Combinations of Machine Cycle Timing	13
6	Technique of Machine Cycle Synchronization . .	13
7	Synchronization Circuit.	14
8	CMFD and UUT With Simulated Failure.	15
9	Comparative Microprocessor Fault Detector. . .	15

TABLE

Number		Page
1	Monitor Points	8

SUMMARY

Development of a microprocessor-based production item demonstrated the need for an efficient method of in-circuit processor troubleshooting. The complex operation of a microprocessor does not lend itself to conventional troubleshooting techniques. Commercial microprocessor analyzers are available but usually require a highly-trained operator. The Comparative Microprocessor Fault Detector (CMFD) that was developed consists of a reference processor, comparators, and a fault display. The reference processor executes an identical program, is operated from the same time base, and receives the same input data as the microprocessor under test. The two processors are synchronized by circuitry in the CMFD. Each signal from the processor under test is continually monitored and compared to the respective signal of the reference unit. The comparators are designed to ignore small differences caused by such things as different rise times or propagation delays. When the first deviation is detected, the CMFD stores the current state of both processors and displays the data on LED indicators. Displaying a complete set of reference and test data makes it easy to identify the failure mode.

Operation of the CMFD is simple. It has only two switches: reset and AC power. Two 40-pin test clips are used to make all connections to the processor under test. The design simplifies setup.

The CMFD has successfully detected and displayed simulated faults. All tests indicate that it is a useful troubleshooting tool. It has significant advantages over the presently available commercial analyzers because the CMFD locates a fault in one operation without requiring the operator to have special digital skills.

DISCUSSION

SCOPE AND PURPOSE

The need for a simple method of detecting microprocessor faults prompted the development of the Comparative Microprocessor Fault Detector (CMFD). The concept of the CMFD consists of comparing the performance of a microprocessor under tests to a reference microprocessor system (Figure 1).

A CMFD was developed to support troubleshooting of an electronic programmer that is a microprocessor-based product using a two-chip F8 processor. The two-chip system consists of a Central Processing Unit (CPU) and a Program Storage Unit (PSU). Unique troubleshooting techniques are required with the F8 processor because the two-chip system does not have an address bus or single step capability.

PRIOR WORK

There are several commercial microprocessor analyzers available, but all require a considerable amount of knowledge about hardware and software to be used effectively. In many cases, this required knowledge makes them unsuitable for use by production personnel in a manufacturing environment. The commercial analyzers have many sophisticated capabilities, but do not have the capability to directly locate a deviation from normal operation. Therefore, the operator must have special skills to locate where a fault occurs, and it may require that the product be exercised many times before the fault is located. This repetition is especially cumbersome if a problem is intermittent.

ACTIVITY

The Comparative Microprocessor Fault Detector (CMFD) is a compact tester that checks the F8 microprocessor in a Unit Under Test (UUT) by comparing it to an internal reference processor executing an identical program. Both processors are operated from the oscillator and external interrupt timer of the UUT. Both receive the same input data; therefore, they should be simultaneously executing the same operations. The signals which are monitored and compared are listed in Table 1.

The CMFD captures the state of both processors when the first deviation is detected. It is important to have information about the first fault because, after a fault, the processor under

Figure 1. Comparative Microprocessor Fault Detector Diagram

Table 1. Monitor Points

Microprocessor Signals Compared	Number of Lines
ROMC	5
Input/Output Ports	18
Data Bus	8
WRITE	1

test may completely diverge from the normal program sequence. Once a processor has deviated from the proper operating sequence, it may begin executing meaningless operations. For this reason, it is essential for failure analysis to know where the first fault occurred.

The comparison circuitry is shown in Figure 2. CD4049 inverters are used to buffer signals. A SN7486 EXCLUSIVE-OR gate is used to make each comparison. The comparison circuit was designed to ignore small differences between the signal caused by slightly different rise times or propagation delays. The circuitry which eliminates these false error indications consists of an RC low-pass filter on the input of a SN7414 Schmitt Trigger. The RC time constant is $2.7 \mu\text{s}$; however, the actual delay is shorter because the $0.003 \mu\text{f}$ capacitor is precharged by I_{IL} of the SN7414. Therefore, this circuit ignores differences (outputs of the SN7486) which are less than $1 \mu\text{s}$ in duration. The clock period of the UUT is $3 \mu\text{s}$. Differences which last for less than $1/3$ of a clock cycle are ignored.

When the first deviation is detected, an ERROR signal is generated to clock the SN7474 latches which store the current state of both processors. As shown in Figure 3, the LED indicators on the front panel display the state. The reference unit indicators (REF) display what the processor should have been doing when the error occurred. The TEST indicators display what the unit under test actually executed. The differences can be easily observed.

If no deviations are detected, no error signal is generated indicating that the microprocessor being tested is not defective. The CMFD will continue to compare the processors until the test is stopped by removing power from the UUT.

Figure 2. Fault Detection Circuitry

Figure 3. Fault Display

The CMFD contains a 3853 Static Memory Interface (SMI). The SMI chip interprets the ROMC lines and data bus into a 16-bit address. This address is used to drive four hexadecimal displays. When an error is detected these displays are latched, storing the address at which the error occurred.

Another feature of the CMFD is the Fetch Cycle Counter. When all five ROMC lines are low, the microprocessor is executing an instruction fetch. Circuitry was designed to detect this state and count how often it occurs. The circuit in Figure 4 counts each fetch cycle until a deviation is detected and ERROR goes low giving additional failure analysis information.

The major difficulty encountered in the development of this analyzer was the synchronization of the processors. Upon application of power, the two processors do not always start with their machine cycles synchronized. This condition can be detected by observing that the WRITE signals are not synchronized. Figure 5 shows the four possible timing relationships. Simultaneously applying an external reset signal to both CPUs does not correct the differences between the machine cycles. Therefore, a circuit was developed to double clock the reference CPU until the processors are synchronized. Figures 6 and 7 show the technique and the circuitry used for this synchronization. Two SN74121 mono-stable multivibrators are used to introduce extra clock pulses at the appropriate times. The SN74121 which is triggered by EXT CLK, generates a 500 ns wide pulse on the positive transition of EXT CLK. This pulse is used as a delay. If the other SN74121 is enabled by the presence of a WRITE signal difference, then it generates a 500 ns pulse which is used to separate one of the EXT CLK pulses into two pulses.

The synchronization correction is accomplished within three machine cycles and is complete before the UUT receives an external reset signal. Therefore, the external reset (EXT RES) signal is used to enable the error detection circuitry.

Figure 8 shows the tester connected to a microprocessor-based product. A clip-lead was installed on the product to introduce a defect by grounding bit-2 of I/O port "5". When the product was exercised with the CMFD attached, a deviation was detected. The display panel shows that the error occurred on I/O port "5" bit-2. The difference occurred the first time the processor under test attempted to set bit-2 to a high state. It should be noted that at this time the data bus (DB) contains the complement of the desired state of I/O port "5". The rest of the indicators show that all of the other bits were still synchronized.

Figure 3 shows another example of a fault detection. In this case, the program stored in the PSU of the UUT differed slightly from the reference. The first deviation occurred when the data lines differed as shown. This difference was detected on the 56th fetch cycle when the processor was executing at address 127₁₆. This corresponds exactly to the first difference between the programs.

ACCOMPLISHMENTS

The Comparative Microprocessor Fault Detector has been successfully constructed and tested. It has consistently detected simulated failures which were introduced in a sample unit and accurately displayed the nature of these errors. As a result of this work, a CMFD will be used to support MC3152 Electronic Programmer troubleshooting and failure analysis.

The design allows easy setup and simple operation. Figure 9 shows that the only controls are the AC power switch and a reset button. The two 40-pin test-clips simplify connection to the processor under test. Using the CMFD, a fault can be located in one operation without special skills. The simple and reliable operation of this fault detector will allow efficient troubleshooting of microprocessor-based products.

This CMFD can be easily adapted to any other F8-based product by simply inserting a PSU which contains the appropriate program.

Figure 4. Fetch Cycle Counter

Figure 5. Possible Combinations of Machine Cycle Timing

Figure 6. Technique of Machine Cycle Synchronization

Figure 7. Synchronization Circuit

Figure 8. CMFD and UUT With Simulated Failure

Figure 9. Comparative Microprocessor Fault Detector

Also, the comparative technique can be extended to other microprocessor systems.

FUTURE WORK

The comparative technique presented in this report is not limited to use with a two-chip F8 system. This concept could be applied to more complex F8 systems and to other types of processors. The control, data, and address lines of other microprocessors would be compared to an appropriate reference unit. Systems which already have an address bus available would simplify the comparator by eliminating the need for an SMI. To monitor systems which operate at other clock frequencies, the time constant of the delay circuits would have to be changed.

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