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THE TRIGGER SUPERVISOR: MANAGING TRIGGERING CONDITIONS IN A HIGH ENERGY PHYSICS EXPERIMENT

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Abstract

We describe a trigger supervisor, implemented in VMEbus hardware, which enables the host computer to dynamically control and monitor the trigger configuration for acquiring data from multiple detector partitions in a complex experiment.

Introduction

Experiment E802 at BNL will study the complex spectra of particles produced in nucleus-nucleus interactions. The detector hardware required for this study is comprised of several detector subsystems (for tracking, particle identification, calorimetry, etc.) referred to as partitions.

Each of the detector partitions may contribute to the first-level trigger which initiates gating and digitization of some 5000 measurement parameters for each event. The trigger logic for up to 16 partitions is collected into one system, the Trigger Supervisor, which enables the host computer to dynamically control and monitor the trigger configuration for the experiment.

The Supervisor consists of a control module and 16 partition modules in one triple-high VMEbus crate. An arbitration module and crate interconnect module in the same crate make the Supervisor a resource available to the master VME crate, providing communication with the host and the crate readout controllers handling the front end electronics for the partitions. The Supervisor's design keeps the insertion time down to approximately 50 nsec.

Functions provided by the Trigger Supervisor include the following:

- Provision for coupled (on beam spill) and uncoupled (off-spill calibration, debug, test) modes of operation for each of the 16 partitions. Coupled partitions share a common dead time, and uncoupled partitions have independent dead times to allow for independent data streams. A first-level trigger from any coupled partition generates gates for all coupled partitions.
- Eight components in the first-level trigger from each partition; each may be individually enabled or disabled. Each trigger component may be prescaled by factors ranging from 1 to 2^{24}.
- Generation of gates/starts for front-end ADCs, TDCs, latches, etc.
- Interrupt generation for crate readout controllers.
- Record provided of pattern of trigger components present in the first-level trigger.
- A transaction counter, updated by accepted trigger, may be used to assure integrity of events assembled from multiple fragments.
- Second-level trigger (veto) logic is provided, including generation of fast clears for ADCs, TDCs, with no computer overhead. Veto survival is provided for rare trigger components.
- In a given partition, the relative delay between the interaction trigger and the gates generated for the front end electronics is constant to within 1 nsec independent of which partition initiated the first-level trigger.
- Diagnostic features are included: computer readout of all control registers including prescale factors and a computer test mode to verify the correct operation of all aspects of the Supervisor's operation.

The paper describes the implementation of these functions, and highlights the more unusual design features.

While the Trigger Supervisor has been designed to serve the needs of a specific experiment, the generality and flexibility it provides make it potentially useful in other experiments involving complex detector systems.

Functional Details

The Trigger Supervisor's principal role is to use selected first-level trigger inputs, prescaled if desired, to generate gates for a partition's ADCs and TDCs, subject to appropriate busy logic. This operation takes place in a manner which differs depending on whether the partition is coupled or uncoupled. A coupled partition's gates are generated whenever a trigger input is accepted from any coupled partition; in other words, all coupled partitions always generate gates for the same events. Gates are generated for an uncoupled partition

only when one of its trigger inputs is accepted. Busy logic is treated differently in the two cases as well: uncoupled partitions have independent busy latches, which may be reset by the microprocessor whenever its front-end electronics has been read out. The busy latch for a coupled partition is set synchronously with those of the other coupled partitions, and only cleared when data for all coupled partitions has been read out.

Each partition module provides for eight independent trigger inputs. Each input is independently enabled/disabled under computer control. If the partition is not busy, the enabled input is subjected to prescaling. Prescaling factors from 1 to 2^{24} are possible.

A second role of the Trigger Supervisor is to provide for second-level vetoes. This is accomplished by providing a veto input on each partition module. In effect, a partition may withdraw its first-level trigger decision at any time up to 1 μsec following the trigger by issuing a veto. If an event is characterized, at this second-level decision time, by having no outstanding triggers, fast clears are issued to the front-end electronics, and the busy logic is reset at the appropriate time.

Any trigger component may be designated as a "Veto Survivor"; the occurrence of such a trigger overrides any second-level veto decision. This provision guarantees that rare events, e.g., beam events scaled down by 10^6, are not discarded because, for example, a desired multiplicity threshold was not exceeded.

A global veto is also provided. Intended to be used to discard events which have been corrupted by post-pileup, it generates the fast clear sequence regardless of the existence of Veto Survivors.

Implementation

The Trigger Supervisor, consisting of the control module and up to 16 partition modules, is housed in a triple-high (9U) VME crate. An arbitration module and crate interconnect complete the crate configuration. On each module, the P1 backplane connector is devoted to VMEbus signals; the center row of the P2 connector is reserved for VME signals (not used here). The remaining rows of P2 are used for control signals between the control module and the partition modules.

The Trigger Supervisor logic is implemented partly in ECL-10KH in order to achieve an insertion time (interaction trigger in to gates out) of $\approx$50 nsec, and partly in LSTTL to achieve greater packing density and functionality and to keep the overall power dissipation within reason.

In the following paragraphs, we limit the discussion to coupled partitions. An interaction trigger (assumed to be present for every event in coupled mode) is subjected to standardization (Figure 1) in order to guarantee that the LSTTL devices in the partition module behave correctly. Standardized pulses have widths of 50 nsec and are separated by a minimum of 125 nsec. A system busy synchronizer functions as the busy latch for the coupled partitions and, further, insures that the release of BUSY does not result in a truncated pulse. The output of the synchronizer is the EVENT STROBE, which is used to time the gates generated by the partition modules.

Figure 2 traces the progress of a trigger component on the partition module "X" to the point of a first-level trigger decision. Each trigger input consists of a two-fold ECL AND, where one of the inputs is optional. If absent, this second input defaults to TRUE. The second level of gating requires an enable level (computer enable) and the EVENT STROBE described earlier. Prescaling, handled in the third level of gating, is implemented out-of-line in order to avoid excessive insertion time. The prescaler increments on the trailing edge of each trigger; when it overflows, the logic accepts the following trigger, and presets the scaler in preparation for another scale-down sequence. Eight such trigger components are wire-ORed to form the "X FIRST LEVEL".

This signal is wire-ORed on the P2 backplane (Figure 3) with similar signals from other coupled partitions to form "SYSTEM FIRST-LEVEL". This signal is used by the Control module to set SYSTEM BUSY. A 10H102 receiver on the partition board produces "X/SYSTEM FIRST-LEVEL", which is logically identical

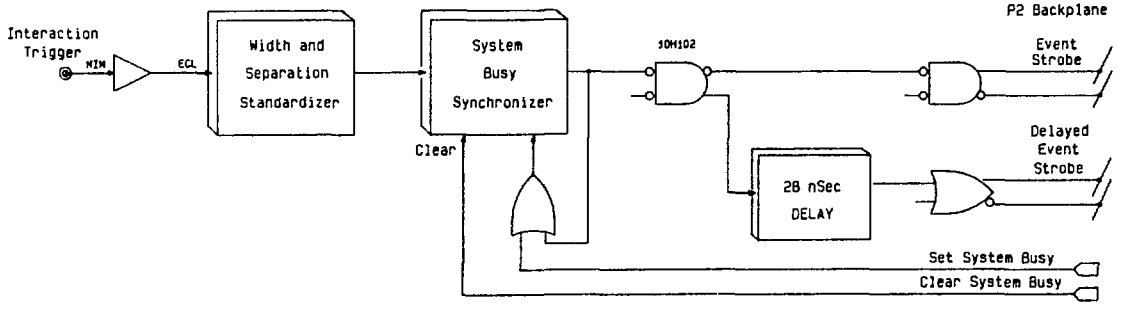

Fig. 1: Control module event strobe generation

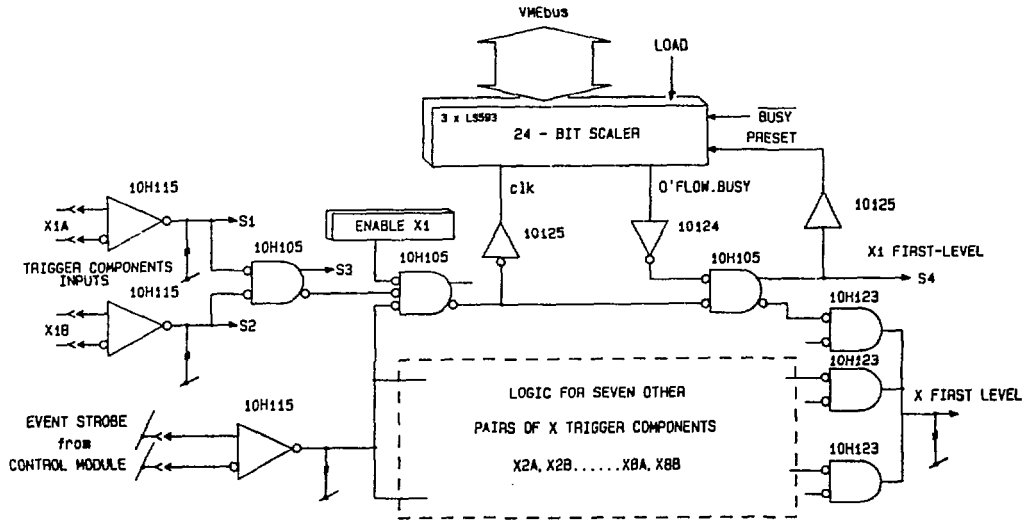

Fig. 2: Generation of X first-level decision in the partition X module

to the backplane signal for the case of a coupled partition. This signal is used to generate the output gates for the X partition, using DELAYED EVENT STROBE distributed via the backplane to time the gates. DELAYED EVENT STROBE, used in this way, guarantees that the start of the gates at the output of any partition board varies not more than 1 nsec, independent of which trigger component initiated the event.

The details of the second-level veto are shown in Figure 4. The X VOTE latch is set by the rising edge of X FIRST-LEVEL. The partition veto logic can clear this latch at any later time. X VOTE is wire-ORed on the backplane with votes from other coupled partitions to form SYSTEM VOTE. One μsec after X/SYSTEM FIRST-LEVEL, SYSTEM VOTE is clocked into a set of latches which initiate the fast clear sequence or initiate the interrupts to the microprocessors (distributed via front panel outputs), depending on whether any votes are outstanding at this time.

Partition veto is supplied by a front panel input, X VETO, which is disabled whenever a trigger component labelled as a veto survivor has contributed to X FIRST LEVEL.

Great care has been taken in the implementation of the ECL wired-OR signals SYSTEM FIRST-LEVEL and SYSTEM VOTE developed and distributed on the backplane. Terminations at each end of the bus and Schottky diode clamps on the partition modules help achieve generally clean signals. In addition, the logic which uses these signals is designed to be insensitive to the trailing-edge glitches which result from the asynchronous release of the OR-bus by the participating drivers.

Computer Access to Supervisor functions

Sixteen-bit registers on the Control module include the Coupled register, which determines which partitions are coupled, the Busy register, which allows microprocessors to determine which partitions are involved in an event, the Event Counter, a transaction counter for events involving coupled partitions, and Set-Clear Select, which serves as a mask for operations on the Busy register. There is also a Function byte which is used to set and clear selected busy bits.

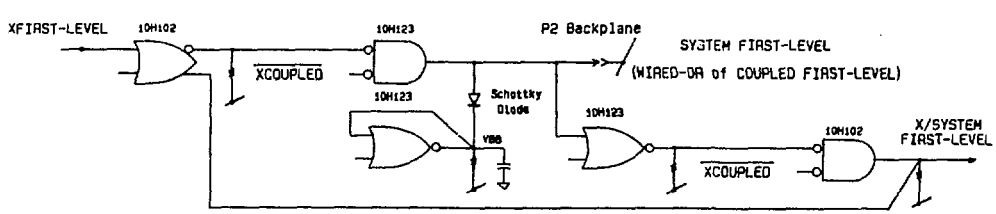

Fig. 3: System first-level decision generation by the partition X module

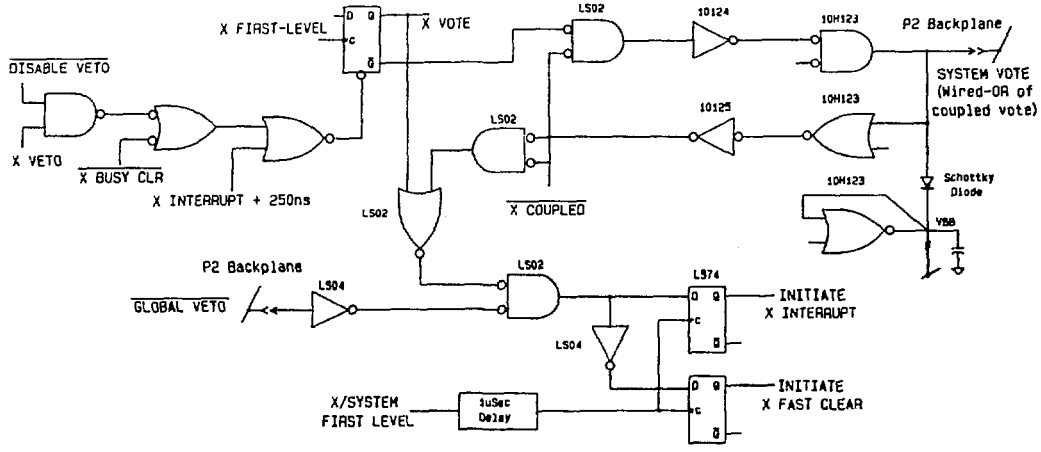

Fig. 4: Second-level veto logic in partition X

On the Partition modules, several 8-bit registers allow Enable and Veto Override to be set, and a transaction counter and trigger pattern register to be read. A Pulse register generates simulated triggers in all enabled components. Finally, the 24-bit prescalers may be read and written.

The Trigger Supervisor occupies 1024 bytes of short addressing space, and responds to both supervisor and user address modifiers. All functions may be addressed as bytes; additionally, 16-bit registers may be addressed as words.

Address lines A05..A08 are used to define the partition board being selected. Hardware on the partition board compares these address lines with a 4 bit geographical address encoded in the P2 backplane. This comparison is only valid when accompanied by one of two partition enable signals generated by the address decoding logic on the control module. One of these is the SCALER SELECT signal which defines the access to the prescaler subspace of the partition address space. The PARTITION SELECT signal defines access to the miscellaneous (non-scaler) functions on the partition boards.

Summary and Status

A system has been described which allows the management of triggering conditions in an experiment where many detector subsystems are invlolved. The system is presently under construction, and is expected to be used in the experiment this Fall.

Acknowledgment

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