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Design, Fabrication, and Performance of a 20 Percent Efficient Silicon Solar Cell

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DESIGN, FABRICATION, AND PERFORMANCE OF A
20 PERCENT EFFICIENT SILICON SOLAR CELL

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A B S T R A C T

A single-crystal concentrator $p^{+}nn^{+}$ silicon solar cell with maximum efficiency greater than 20 percent at 27°C is described. The intrinsic cell design has been used with several metallization patterns targeted for different system designs in the ten to several hundred suns concentration range. The design and fabrication of the intrinsic cell is specified. Performance data for the best cells of three metal patterns with the intrinsic cell are presented and discussed.

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DESIGN, FABRICATION, AND PERFORMANCE OF A 20 PERCENT EFFICIENT SILICON SOLAR CELL

Introduction

During the past five years three different types of silicon solar cells have been designed and fabricated at Sandia National Laboratories. The first, an n^+p cell typical of devices used for space applications, exhibited a maximum energy-conversion efficiency of 15 percent.¹ This cell was manufactured in small quantities by Sandia and used in the construction of a 1 kW array. A problem with this design was its low-current collection, which was attributed to minority carrier lifetime degradation during processing.

In order to increase the cell current, a second design, the p^+nn^+ back-surface-field (BSF) cell, was fabricated using a high (10 ohm-cm) base resistivity, n-type substrate. This change was very successful in that a substantial current increase was realized, and the maximum efficiency increased to above 18 percent under concentrated sunlight.² The improvement was primarily the result of the longer lifetime of the higher resistivity substrates and maintaining this lifetime during processing.

It is interesting to note that 18 percent cells were fabricated in industry during the same period of time, but the cell type was n^+p of the same general structure as the original Sandia cell. A higher performance level was achieved in this case by lower temperature, higher-quality processing than used at Sandia.

The third type of Sandia cell is basically the same as the BSF but with lower base resistivity (0.3 ohm-cm). This cell loses some current relative to the BSF structure but more than compensates for this loss with increased open-circuit voltage and fill-factor.

This report will discuss the design considerations and fabrication process which have developed single-crystal silicon solar cells of greater than 20 percent conversion efficiency under concentrated sunlight at 27°C. Performance data are presented and the important parameters are discussed.

Cell Design

The intrinsic solar cell design is a p^+nn^+ structure fabricated using gaseous source diffusions into an n-type, 0.3 ohm-cm, float-zone, single-crystal silicon substrate. The work reported here is a continuation of the earlier efforts to maximize the conversion efficiency of this structure. Parametric studies have effected the design of a processing sequence which has demonstrated 20 percent efficient solar cells at 27°C. Parameters which have,

been investigated using experimental parametric studies and numerical device codes are substrate doping, p^+ and n^+ diffusions, front surface passivation, and front electrode pattern design.

Substrate Doping

Through parametric studies the effect of the resistivity of the starting material on efficiency was investigated. It is well known that there is a trade-off between open-circuit voltage and short-circuit current as the substrate doping is varied. Several experimental runs indicated that the most consistent, as well as best results, could be obtained using 0.3 ohm-cm material.

The Sandia device code, which was developed as part of the silicon solar cell program, subsequently predicted a small advantage for the 0.3 ohm-cm cell. More importantly, however, the code shows that the BSF structure is more sensitive to process variations, which invariably occur, than the 0.3 ohm-cm cell. That a higher yield of high-efficiency 0.3 ohm-cm cells is observed is evidence of the validity of this analysis.

The wafers used are mechanically and chemically polished, commercially available, single-crystal silicon of (100) orientation from Monsanto. These wafers are 2-inch diameter, float-zone grown (which generally has a higher lifetime than Cz material), 12 mils thick, and n-type phosphorous doped.

P⁺ and N⁺ Diffusions

The formation of the p⁺ and n⁺ layers is a critical step affecting the eventual performance of the intrinsic device. The depth of the front surface p⁺n junction must be shallow to ensure good UV spectral response, while the top layer's sheet resistivity must be kept low to keep spreading resistance effects to a minimum. These requirements conflict since sheet resistivity is inversely proportional to junction depth; i.e., as the diffused layer thickness is decreased, sheet resistivity increases. A junction depth of 0.35 microns and a sheet resistivity of 50 ohms/square are compatible and ensure good, short-wavelength spectral response and high overall energy-conversion efficiency of the cell. The n⁺ diffusion in the back surface guarantees good ohmic contact to the back surface, and its formation will also getter heavy metal impurities inadvertently introduced during processing. It has been found that a 1000°C, 30-minute diffusion for both layers meets the above criteria.

Electrode Pattern Design

Several different contact pattern designs have been used with the intrinsic cell design discussed in the previous sections. In each pattern there is a trade-off between the amount of shadowing and the series resistance which can be tolerated in the electrodes. Decreasing the metal coverage increases I_{sc} but also increases the I^2R losses in the electrodes and diffused layers, while increasing the metal coverage decreases I^2R losses but also decreases I_{sc} .

The optimum metal pattern will also depend on the insolation for which the cells are designed and the cell size, which may be determined by the system application, i.e., point focus, line focus, etc.

In this program, three metal patterns have been examined, as shown in Figure 1. The S08 pattern is a double buss-bar configuration for use in line-focus systems with effective active area of .81 sq cm. It has been the test vehicle for a number of parametric studies which led to an effective processing sequence. The performance for this cell peaks at about 60-80 suns. The S13 design has a single buss-bar encircling the active area with grid fingers perpendicular to the buss at each edge. Its active area is 4.2 sq cm and is targeted for a point-focus, fresnel lens system at 30-suns concentration. This pattern was designed using a code which considers sheet resistance, shadowing, and grid resistance losses.³ The S10 pattern was designed for less than 10 suns insolation in a dye concentrator system, has a single buss-bar, and an active area of .963 sq cm.⁴

The electrode metal used is an evaporated titanium-palladium-silver trimetal. The titanium layer is ~ 500 Å thick and provides adhesion and ohmic contact to the silicon. The palladium middle layer is also 500 Å thick and acts as a corrosion inhibitor and a diffusion barrier against silver. The thickness of the initial two-micron-thick evaporated silver layer is increased by electroplating silver after fabrication to provide the conductivity required for the electrode to carry the design current loads.

The use of the intrinsic cell design with the S08 and S13 electrode patterns has resulted in silicon solar cells with demonstrated conversion efficiencies of 20 percent at 27°C for concentrator systems. This is the highest efficiency that has been achieved in silicon to date. The S10 pattern produced a cell with a one-sun, energy-conversion efficiency above 18 percent, which is also the highest one-sun efficiency to date.

SANDIA NATIONAL LABORATORIES

SILICON PHOTOVOLTAIC CELLS

S13 PATTERN

S08 PATTERN

S10 PATTERN

Figure 1

Cell Fabrication Process

Conventional integrated circuit processing technology is used to implement the cell design. The processing sequence is listed in Table 1 and is illustrated in Figure 2. First, a detergent scrub and acid clean are done to ensure a clean surface. A dry oxide is then grown on the front surface prior to CVD oxide deposition. This acts to prevent dislocations and strain-induced surface defects caused by the CVD masking oxide.

The back nn^+ junction is then formed by solid-state diffusion of phosphorous using phosphine with oxygen as the gaseous source with nitrogen as a carrier gas. This predeposition is done at 1000°C for 30 minutes and provides a highly-doped surface to ensure good ohmic contact. A junction depth of approximately 1.0 microns is obtained with a sheet resistivity of 5-10 ohms/square. After the excess phosphorous glass is etched away, the active cell area is photolithographically defined.

TABLE 1
Cell Processing Sequence

Step	Description
1	Wafer double scrub, acid ($\text{H}_2\text{SO}_4\text{-H}_2\text{O}_2$ 7:3) clean, HF dip ($\text{H}_2\text{O-HF}$ 10:1).
2	Front oxides: dry SiO_2 ($\sim 300 \text{ \AA}$), CVD SiO_2 ($\sim 10 \text{ k\AA}$).
3	Phosphorous predeposition diffusion (phosphine 1000°C , 30 m).
4	Phosphorous glass etch (BHF).
5	Photolith. Step to define p^+ well.
6	SiO_2 etch (BHF).
7	Photoresist strip, wafer scrub, acid clean, HF dip.
8	Silox oxide deposition on back ($\sim 5 \text{ k\AA}$).
9	Boron predeposition diffusion (Diborane 1000°C , 30 m).
10	FB acid etch, steam oxide (850°C , 20 m), FB acid etch.
11	Dry SiO_2 ($\sim 100 \text{ \AA}$).
12	FG anneal (N_2 w/10% H_2 , 450°C , 20 m).
13	Plasma deposited (300°C) SiN_x AR coat ($680 \text{ \AA}$) on front.
14	Photolith. Step to open front contact windows.
15	Nitride etch (phosphoric acid at 160°C), SiO_2 etch (10:1 $\text{H}_2\text{O-HF}$).
16	Photoresist strip, wafer scrub, acid clean, HF dip.
17	Titanium ($500 \text{ \AA}$), palladium ($500 \text{ \AA}$), and silver (2 microns) front evaporations.
18	Photolith. Step to define metal electrode pattern.
19	Silver etch (H_2O_2 , NH_4OH , H_2O).
20	Palladium (HNO_3 , HCL , H_2O at 60°C) and titanium (H_2SO_4 and H_2O at 120°C) etches.
21	+ Photoresist front, SiO_2 etch (BHF) backs.
22	Photoresist strip.
23	Titanium ($500 \text{ \AA}$), palladium ($500 \text{ \AA}$), and silver (2 microns) back evaporations.

SCHEMATIC ILLUSTRATION OF BSF STRAWMAN AND DYE CELLS PROCESS FABRICATION SEQUENCE

1. FRONT SURFACE PASSIVATION AND N+ DIFFUSION OXIDE MASK

2. N+ PHOSPHOROUS DIFFUSION AND GETTERING

3. PLANAR PATTERN

4. SILOX BACK TO MASK AGAINST BORON DIFFUSION

FIGURE 2

5. P+ BORON DIFFUSION

6. FRONT DRY OXIDE PASSIVATION & FORMING GAS ANNEAL

7. PLASMA NITRIDE AR COAT

8. OPEN CONTACT PATTERN

FIGURE 2 (Continued)

9. EVAPORATE FRONT METAL

10. DEFINE METAL PATTERN

11. PROTECT FRONT & ETCH SILOX OFF BACK

12. EVAPORATE BACK METAL

FIGURE 2 (Continued)

Windows are opened in the masking oxide by etching with buffered hydrofluoric (BHF) acid, and after photoresist removal, a layer of Silox is applied to the back to mask against the boron diffusion. A boron diffusion is done at 1000°C for 30 minutes using diborane and oxygen as the gaseous source with nitrogen as the carrier gas, forming an active $p^{+}n$ junction near the illuminated front surface. This p^{+} emitter has a sheet resistivity of about 30-50 ohms/square and a junction depth of $\sim 0.3\text{-}0.4$ microns. The boron concentration at the surface is about $1 \times 10^{20} \text{ cm}^{-3}$. Boron glass formed at the surface during the predeposition is removed by a fluoroboric acid etch, oxidation, and fluoroboric acid etch sequence. A thin dry oxide which acts as a surface passivation layer is grown and annealed in forming gas (10 percent hydrogen in nitrogen) as specified in Table 1.

The AR coating is a low temperature ($\sim 300^{\circ}\text{C}$), plasma-assisted CVD nitride layer approximately $670 \text{ \AA}$ thick with a refractive index of ~ 2.05 . With the dry passivation oxide, this layer thickness has been optimized to reduce surface reflectance over the usable solar spectrum.⁵

Contact windows are defined and opened using boiling phosphoric acid in a reflux unit to etch through the nitride, and a quick (30 seconds) 10:1 HF dip to etch through the thin oxide. The photoresist is stripped off, the wafers are cleaned, and then titanium, palladium, and silver are evaporated sequentially on the fronts. The metal pattern is defined photolithographically and the metals are

sequentially etched to form the desired electrode pattern. Positive photoresist is used to protect the fronts while the Silox masking layer is etched off the back and, after cleaning, the same trimetal system is evaporated onto the wafer back.

Finally, the front metal is electroplated to 10 microns for the S13 pattern and 8 microns for the S08 pattern. During electroplating the grid lines mushroom out, increasing the shadowing losses to a maximum of 8.2 percent and 12.0 percent for the S13 and S08 designs, respectively. After one-sun screening on the wafer, the cells are separated from the wafer by laser scribing. This technique introduces less edge damage than dye separation using a diamond saw.

Performance Data

Performance data were obtained using a Fresnel lens concentrator in Albuquerque sunlight. One sun current calibration was obtained under collimation with a NASA reference cell to determine irradiance. To determine the concentration, the short circuit current of the cell under test was assumed linear with irradiance.

The performance data under concentrated sunlight for the S08 cell design is shown in Figure 3. The total active cell area of the front surface, excluding buss-bars, was used to calculate the energy-conversion efficiency. The energy-conversion efficiency peaks above 20 percent at 27°C at about 60-suns insolation. It should be noted that the efficiency stays above 18 percent out to 300-suns

insolation. The open-circuit voltage increases ~ 60 mV per decade from 10 to 100 suns indicating a diode factor of ~ 1 . A major factor contributing to the high performance of this cell is the excellent fill-factor. Figure 3 shows that the fill-factor stays above .80 up to 100 suns.

For the S13 design the cell area is taken as that inside the large buss-bars. The efficiency shown in Figure 4 peaks above 20 percent at 27°C at about 30 suns. The open-circuit voltage also increases ~ 60 mV per decade from 10 to 100 suns for a diode factor of ~ 1 . Here the fill-factor stays above .80 only out to 50 suns. The one-sun and concentration performance data for both S08 and S13 are summarized in Table 2.

Several conclusions can be drawn from these performance figures. First, the fact that the current-collection efficiency is so high indicates long lifetimes in these cells. Therefore, the processing does not significantly degrade the lifetimes, and lifetimes may actually be improved due to the gettering action of the phosphorous diffusion. Second, the high open-circuit voltages are indicative of low-leakage currents. This is a result of adequate front surface passivation and maintaining high lifetimes in the base of the cell.

A further indication of the excellent performance of the intrinsic cell is given by the efficiency of a cell with a metal pattern designed specifically for less than 10-suns operation. Using the S10 electrode pattern, one-sun efficiencies above 18 percent have

been reached. Note that the one-sun current is significantly higher, since shadowing loss is lower in this design (3 percent) than in the S08 and S13 design. This data is included in Table 2.

Figure 3. S08 Metal Pattern Cell:
 V_{OC} , FF and γ vs Concentration

Figure 4. S13 Metal Pattern Cell:
 V_{OC} , FF and η vs Concentration

TABLE 2

Summary of Solar Cell Performance

(T = 27°C, AM1.0 Spectra)

Insolation	V _{OC} (V)	Fill-Factor	η (%)
S08		J _{SC} @ 1 sun = 32.5 mA/cm ²	
1	.641	.83	17.2
10	.700	.84	18.9
60	.747	.84	20.2
100	.759	.82	19.9
500	.794	.68	17.4
S13		J _{SC} @ 1 sun = 33.32 mA/cm ²	
1	.643	.83	17.8
10	.703	.84	19.6
30	.730	.83	20.2
100	.761	.74	18.9
500	.771	.70	17.9
S10		J _{SC} @ 1 sun = 34.4 mA/cm ²	
1	.640	.83	18.1

Summary

The cell design and fabrication process which has led to conversion efficiencies above 18 percent at one sun and above 20 percent under concentrated sunlight at 27°C have been presented. Two different metal patterns used resulted in cells above 20 percent energy-conversion efficiency indicating the versatility of the intrinsic cell design for use in various concentrating systems.

Further improvements can be made to increase the energy-conversion efficiency of the silicon solar cells made at Sandia. First, the use of textured front surfaces with a quarter-wavelength AR coating can possibly improve the current collection efficiency up to 10 percent. Also, double-layer AR coatings of Al_2O_3 and TiO_2 are being studied. Second, the use of thick photoresists to define very straight-walled metal lines will improve the conductivity of the metal electrodes without increasing shadowing losses. Work in both of these areas is proceeding at present with the expectation of improving the maximum energy-conversion efficiencies to about 22 percent.

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