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SOLID-STATE PROCESSES TO PRODUCE HEMISPHERICAL
COMPONENTS FOR INERTIAL FUSION TARGETS

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Abstract

The designs proposed for next-generation targets and components for inertial fusion (IF) involve complex multilayer, multishell configurations. Solid-state process technology offers a wide assortment of fabrication techniques useful in the realization of such structures. This paper presents several such processes which are capable of producing freestanding hemishells of a variety of materials.

INTRODUCTION

Many of the target designs proposed for the next generation of Inertial Fusion (IF) experiments and for IF reactor fuel pellets involve a spherical fuel container surrounded by multicomponent, multilayered concentric spherical shells. The various layers and shells are designed to enhance the response of the target to irradiation from a high energy laser or other driver. One approach to realizing these complex structures is to assemble hemispherical components (hemishells). The dimensions of the hemishells are small (i.e., $<500\text{ }\mu\text{m}$ diameter) and the surface and uniformity criteria are very stringent for the currently proposed targets, especially for laser fusion targets.

Techniques to manufacture hemishells such as molding, stamping or machining are not suitable as conventionally practiced. Hemispherical components have been produced by micromachining methods but the technique is inherently time consuming, labor intensive and costly. Yields are also low due to the difficulty of matching two hemishells for assembly. Other fabrication techniques are thus being pursued.⁽¹⁻⁴⁾

One promising approach which we are developing is to apply semiconductor process technologies to the fabrication of IF targets and components. Solid-state processing techniques are attractive since they offer a design and fabrication flexibility which results from the wide assortment of processes available. Developed for the semiconductor industry, these processes are generally batch, lend themselves to automation, and have proven cost-effective in high-volume production. In addition, the technology base is extensive and sufficiently developed to permit the fabrication of a variety of microstructures with a high degree of precision and reproducibility.

This paper first reviews the basic semiconductor processes which have already been demonstrated for the production of hemishells.⁽¹⁻³⁾ The efforts to extend these basic methods to the production of free-standing hemishells of materials other than silicon by employing additional solid-state processes are then described.

BASIC HEMISHELL PROCESSES

The semiconductor processes basic to the production of hemispherical components have already been described.⁽¹⁻³⁾ The main aspects of the hemishell fabrication sequence involve forming a hemispherical cavity in a silicon wafer, forming the hemishell wall, and then freeing the hemishell from the supporting wafer matrix. The key step in the production of the hemishells is the formation of high-quality hemispherical cavities in the silicon wafer using batch photolithography and isotropic etching. Etch mask patterns are defined photolithographically through a mask consisting of successive layers of thermally grown silicon dioxide, chromium and gold. The cavities are formed with an isotropic etchant composed of hydrofluoric and nitric acids. If desired, a self-aligned flange can be added to the structure by deliberately undercutting the oxide layer prior to the metal mask removal. The hydrofluoric acid concentration and the velocity of the etchant normal to the surface must be controlled to achieve uniform, reproducible cavities. Surfaces free of features at 10,000X by SEM are obtained for the appropriate conditions.

Once a high quality hemispherical cavity is formed, fabrication of a hemishell can proceed in either of two ways. In the first approach, the cavity wall is modified so that it is retained following dissolution of the supporting wafer. Doping silicon with high levels of boron

renders it insoluble in the anisotropic silicon etchant, ethylene diamine/pyrocatechol/water. The etch rate for this etchant drops to near zero for boron levels which exceed $5 \times 10^{19} \text{ cm}^{-3}$ (about 0.1% boron in the silicon lattice).⁽⁵⁾

When the undoped portion of the silicon wafer is dissolved, free-standing hemishells of single crystal silicon remain. The quality of the hemishell depends upon the etching and diffusion procedures employed. Hemishells are being produced where both the inner and outer surfaces are featureless within the resolution of the SEM at 10,000X. Figure 1 shows two silicon hemishells. The larger hemishell is about 1000 μm in diameter. The wall thickness of both hemishells is 1 μm .

The cavity wall can also be modified by thermal oxidation to form silicon dioxide (SiO_2). The etch rate for SiO_2 , in a similar anisotropic etchant, is less than 4 $\text{\AA}/\text{minute}$ compared to about 10,000 $\text{\AA}/\text{minute}$ for silicon. When the silicon is dissolved, an array of transparent SiO_2 hemishells remains. Wall thicknesses of 5 μm are readily achieved. The surfaces appear featureless and should be as good as or better than the original cavity surfaces. Since silicon oxidizes by the diffusion of oxygen through the oxide, the cavity surface becomes the interior of the hemishell. And, since about 60% of the SiO_2 wall thickness comes from the oxygen atoms, a leveling effect is expected. Figure 2 shows an array of SiO_2 hemishells. These arrays are being used in the development of laser characterization techniques and for the experimental verification of the behavior of double shell cryogenic targets.⁽⁶⁾

In the second approach, the cavities in the silicon wafer are used as a primary or secondary mold. The desired shell materials or materials are deposited on the cavity surface. The wafer mold is then removed destructively or nondestructively freeing the hemishells or arrays.

NEW HEMISHELL PROCESSES

From current target designs the components desired for IF targets will not be made of silicon or useable in the form of arrays or sheets. Thus processes are required which are capable of producing freestanding components of a variety of materials. An additional photolithography step can be used to realize freestanding hemishells. However, such an approach requires accurate alignment and flanged hemishells. Also as the hemishell walls become thicker ($>5 \mu\text{m}$), the required masking and etching procedures become increasingly more difficult to perform. The fabrication schemes to be discussed avoid these problems and produce freestanding configurations directly.

Freestanding SiO_2 Hemishells by Selective Oxidation

A process to produce freestanding hemishells of SiO_2 is illustrated in Figure 3. This scheme relies on several of the basic hemishell processes already described and, in addition, uses a selective oxidation technique.

The process begins with the chemical vapor deposition of a thin ($\sim 0.2 \mu\text{m}$) layer of silicon nitride (Si_3N_4) onto the surface of a silicon wafer. Successive layers of chromium, gold and photoresist are then applied as a mask. Photolithographic patterning occurs by wet chemical etching of the chromium and gold and by plasma etching of the Si_3N_4 .

The hemispherical cavity is formed in the same manner as in the basic hemishell process. If a self-aligned flange is desired on the hemishell, the Si_3N_4 can be undercut. The metallic mask is then removed and the silicon oxidized to SiO_2 . Silicon nitride blocks the diffusion of oxygen to the silicon surface and thus confines the oxide growth to the exposed silicon surfaces. The SiO_2 hemishells are freed from the silicon wafer by anisotropic etchants which dissolve the silicon preferentially as in the basic hemishell process. Figure 4 shows some freestanding SiO_2 hemishells produced by this process.

Freestanding Metal Hemishells by Selective Deposition and Lift Off

Metal hemishells can be realized by a variety of deposition techniques for a variety of metals. The most promising approach for thick wall hemishells involves plating. While the proper plating conditions must be determined empirically, surfaces can be bright with grain sizes less than $200 \text{ \AA}$.

Figure 5 shows a process which produces freestanding metal hemishells. As in all the hemishell schemes, the process begins with the formation of a hemispherical cavity by isotropic etching of the silicon through an appropriate mask. Either a nitride or an oxide mask can be used. After the cavity is formed, a metal flash is evaporated onto the wafer substrate. This flash is then stripped from the flat surface with tape or by a lithographic lift off process. Since the silicon is electrically conductive and the oxide or nitride is insulating, the substrate can be biased to cause plating to occur selectively in the hemispherical cavity. The resulting metal hemishells are then lifted from the silicon mold.

The mating surface of the hemishell can be lapped smooth prior to its removal from the silicon wafer if the edge quality is not adequate for a gas-tight seal. Figure 6 shows a freestanding gold hemishell made by the scheme illustrated in Figure 5.

Freestanding Hemishells With Thick Walls by a Back Filling Technique

For some applications it is desirable to produce hemishells with walls considerably thicker than achievable with the fabrication schemes previously described. For walls less than 10 μm in thickness, thermal oxidation, chemical vapor deposition, and plating can be used to obtain walls having the required thickness, uniformity, and surface finish. For very thick walls 10 to 200 μm , these techniques are not appropriate.

Figure 7 shows one fabrication scheme to produce thick walled hemishells. The process begins with the formation of a hemispherical cavity as previously described. Now, however, instead of selective oxidation, the silicon or selective deposition of a metal, the cavity is back filled with the desired hemishell material such as a metal, glass or compound. The back filled material is then polished down to the nitride "break" layer and a second masking layer is deposited. A hemispherical cavity is then formed in the back filled material in the same manner as the cavities were produced in the silicon (i.e., photolithographic pattern definition and isotropic etching). This approach is being evaluated using glass and lead as the backfill materials.

CONCLUSION

Several methods utilizing semiconductor processing techniques have been demonstrated to be useful for the production of freestanding hemishells of a variety of materials. The processes illustrate the considerable range and versatility of these solid-state fabrication techniques and the design possibilities they provide to the IF target area. Refinement of these processes and extensive characterization of the hemishells they produce are underway.

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FIGURE CAPTIONS

1. Freestanding silicon hemishells fabricated using precision etching technologies. The larger hemishell is 1 mm in diameter. The smaller hemishells has a flange of about 5 μm . The wall thickness for both is 1 μm .
2. Array of SiO_2 hemishells produced by oxidation. The wall thickness is about 5 μm .
3. Fabrication scheme to make freestanding SiO_2 hemishells.
4. Freestanding SiO_2 hemishells. The diameters and wall thicknesses are 300 μm and 1.5 μm , respectively.
5. Fabrication scheme to make freestanding metal hemishells.
6. Freestanding gold hemishell. The diameter and wall thickness are about 350 μm and 4 μm , respectively.
7. Fabrication scheme to produce freestanding hemishells with thick walls (>10 μm).