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1. ABSTRACT

Attempts have been continued to increase the short circuit current in cells of enhanced open circuit voltage. Both deposition of copper on the surface of the Cu_2S layer and hydrogen plasma treatments have been attempted. To date, no significant increase in ultimate current has been achieved. Various changes in cell production procedure have been made with significant improvements in reproducibility. Improvements in the structure of $(\text{CdZn})\text{S}$ layers and resulting cell properties have been achieved using modified substrates based on NiFe . Improvements have been made to the capacitance measuring systems with a consequent gain in resolution, accuracy and reproducibility. Structural studies of the electron beam deposited glass have revealed the presence of cracking and experiments have been carried out to determine the optimum deposition conditions for producing defect-free coatings.

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3. INTRODUCTION

The basic parameter limiting the conversion efficiency of the CdS/Cu₂S solar cell is the short circuit current. It has so far proved impossible to achieve the current levels of the standard solution reaction cell with the planar junction cell that shows an approximately 8% higher open circuit voltage. During this quarter, experiments were made to improve the short circuit current by the Bogus⁽¹⁾ treatments of depositing a thin layer of copper on the Cu₂S or by treating the Cu₂S layer in hydrogen plasma. Neither technique has been found to result in a short circuit current that is higher than would be anticipated using our more conventional heat treatments. It is concluded that the Cu₂S layers produced by standard procedures at IEC are not copper deficient and therefore, cannot benefit from the Bogus-type treatments.

Improvements in reproducibility have been achieved by reverting to a single layer antireflection coating and by a number of housekeeping changes in the standard cell production line.

Further studies of the deposition (CdZn)S layers are reported as are the results of some in depth structural studies. Progress is reported on the production of voltage stable cells using expansion matching substrate of NiFe.

Some instrument modification has been made to the capacitance measuring system to improve resolution and reproducibility. Problems achieving uniform

illumination of cells during capacitance testing have been eliminated. Temperature capability has been extended to cover the range from 77 to 300 K. Preliminary results on the influence of temperature on light and dark capacitance are reported.

Further studies of the structure of electron beam deposited glass layers are reported and the significant effect of the substrate temperature during deposition.

4. Cell Production Analysis and Testing

4.1 CdS/Cu₂S Solar Cells

A major thrust this quarter has been to improve the reliability and reproductibility of the various cell formation processes. It was found that scheduling to minimize time delays between the various steps substantially improved yield and performance. Reverting to a single layer AR was found to improve performance and repeatability. Attempts to enhance the short circuit current by glow discharge in hydrogen or by depositing extra copper are reported.

4.1.2 Phase 2 Maximize J_{sc} by Cu₂S Control

Bogus and Mattes⁽¹⁾ reported improved cell performance by either depositing a thin film of copper (30 - 100 $\text{\AA}$) on the Cu₂S layer or by treating the cell in a hydrogen plasma. Experiments have been carried out using both of these approaches to determine whether the short circuit current of the solid state Cu₂S cells can be increased. Experiments on cells made using the solution reaction revealed that adding extra copper does not result in a net improvement in cell performance. Parallel treated and untreated cells

were made on substrates #21111, 21112, 21113 and 21114 with the results shown in Table 1.

Table 1

CdS/Cu₂S Performance Figures.

Cell #	max (%)	J _L (max) (mA/cm ²)	V _{oc} (V)	Cu ₂ S (Å)
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Performance of Standard Evaluation Process cells (SEP) without
Additional Copper

21113-11-2	8.98	23.77	.5276	3128
21114-11-4	8.82	24.11	.5198	2330
21114-11-2	8.72	24.46	.5226	2330
21113-11-4	8.30	23.98	.5279	3128
21111-11-4	8.01	21.50	.5238	3446
21112-11-4	7.90	21.57	.5179	3184
21112-11-2	7.28	20.62	.5074	3184
21111-11-2	4.56	22.05	-	3446

Performance of SEP cells with 50 Å⁰ of copper

21113-11-3	7.95	23.97	.5130	3128
21112-11-3	7.59	22.89	.5207	3184
21113-11-1	7.52	23.52	.5090	3128
21111-11-3	7.15	20.34	.5186	3446
21114-11-3	6.88	21.42	.5128	2330
21114-11-1	6.73	20.92	.5140	2330

The beneficial effect of adding copper reported by Bogus⁽¹⁾ is believed to be due to enhancement of the Cu_2S stoichiometry. It is concluded from the experiments on SEP cells that these cells are able to achieve the optimum stoichiometry without additional copper. Accordingly experiments were conducted on cells with solid state Cu_2S which have as yet failed to match the SEP cell in current generating capacity.

Cell #21035.212 was made by the solid state process with $2170 \text{ \AA}^{\text{O}}$ of Cu_2S . After protracted heat treatment (250 hours $130\text{--}170^\circ\text{C}$) the maximum J_L at 100 mW/cm^2 was 19.0 mA/cm^2 without AR. Following deposition of $50 \text{ \AA}^{\text{O}}$ of copper and heat treatments of 64 hours at 120°C in H_2 and 5 minutes in air at 150°C the J_L had risen to 19.8 mA/cm^2 . Further treatment at 170°C in H_2 for 16 hours increased this to 21.3 mA/cm^2 but with some instability in the I-V. Similar results were recorded for cells #21035.211 and 21066.214.

Experiments with $100 \text{ \AA}^{\text{O}}$ of Cu were totally unsuccessful. Further experiments are planned and will be reported next quarter.

A basic difficulty with optimizing the Cu_2S stoichiometry by reducing heat treatments is that there are simultaneous effects on the compensated regions of the CdS. In an attempt to separate these two effects some preliminary experiments have been carried out on the use of H_2 plasmas to reduce the Cu_2S . This also has a potential of significantly reducing the time taken to optimize cells using this procedure. Tests have been carried out in both RF (radio frequency) and DC (direct current) discharges.

In general cells in both H₂ and H₂/Ar plasmas showed a collapsed I-V indicative of excessively resistive Cu₂S. Subsequent treatment by either elevated temperature exposure to air or an O₂ plasma treatment caused reversion to a square I-V curve with a value of J_L higher than that prior to the H₂ plasma treatment. However, in no case was the J_L higher than would have been anticipated by conventional reducing heat treatment. Typical cell parameters at various stages of these treatments are given in Table 2.

Table 2
Influence of H₂ Plasma Treatment on Cell Performance.

Cell #	<u>V_{oc}</u> (Volts)	<u>J_{sc}</u> (mA/cm ²)	<u>FF</u> (%)	<u>Comments</u>
21002.114	0.520	13.02	72.8	Initial
	0.210	2.34	-	RF plasma, H ₂ , 6 min.
	0.502	16.15	63.9	170°C Air, 1.5 hour
20932.123	0.495	8.98	72.2	Initial
	0.116	2.58	28.5	RF plasma, H ₂ , 1 hour
	0.505	13.27	63.1	170°C Air, 1.5 hour
	0.500	12.63	73.2	Air storage, 42 days
21067.112	0.492	12.27	69.0	Initial
	0.259	4.97	32.8	DC plasma, H ₂ , 30 seconds
	0.485	11.88	59.5	22°C Air, 3 days
21067.113	0.492	12.31	65.3	Initial
	0.158	1.07	27.7	DC plasma, H ₂ , 1 minute
	0.484	9.16	61.2	150°C Air, 30 second

As was anticipated, plasma control using RF excitation was more convenient and reliable than with DC discharges. The latter are of course subject to significant spacial variations. Work in the literature⁽²⁾ also suggests that DC plasmas may not be as effective as RF in reducing surfaces.

Further work to optimize the plasma reduction of Cu_2S was not judged appropriate at this time. Systematic work would require constructing special equipment and in the absence of indications of noticeably enhanced J_L this was not deemed worthwhile. It is noted that there is a potential for significantly reducing the amount of time necessary to optimize cell performance using plasma reduction and this may become of importance in the development of commercial production technology.

4.1.3 Phase 3 - Optimize V_{oc} , FF for J_{sc} Greater than 26 mA/cm²

In the previous quarterly report a description was given of the deposition of the two layer $\text{TiO}_x/\text{SiO}_2$ anti-reflection coatings. During this quarter some difficulties were experienced in reproducible two layer AR coatings and on a number of occasions excessive loss of short circuit current was noted immediately after the AR deposition. Accordingly the efficacy of a single layer Ta_2O_5 was explored and it was shown that the optical effects of this layer were equivalent to the two layer AR. Furthermore, the deposition process is shorter and more straightforward and under appropriate control virtually no loss of current was observed immediately following the AR deposition. The Ta_2O_5 is electron beam evaporated from a crucible containing the source powder. To avoid oxidation of the Cu_2S layer during the process the vacuum

system is pre-pumped to 2×10^{-5} Torr, back filled with N_2 and re-pumped to better than 7.5×10^{-6} Torr. During the evaporation the pressure rises to about 7.5×10^{-5} Torr but quickly recovers to better than 10^{-6} Torr. Table 3 shows a comparison between single and double layer AR cells made during February. The higher reproducibility of the single layer process is very evident.

Figure 1 shows a direct comparison between cells made on substrate #2.1106. The figure shows clearly that a marked reduction in J_L has occurred on application of the double layer AR (cells 1 and 3) which subsequent heat treatment will recover but generally at the expense of fill factor. Table 3 shows that the ultimate efficiency achieved by cells 2 and 4 exceed that shown by cells 1 and 3.

SINGLE AND DOUBLE LAYER ANTI-REFLECTION COATINGS

Figure 1

Influence of single layer Ta₂O₅ and double layer TiO_x/SiO₂ anti-reflection coatings on cell performance.

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Table 3

Comparison of Single and Double Layer AR for Cells Made During February 1980

<u>Cell #</u>	<u>Date Made</u>	<u>Max. η (%)</u>	<u>J_L (mA/cm²)*</u>
<u>Single Layer Ta₂O₅</u>			
21105-11-4	2-12-80	8.85	23.17
21110-11-2	2-14-80	8.75	23.06
21106-11-2	2-14-80	8.61	23.40
21106-11-4	2-14-80	8.57	22.81
21109-11-2	2-14-80	8.53	23.81
21108-11-2	2-14-80	8.51	23.89
21108-11-4	2-14-80	8.32	23.50
21110-11-4	2-14-80	8.14	22.35
21105-11-2	2-12-80	8.07	21.14
21109-11-4	2-14-80	6.93	21.17
<u>Two Layer TiO_x/SiO₂</u>			
21106-11-3	2-14-80	8.24	21.85
21108-11-1	2-14-80	8.02	22.76
21110-11-3	2-14-80	7.83	21.82
21106-11-1	2-14-80	7.66	21.57
21110-11-1	2-14-80	7.38	20.69
21108-11-3	2-14-80	7.26	20.35
21109-11-3	2-14-80	7.02	19.32
21109-11-1	2-14-80	7.00	18.80
21105-11-1	2-12-80	5.52	14.94
21105-11-3	2-12-80	4.72	12.69

* At 100 mW/cm²

A review of the yield of cells processed by the standard procedure (20 - 40 second etch in dilute HCl and 10 second reaction in CuCl solution) revealed that there had been some decline during the first part of the quarter. In the middle of January a focused effort was made to ensure that each step of the process was carried out with great attention to detail and that cells were moving from stage to stage with a minimum of delay. As a result a substantial improvement in performance was achieved as revealed by the following statistics. During February 88 cells were made using the standard process. Of these 24 cells exceeding 8% with a maximum efficiency of 8.98%, 31 cells were between 7 and 8% efficiency, 16 cells between 6 and 7% and only 17 cells less than 6%. A full statistical analysis of cell yield will be given in the next quarterly report.

Further attempts to improve the current of solid state process cells are being made on substrate #2.1103. A short solution reaction in the standard bath is being utilized. Initial test results are promising. The final heat treatments will take place during the next quarter.

4.2 (CdZn)S/Cu₂S Solar Cells

4.2.1 Material Analysis

During the past quarter alternative material designs were investigated to address the problems of the bimodal grain size distribution in the (CdZn)S films, and the temporal instability of V_{oc} . Such an approach was necessitated

by the fact that the V_{OC} stability that was expected using the solid state reaction Cu_2S formation process did not occur even though a greatly reduced Cu_2S intrusion morphology was realized with this process. It was concluded that either the small submicron grains of the bimodal distribution or some other aberration in the Cu_2S morphology was responsible. In particular with respect to the latter, it was thought that since the $(CdZn)S$ films were observed to be more brittle than CdS , they would be more susceptible to the occurrence of cracks and defects. For example, such cracks or defects could occur as a consequence of the relaxation of mechanical stresses caused by the thermal mismatch between $(CdZn)S$ and the copper substrate, and/or the handling which attends device fabrication. The two approaches designed to address these separate possibilities are described below.

$NiFe$ (42% Ni , 58% Fe) has a thermal expansion coefficient ($4.6 \times 10^{-6} \text{ }^{\circ}C^{-1}$ from $25^{\circ}C$ to $300^{\circ}C$) which matches well with CdS ($C : 4.3 \times 10^{-6} \text{ }^{\circ}C^{-1}$ at $25^{\circ}C$; $5.7 \times 10^{-6} \text{ }^{\circ}C^{-1}$ at $200^{\circ}C$) and fairly well with $(CdZn)S$ having low zinc content (for ZnS , $C : 6.5 \times 10^{-6} \text{ }^{\circ}C^{-1}$ at $25^{\circ}C$ (3)). Thus, in contrast to $(CdZn)S$ films grown on copper substrates at elevated temperature ($\sim 200^{\circ}C$), $(CdZn)S$ films grown on $NiFe$ substrates at elevated temperatures do not exhibit the curling effect that attends cooling the substrates to room temperature. However, owing to the poor optical reflection properties of the $NiFe$ in the spectral region important for the multiple pass aspect of device operation, it is necessary to develop a thin covering layer which increases substrate reflection. Of the several material options available to be the reflecting layer, which included

aluminum and silver, copper was chosen. As in the case with the copper substrate, an additional protective layer is necessary in order to inhibit the formation of unwanted Cu_2S during the initial stages of $(\text{CdZn})\text{S}$ deposition. Two material options were considered for this protective layer: zinc and ITO. A layer of zinc has been shown to work as the protective layer for the copper substrate. However, since zinc is a poor reflector the layer must be thin enough ($\sim 0.3 \mu\text{m}$) to allow brassification to occur, thus improving substrate reflection. Alternatively, an ITO layer would protect the copper layer and in addition, because it transmits light in the spectral region of interest, offers the opportunity to realize a greater amount of the reflection from the copper surface. The optical results of initial work on the development of suitable reflective/protective layers for NiFe are presented in Section 4.2.2, and the accompanying cell results in Section 4.2.3.

In general, it has been observed that CdS films do not exhibit the bimodal grain size distribution typically observed in $(\text{CdZn})\text{S}$. It was decided that perhaps the $(\text{CdZn})\text{S}$ nucleation and growth habit could be influenced by providing a CdS substrate. Both CdS and $(\text{CdZn})\text{S}$ films are of the wurtzite structure and typically grow with their c-axes approximately perpendicular to the substrate. For zinc concentration less than 20% the difference in lattice constant perpendicular to the c-axes is less than 1.5%. To the extent that the electron affinities for the CdS and $(\text{CdZn})\text{S}$ will differ by up to 0.2 eV for the range of interest, depending on the zinc composition, there will be a junction found at the CdS/ $(\text{CdZn})\text{S}$ interface. However, if this

junction is sufficiently far away from the photovoltaic (CdZn)S/Cu₂S junction, it may be treated as a diode in series with the photovoltaic junction. It is shown in an Appendix to this report that as long as the CdS resistivity is less than 0.3 ohm-cm (for $x = x_{\text{CdS}} - x_{\text{(CdZn)S}} = 0.2$ eV) or less than 16 ohm-cm (for $x \approx 0.1$ eV), then V_{oc} and J_{sc} for the device is unaffected, and at the maximum power point for the device, the power loss due to the (CdZn)S/CdS junction is less than 1%. The structural results of the initial experiments to grow bilayer films (i.e. (CdZn)S on CdS) are presented in Section 4.2.2 and the accompanying cell results in Section 4.2.3.

4.2.2 Material Fabrication

A. Nickel Iron Substrates

The 50 μm thick NiFe substrates are first precleaned in Buhler detergent, and then in 10% H_2SO_4 prior to the application of a plated copper layer. An approximately 0.5 μm thick copper plating is accomplished using a copper chloride solution. The structure of the copper surface is characterized by small, sub-micron grains, and the morphology replicates the NiFe surface being quite flat as compared to the conventional copper substrate.

Several copper-plated NiFe substrates were subsequently coated with a 0.2 μm thick sputtered ITO protective layer. The reflectivity spectrum of these substrates was quite good rivaling that of the reflectivity from a non-zinc plated conventional copper substrate. However, (CdZn)S films deposited on these substrates contained small black areas, most likely occurring where the ITO did not cover the underlying copper, allowing the formation of

Figure 2

Total reflectivity from zinc/copper plated NiFe and zinc plated copper substrate.

Cu_2S at the substrate-(CdZn)S interface. Cells made on these substrates displayed value of V_{oc} which were lower than expected for the zinc composition, and the device fill factors were generally less than 60%. Although there have been successes with NiFe Cu-ITO as a substrate for CdS films, its present utilization in the (CdZn)S program was deemed inappropriate.

The procedure for applying an approximately $0.35 \mu\text{m}$ thick plated zinc layer to the NiFe/Cu substrate is identical to that used for the conventional copper substrates. Cells made from such substrates (details in Section 4.2.3) typically exhibited low light-generated currents, and reduced V_{oc} . The reduced V_{oc} was most likely a consequence of the many small (CdZn)S grains of these films. A large factor contributing to the low ($\sim 11\text{--}12 \text{ mA/cm}^2$) light generated current was the lack of suitable reflectivity from the back contact (i.e. (CdZn)S-substrate interfaces). Figure 2 shows a comparison of the reflectivity spectrum for a zinc-plated ($\sim 0.5 \mu\text{m}$), copper plated ($\sim 0.6 \mu\text{m}$) NiFe substrate with the spectrum for zinc plated ($\sim 0.6 \mu\text{m}$) copper (shiny side). Both spectra were taken on samples which had been heat treated in vacuum for a time sufficient to insure that no further change would occur in the respective spectrum as a consequence of the interdiffusion of zinc and copper. A solar weighted average reflectance at AM1.5 from NiFe/Cu/Zn substrate was 61% as compared to 78% from the Cu/Zn substrate. It is expected that an increase of up to 15% in light generated current can be achieved by making up this difference in reflectivity from the back, and by assuring a substrate morphology which allows for light trapping⁽⁴⁾.

The spectral response curve for (CdZn)S/Cu₂S cells prepared on the NiFe/Cu/Zn is shown in Figure 3 along with the spectral response of a high efficiency (>8%) CdS cell. Part of the reduction of the overall response, and the fall-off at longer wavelengths is a consequence of inadequate substrate reflection. Because optimal device operation depends on the occurrence of multiple reflection (i.e. increased optical path lengths), the decreased substrate reflection reduces spectral response, since with increasing wavelength the Cu₂S optical absorption coefficient is decreasing.

During the next quarter work will be undertaken to improve the copper and zinc plated layers. In particular copper films having a suitable light trapping morphology will be developed. It is planned to accomplish this by preparing thicker films (up to 4 μ m) which will permit, after suitable heat treatments to inter-diffuse the copper and zinc layers, the appearance of a higher fraction of copper at the (CdZn)S interface, thus increasing substrate reflectance⁽⁵⁾. To accomplish this however, it is further necessary to prepare a zinc layer which on the one hand is thick enough to exclude the formation of Cu₂S during initial (CdZn)S film growth, and on the other hand thin enough to insure the best substrate reflection (i.e. after brassification).

B. Bilayer (CdZn)S/CdS Films

Figure 4(a) shows a SEM micrograph of a bilayer (CdZn)S/CdS film grown on a zinc plated copper substrate and reveals grain sizes in the range of 2 to 4 μ m. The grain structure is revealed by sequentially forming and removing a Cu₂S layer using the wet process⁽⁸⁾. The bilayer was prepared by first growing

Figure 3

Spectral response for a (CdZn)S/Cu₂S cell on NiFe/Cu/Zn and a high efficiency CdS/Cu₂S cell.

a 20 μm thick CdS film, then following a break in vacuum, an 18 μm thick film of (Cd/Zn)S; the substrate temperature for both film growths was 225°C. For comparison Figure 4(b) shows a 22 μm thick (CdZn)S film grown directly on a zinc-plated copper substrate. Inspection shows that the single layer film in contrast to the bilayer film, is characterized by a bimodal distribution grain size; one having an average size in the range of 2-4 μm , the other less than 0.5 μm .

Figure 5 is an SEM micrograph of a single layer (CdZn)S film grown on a zinc-plated (0.35 μm thick), copper-plated (0.50 μm thick) NiFe substrates which reveals a grain structure dominated by sub-micron grains. Figure 6 is the SEM micrograph of a bilayer (CdZn)S (18 μm thick)/CdS (19 μm thick) film grown on a similar substrate and indicates the absence of sub-micron grains.

Recently modifications in the bell jar film growth system have been completed which will enable both films of the bilayer structure to be grown without breaking vacuum. In addition, the improved substrate temperature control system previously implemented in the CdS growth system has been added to the (CdZn)S system.

4.2.3 Device Fabrication and Analysis

For the purpose of evaluating the various (CdZn)S-substrate structures cells were made from these substrates. Prior to Cu_2S formation using the

(a)

(b)

Figure 4

(a) Grain structure of (CdZn)S/CdS bilayer on Cu/Zn.

(b) (CdZn)S layer on Cu/Zn. x2000

Figure 5

Structure of a single layer of (CdZn)S grown on NiFe/Cu/Zn. x2000

Figure 6

Structure of a bilayer (CdZn)S/CdS grown on NiFe/Cu/Zn. x2000

solution reaction process, the (CdZn)S surface was textured by immersion for 10-20 sec. in a 25% HCl solution held at 60°C. A previous investigation for (CdZn)S films on copper substrates, recently substantiated for films on NiFe as well, has shown that reaction times of this duration are sufficient to optimize light trapping⁽⁶⁾. The details of the standard CuCl solution used to form the Cu₂S have been previously reported⁽⁷⁾. Standard 32.5 line/cm. grids are subsequently applied; typically, for these evaluations, no AR coatings are used.

Table 4 shows a comparison of cell data averages for single (CdZn)S (SS# 1-296) and bilayer ((CdZn)S/CdS) films grown on copper substrates. Both structures have zinc concentrations of 14%; they exhibited similar values of open circuit voltage and light generated current, and produced cells with conversion efficiencies (without AR) in excess of 7%. However, despite the

TABLE 4

Cell parameters for (CdZn)S/Cu₂S cells grown on Cu substrates.

<u>SS #</u>	<u>t_{CdS} (μm)</u>	<u>t_{(CdZn)S} (μm)</u>	<u>Zn (%)</u>	<u>(ohm-cm)</u>	<u>V_{oc}(mV) @ 25 mA/cm²</u>	<u>J_L (mA/cm²) @ 100 mW/cm²</u>	<u>best η (%)</u>
1-296	x	22	14	7.8	594 6	18.6 1.4	7.3
1-317	20	18	14	0.3	600 5	17.5 0.3	7.6

Cell parameters for (CdZn)S/Cu₂S cells grown on NiFe substrates.

1-320	x	18	14	2.2	609 3	11.3 0.4	4.3
1-323	19	18	13	0.4	620 7	12.8 0.2	4.6

absence of the bimodal structure, cells made on the bilayer film (#1-317) still exhibited temporal instability in V_{oc} .

Table 4 also shows a comparison of cell data (averages) for single ((CdZn)S) (#1-320) and bilayer ((CdZn)S/CdS) (#1-323) films grown on NiFe substrates.

For similar zinc concentrations the open circuit voltages are comparable, and somewhat higher than on the copper substrates, perhaps as a consequence of the more planar morphology that characterizes the surfaces of films grown on NiFe.

The light generated currents are quite low for both types of film structures. However, as discussed earlier the substrate (i.e. (CdZn)S substrate interface) reflection and light trapping properties are not properly optimized. On the other hand cells made from both the single layer structure, characterized by small ($\sim 0.5 \mu\text{m}$) average grain sizes, and the bilayer, which had an average grain size of about $2 \mu\text{m}$, exhibited no temporal instability in V_{oc} .

Table 5 summarizes the grain structure and V_{oc} stability data for both the single and bilayer film structure on copper and NiFe substrates.

TABLE 5

Influence of substrate and growth process on the
grain structure of (CdZn)S films and the
stability of (CdZn)S/Cu₂S cells.

<u>Substrate</u>	<u>Layer-Structure</u>	<u>Grain Structure</u>	<u>Voc Stable</u>
Copper	Single Layer	Bimodal (~0.5 μ m and 2-4 μ m)	No
Copper	Bilayer	2-4 μ m	No
Nickel-Iron	Single Layer	0.5 μ m	Yes
Nickel-Iron	Bilayer	1-2 μ m	Yes

It is concluded that the existence of small, sub-micron grain sizes is not sufficient to cause V_{oc} instability. Furthermore, to date cells fabricated on those films grown on NiFe substrates do not exhibit temporal instability. It is inferred that one or more film defects are caused by the relaxation of thermal mismatch stresses, or handling operations that accompany device fabrication, and that it is these defects that are responsible for V_{oc} instability. During the next quarter an investigation as to the identity of these defects will be undertaken.

4.3 Electro-Optic Analysis & Modeling

Changes have been made in the capacitance measuring system to improve resolution, accuracy, and reproducibility. These are described below, first treating details of the modifications to the circuit and method, then in terms of results in N_D^* , S_1/μ_2 , and changes in deep-level trapping with temperature.

Figure 7 shows the block diagram of the capacitance measuring system. The basic method has not been changed, but a new amplifier and current-to-voltage converter have been incorporated into the system. The amplifier, whose circuit is shown in Figure 8, supplies the signal $(V + V_{AC})$ to the cell, where the DC bias V can be set from about -10v to +1v without overloading the circuit, and V_{AC} is the AC modulation. Noise problems in the V_{AC} are much less serious in the new amplifier than in the earlier system. The new current-to-voltage converter, shown in Figure 9, comprises two RC-coupled stages, so that DC in the cell does not affect the AC from which capacitance is determined.

Capacitance test circuit

Figure 7. Block diagram of capacitance test circuit.

Amplifier for Signal
applied to cell in capacitance test

Figure 8

Amplifier for signal applied to cell.

Figure 9
Current to voltage converter.

Interface recombination measurements: From variation of capacitance and collection efficiency η_c with white-light illumination of the cell, its interface parameters have been deduced. Analysis of earlier results revealed excessive scatter in η_c , caused mostly by non-uniformity in illumination of the cell and the Si monitor cell below it. This problem has been corrected, with the result that S_1/μ_2 and the other parameters are obtained with greater accuracy. Error has typically been reduced by a factor of 4.

In addition, a computer program has been put into operation to obtain the parameters more efficiently, as well as their expected errors. The errors are obtained by standard statistical methods, and allow one to assess the precision of stated values and the significance of differences between results of different experiments.

Schottky barriers: Four Schottky barriers of different areas were made by evaporating Au front contacts on CdS substrate #2108. Capacitance was measured on each of these at DC bias from -1.0v to .2v. Figure 10 shows plots of the resulting $(A/C)^2$ vs. V, along with fitted straight lines and calculated effective donor densities N_D^* . The close agreement in slope indicates, besides good reproducibility, that area effects, and therefore edge effects, have little influence on the results. The derived N_D^* is larger than values characterizing CdS/Cu₂S cells by a factor of ~ 4 to 25. Resistivity of this substrate was 4.5 ohm-cm, and barrier height, from a plot of $\log J$ vs V, was .75eV.

Figure 10

$1/C^2$ vs V plots for Au/CdS Schottky barrier.

Low temperature measurements: A cryostat has been set up, after some initial difficulties, to allow capacitance measurements of samples at a temperature which can be held anywhere between 77K and 300K. A mounting block for 1 cm^2 cells has been placed so as to be illuminated through two windows at right angles to each other. Calibration at the sample location indicates good accuracy of the built-in temperature controller.

Temperature effects: As a baseline for later measurements, effects of low temperature on C_{AM1} and C_{dark} have been measured.

Cooling cell #21065.111 from room temperature to liquid nitrogen temperature affects C_{dark} rather weakly. Specifically, C_{dark}/A drops from 3.5 nF/cm^2 at 297K to 3.1 nF/cm^2 at 78K. Variations of C_{dark} with DC bias gives $N_D^* = 1.9 \times 10^{16}\text{ cm}^{-3}$ at 297K and $N_D^* = 2.9 \times 10^{15}\text{ cm}^{-3}$ at 78K. The extent to which this decrease results from either a change in density of states or in decreasing excitation from shallow donor levels will be investigated in later experiments.

Effects of temperature on C_{AM1} are considerably stronger. Figure 11 shows schematically the variation of C_{AM1} and I_{sc} as a function of temperature. The minimum in C_{AM1} at 223K and the maximum at 85K are certain to within about $\pm 5\text{K}$, but the locations of the other features are subject to correction because effects of thermal lag have not been taken into consideration. Planned transient experiments combined with these results should give information on traps in the CdS, their energy levels, cross-sections, and density variations.

cell 1065.111
variation of C_{AM1} and I_{sc}
with temperature (schematic)

Figure 11

Variation of C_{AM1} and I_{sc} with temperature. CdS/Cu₂S cell #21065.111.

4.4 Encapsulation for Improved Stability

In order to determine the optimum for the trial deposition parameters glass (IEC 9658) a 2 x 2 matrix of deposition rates and temperatures has been carried out on the matte and smooth side of electro-cleaned copper foil. The temperatures were 25 and 150°C and the rates were 5 and 50 Å/second. SEM examination showed that best films, in terms of the structure, are obtained when the deposition rate and substrate temperature are respectively 5 Å/second and 150°C. Under these deposition conditions, on the smooth side of copper foil, no discernable loss of adhesion or overgrowths were observed over an area of 1/2" x 1/2". On the other hand, when the substrate temperature is lowered to 25°C (keeping the rate of deposition at 5 Å/second) the prevalence of overgrowths was increased. Figure 12 shows the surface topography of these two films.

(a)

(b)

Figure 12 Surface topography of glass films deposited on the smooth side of electro-cleaned copper foil. Deposition rate $5 \text{ \AA/sec}$. Marker - $10 \text{ }\mu\text{m}$. (a) Substrate temperature: 25°C . (b) Substrate temperature: 150°C .

Films deposited on the rough side of the copper foil showed similar behavior. In this case however, it was not possible to eliminate the structural imperfections completely (over a 1/2" x 1/2" area). Even at 5 $\text{\AA}/\text{second}$ and 150°C some minimal cracking was observed. The structure of the glass film on the rough side of the copper foil is shown in Figure 13.

Figure 13 Surface topography of glass film deposited on the rough side of the copper foil. Marker = $10\text{ }\mu\text{m}$. Deposition rate $5\text{ }\text{\AA}/\text{second}$. Substrate temperature 150°C .

In order to establish that no significant change in chemistry is resulting from e-beam evaporation both the source powder and the glass film were examined by EDAX. The results are shown in Figure 14. The film analyzed was deposited on the smooth side of copper foil at 5 Å⁰/second and at 150°C. As can be seen in Figure 14 there are no significant chemical changes taking place during evaporation at least in terms of the major components (i.e. Al, Si, and Ba).

Figure 14

X-ray emission spectrograph of source glass and e-beam deposited film.

IEC80290

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APPENDIX

Influence of (CdZn)S/CdS Junctions

For a layer of (CdZn)S deposited on CdS the band details of the junction between them depend on the electron affinities, ϕ_{CdZnS} and χ_{CdS} , and the work functions, ϕ_{CdZnS} and ϕ_{CdS} . Figure A1 shows the schematic representation of the two materials prior to junction formation, and for three separate specific cases, the resulting band bending that attends junction formation. Using the defined quantities, $\Delta\chi$ and $\Delta\phi$, the expression

$$\Delta\chi + \Delta\phi = (\phi_{\text{CdZnS}} - \chi_{\text{CdZnS}}) - (\phi_{\text{CdS}} - \chi_{\text{CdS}}) \quad (\text{A1})$$

relates the energetic differences between the Fermi level and conduction band edge for the (CdZn)S and CdS, respectively. Equation (A1) may be written in terms of effective densities of states, N_{ci} , mobilities, μ_{ni} , and conductivities, σ_i for (CdZn)S ($i = 1$) and CdS ($i = 2$) as

$$\begin{aligned} \Delta\chi + \Delta\phi &= \frac{kT}{q} \left(\ln \frac{N_{c1} e \mu_{n1}}{\sigma_1} - \ln \frac{N_{c2} e \mu_{n2}}{\sigma_2} \right) \\ &= \frac{kT}{q} \ln \left(\frac{N_{c1}}{N_{c2}} \frac{\mu_{n1}}{\mu_{n2}} \frac{\sigma_2}{\sigma_1} \right) . \end{aligned} \quad (\text{A2})$$

Assuming that $N_{c1} \approx N_{c2}$, $1 < \left(\frac{\mu_{n1}}{\mu_{n2}} \right) < 1$, and $1 < \left(\frac{\sigma_2}{\sigma_1} \right) < 10$, then

$\Delta\chi + \Delta\phi < .06\text{eV}$. Since $\Delta\chi \approx 0.2$, therefore $\Delta\phi < -0.14\text{eV}$; and for the range of values considered $|\Delta\phi| < \Delta\chi$. Thus, since $\Delta\phi < 0$ and $|\Delta\phi| < \Delta\chi$ the junction schematic IB of Figure A1 describes the (CdZn)S-CdS junction. For the worst case, which has all the band bending occurring in the (CdZn)S

as depicted in Figure A2, the barrier height, ϕ_B , is given as

$$q\phi_B = \Delta\chi + (\phi_{\text{CdS}} - \chi_{\text{CdS}}). \quad (\text{A3})$$

Figure A3(a) shows an equivalent circuit for a photovoltaic battery which produces the potential V_j (j_+) given as

$$V_j = \frac{kT}{q} \ln \frac{j_+ + j_L + j_{01}}{j_{01}}. \quad (\text{A4})$$

Figure A3(b) shows the equivalent circuit for the photovoltaic battery, an applied voltage, V_A , and a diode in series. The diode represents the (CdZn) S/CdS junction and may be treated as a series component if that junction is not involved in current collection. For the circuit in Figure A3(b)

$$V_2 = \frac{kT}{q} \ln \frac{j_{02}}{j_{02} - j_+}. \quad (\text{A5})$$

Using the relation $V_A = V_j + V_2$ and the results of equations (A4) and (A5), we derive

$$V_A = \frac{kT}{q} \left(\ln \frac{(j_+ + j_L + j_{01})}{j_{01}} - \frac{j_{02}}{(j_{02} - j_+)} \right). \quad (\text{A6})$$

and rewriting

$$j = \frac{-j_L + j_{01} (e^{qV_A/kT} - 1)}{(j_{01} e^{qV_A/kT} + 1)} \quad (A7)$$

From (A6)

$$V_A (j_+ = 0) \equiv V_{oc} = \frac{kT}{q} \ln \frac{j_L + j_{01}}{j_{01}} \quad (A8)$$

and from (A7)

$$J (V = 0) \equiv j_{sc} = - \left(\frac{j_{02}}{j_{01} + j_{02}} \right) j_L \quad (A9)$$

Thus, so long as $j_{02} \gg j_{01}$ there is no loss in either V_{oc} or j_{sc} as a consequence of the (CdZn)S/CdS junction.

In order to limit the power loss due to the series diode to less than 1%, we require that

$$P_{loss} = J_{mp} V_{2f} < 10^{-4} \text{ watts/cm}^2 \quad (A10)$$

where

$$V_{2f} = \frac{kT}{q} \ln \frac{j_- + j_{02}}{j_{02}} \quad (A11)$$

Combining (A10) and (A11) with $j_- = J_{mp}$, we get

$$j_{mp} \left(\frac{kT}{q} \ln \frac{j_{mp} - j_{02}}{j_{02}} \right) < 10^{-4} \text{ watts/cm}^2$$

and the condition on j_{02} becomes

$$j_{02} > \frac{j_{mp}}{e^{\left(\frac{q}{kT}\right) \left(\frac{10^{-4}}{j_{mp}}\right)} - 1} \quad (A12)$$

If $j_{mp} = 25 \times 10^{-3} \text{ amps/cm}^2$, then $j_{02} = 1.5 \times 10^{-1} \text{ amps/cm}^2$.

By using the relationship between j_{02} and ϕ_B ,

$$\phi_B = \frac{kT}{q} \ln \frac{j_{00}}{j_{02}} \quad (A13)$$

and combining the expression for resistivity,

$$\rho_{CdS} \text{ (ohm-cm)} = \frac{1}{N_C q \mu e^{-(q\phi_{CdS} - \chi_{CdS})/kT}} \quad (A14)$$

with equation (A3) we get the relation between ρ and j_{02}

$$\rho_{\text{CdS}} = \frac{j_{00}}{j_{02}} \left(\frac{1}{N_c q \mu_e \Delta\chi / kT} \right). \quad (\text{A15})$$

Since by (A12) we found that $j_{02} > 1.5 \times 10^{-4}$ amp/cm², thus

$$\rho_{\text{CdS}} < 6.7 j_{00} \left(\frac{1}{N_c e \Delta\chi / kT_e} \right).$$

If $N_c = 2 \times 10^{18}$ cm⁻³, $\mu = 2 \times 10^2$ cm² volt⁻¹ sec⁻¹, $j_{00} = 10^4$ amp/cm² and $\Delta\chi = 0.2$ eV, then $\rho > 0.34$ Ω .cm in order to insure minimal external fill factor loss. If $j_{00} = 10^4$ amp/cm² and $\Delta\chi = 0.2$ eV, then $\rho < 16$ Ω cm. to minimize external fill factor loss.

Define: $\Delta \chi \equiv \chi_{CdS} - \chi_{(Cd/Zn)S}$

$$\Delta \phi \equiv \phi_{(CdZn)S} - \phi_{CdS}$$

Possible Junctions:

1. $\Delta \phi < 0$

A. $|\Delta \phi| > \Delta \chi$

B. $|\Delta \phi| < \Delta \chi$

2. $\Delta \phi > 0$

Figure A1. Schematic of (CdZn)S/CdS junction.

Figure A2. (CdZn)S/CdS junction for $\Delta\phi < 0$ and $|\Delta\phi| < \Delta\chi$ with all band bending occurring in (CdZn)S.

(a)

(b)

Figure A3.

- (a) Equivalent circuit for photovoltaic battery.
- (b) Simple series circuit for photovoltaic battery, diode and source of applied voltage.