DATA HANDLING FACILITY
for the
SANDIA PARTICLE BEAM FUSION ACCELERATOR*

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MASTER

Introduction

This paper describes an on-line data handling facility for Sandia's Particle Beam Fusion Accelerator, PBFA-I, and the upgrade prototype machine Supermite. These accelerators are used for research on inertial confinement fusion (ICF) using particle beams. The main objectives in designing the data acquisition system were:

1. process both experiment and machine performance diagnostic signals,
2. record high signal-to-noise ratio, wideband waveforms in a severe EMP environment,
3. support multiple users recording and analyzing data simultaneously, and
4. provide fast turnaround for experimental results.

Commercially available equipment is used wherever possible. However, several special purpose devices were developed. This data handling facility is a significant upgrade of an existing system that supports other Sandia particle beam fusion research accelerators.

Accelerators

PBFA-I has 36 independent beam lines and is capable of delivering 30 terawatts and 1 megajoule in a 2 to 4 megavolt, 35 ns pulse into a target chamber.² The accelerator can be configured to generate either electrons or ions. The objective is to deliver sufficient beam energy to demonstrate the scientific feasibility of ICF. The accelerator upgrade, PBFA-II, will provide 3 times as much power in the 1984-85 time frame. The Supermite accelerator is a 4 module prototype used to develop higher power components. Other small accelerators are also planned for the facility.

Cable System

Signals to be recorded are fast transient pulses of 10-1000 ns duration and 10-5000 volt peak amplitude. These waveforms must be recorded in the presence of EMP levels generated by di/dt and dv/dt of 10^{15} amps and volts per second. This EMP level requires that signal cables be carefully shielded over the entire run. A picture of the cable plant is shown in Fig. 1.

Jumper cables run from diagnostic monitors to feedthru ports near the floor of the tank. These

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consist of RG-214 cable run inside flexible solid convolute shield tubing. Special adapters were designed to mate the shield conduit to type N and HN connectors in an electrically and mechanically sound fashion. Ferrite sleeves are inserted in the adapters to further reduce noise pickup. Fig. 2 shows an assembled cable and the convoluted shield. The entire I-beam support structure beneath the tank was made rf-tight. This enclosure contains 800 RG-331 cables which run from feedthru ports in the bottom of the accelerator to a shielded splice room. All cables serving similar diagnostics were cut to equal lengths to $\pm .5$ ns. From this point signals can either be recorded and processed locally or jumpered to the main screen room for processing. There are 270 RG-331 cables run from the splice room to the screen room in nine 6-inch diameter conduits. A tenth conduit is available for further expansion. Unshielded RG-214 cables are used as jumpers in both the splice and screen rooms.

Computer Hardware

Most data recording and processing electronics are housed in a high quality double-shielded rf screen room. A photograph is shown in Fig. 3. This room is 15'W x 65'L x 10'H with a raised floor.

A block diagram of the waveform recording system is shown in Fig. 4. The main computer is a Hewlett-Packard HP-1000 system with 256 Kb of 16 bit memory and a hardware floating point processor. Mass storage consists of a 20 Mb moving head disc drive with a 10 Mb removable cartridge and two 256 Kb floppy disc drives. A nine track, 45 ips, 850 bpi tape drive is also available. The system console is an HP-2648 graphics terminal with dual cassette tape drives. Two Tektronix 4014 Display Terminals with Enhanced Graphics Modules are available for data acquisition and reduction. Each terminal has a 4631 hard copier with 4-channel input multiplexer. A Versatec 1200A printer/plotter is also available. This device has a Versatec 5-channel input multiplexer to enable the plotter to make high quality hard copies from the Tektronix terminals. The data acquisition HP-1000 is tied via an HP DS-1000 inter-computer link to a similar computer in the PBFA facility control room.

Waveform Digitizing Hardware

The facility has 44 Tektronix 7912AD Transient Digitizers with 7A16P programmable vertical amplifiers and 7B90P programmable time bases. The vertical amplifier has a specified minimum bandwidth of 200 MHz. This is adequate for recording virtually all

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accelerator and experiment diagnostic signals.

The 7912AD's are interfaced to the HP-1000 computer via IEEE 488 General Purpose Instrumentation Buses (GPB). Each GPB is specified to handle 15 devices, including the controller. However, the bus would intermittently fail whenever more than eight 7912AD's were powered up on that bus. This problem was solved by installing capacitors on the HP controller cards to slow down the handshaking process. The fastest pulse widths were increased from 300 ns to 600 ns. This enabled bus signal levels to reach a full 2.5V.

Data signals from up to three different experiments are cabled to the input ports of a computer controlled four-position coax rotary switch module. Computer generated calibration signals are connected to the fourth port. The coax switches are Tektronix SM-2 matrices with twelve modules per unit. The SM-2's are controlled by 32 bit digital output cards in a Tektronix 1340 Data Coupler. The Data Coupler also houses the vertical and horizontal reference signal generator cards used for autocalibration. The Data Coupler is interfaced to the HP-1000 computer via an RS-232 link operating at 1100 baud.

The output signal from the coax switch is fed into a programmable attenuator. A fiducial timing marker pulse can then be added to the signal via a resistive power adder. This configuration requires an isolation amplifier in the fiducial signal line to prevent cross-talk among data signals through the fiducial fanout network. In some cases the fiducial signal is routed to the 7912AD vertical amplifier B channel, and timing information is only recorded during the preshot baseline check.

The programmable attenuators are Allen Industries Model 50DA63. Attenuations of 0-63 dB may be selected in 1 dB steps by relay closures. They are controlled by standard relay driver cards in Hewlett-Packard Multiprogrammer chassis. The Multiprogrammers are interfaced to the computer over the GPB. The attenuators can reliably withstand 500 V, 100 ns pulses. Higher energy signals are routed through special fixed attenuators in front of the coax switch. These devices consist of 3 and 8 W low inductance resistors mounted on 50 Ω stripline boards in a minibox with type N connectors.

Precision timing is required to record and analyze the diagnostic signals. All cables have been built to $\pm .5$ ns as measured by a cable length digitizer. Special trigger and fiducial marker pulse generators were developed for this facility.

The trigger generator was built by Science Applications, Inc. (SAI).³ The unit is fabricated as 6 NIM-type modules. Analog, digital, manual, and internal rep rate inputs are provided. Each analog input has a slope/level discriminator. Minimum delay time is 30 ns for both analog and digital inputs. Outputs are divided into four groups of 16 each. Each group is separately delayable from nominal 0-10 ns in 10 ns steps. Asynchronous clocks are used to yield a

shot-to-shot jitter of < 1.0 ns. All functions of the trigger generator can be computer controlled via the GPB. Programmable functions include: input enable for any or all channels; analog slope and level; digital slope; output delay.

The fiducial generator was also developed by SAI.⁴ This device will trigger on a fixed minimum input pulse level of 2 volts. The unit has ten outputs of 35 volts simultaneous to $\pm .1$ ns. Output pulse width is variable from 2-20 ns in 2 ns steps. The width may be increased by increasing the length of the internal 10 Ω printed circuit charge line.

The data system has the requirement to record almost 400 diagnostic signals to fully monitor PBFA-I performance. This precludes using 7912AD's. Sandia is funding development of a multichannel waveform digitizer to record transient signals. The design goals for this device are 40 channels sampled simultaneously at intervals variable from 1-50 ns and a record length of 240 samples per channel. Full scale amplitude sensitivity is fixed at 2 V. A ± 1 V offset is available to allow efficient recording of of unipolar or bipolar signals.

A block diagram of the multichannel recorder is shown in Fig. 5. Input voltage signal channels are converted to light by fast LED's. All light outputs are routed by fiber optics to the photocathode input faceplate of a streak camera tube. The electron beams from the photocathode are accelerated, focused and swept across the phosphor screen output faceplate. Fiber optic faceplates are used on both input and output to maximize light transfer. The light from the phosphor is carried by a fiber optic reducing bundle to a commercial TV format Charge Coupled Device (CCD) chip. The CCD serves as an analog storage device. Data signals are clocked out from the CCD, digitized, and stored in a digital solid state memory at conventional rates. The multichannel recorder is interfaced to the computer via the GPB. The initial prototype is scheduled for completion in 1981.

Accelerator Performance Monitors

Many accelerator performance diagnostic signals may be adequately monitored by a single parameter once the machine operation has been characterized. These parameters include switch closure times, peak amplitudes, and time integrals. A stand-alone accelerator Performance Measuring and Evaluation System (PMES) is being developed to record and process single point data. A typical signal channel is shown in Fig. 6.

Commercial CAMAC modules are used to record approximately 300 channels of signal parameters. Special NIM-type signal conditioning and trigger modules have been developed to support this system. Inputs to CAMAC time digitizers are buffered by 16 channel avalanche transistor discriminator modules. Inputs to CAMAC gated peak detectors and integrators are processed by modules which can contain any combination of attenuators, power splitters, pulse

inverters, and integrators. Trigger fanout modules with four TTL input channels and six low level NIM outputs per channel are used to start time digitizers. Gate generator modules with one TTL input and four low level NIM outputs are used to drive gated peak detectors and integrators. Commercial NIM time delay generators are also used in the system.

The PMES operates in a stand-alone mode with a Standard Engineering MIK-11/2 crate controller with dual double-density floppy discs. The CAMAC system will be located in the cable splice room below the accelerator tank. This location was chosen because of the limited number of cables running to the main screen room. The MIK-11/2 is interfaced to the main facility CPU via an RS-232 fiber optic link.

Software

The HP-1000 computer runs under the RTE-IVA operating system with the Multi-Terminal Monitor. The only modification required on the system software was to enable the GPIB driver to schedule a user program upon receipt of a service request interrupt (SRQ). Previously the driver could only be enabled to auto-poll predefined devices. However, the auto-polling would not process extended talker and listener devices which require secondary addressing. This feature is used in the 7912AD's to distinguish main-frame, vertical amplifier, and time base commands.

Applications software for the PBFA data handling system is functionally similar to that developed for the previous facility. However, all programs have been rewritten in a structured, table-driven format to maximize maintainability and expandability. The programs were also designed to be as machine independent as possible. Approximately 12,000 lines of Fortran code have been developed.

Major programs support the following functions:

1. Automatic digitizer set up and data collection.
2. Automatic digitizer calibration.
3. Interactive data reduction.
4. Shot archiving.

Fortran was used because it was the only supported high level language available for the HP-1000 when the project was started. All hardware configuration parameters are placed in tables. Input table data is in ASCII format and may be modified by the source editor. Special programs translate the source tables to mixed-type-variable records and store them in random access files. Special subroutines access these tables for applications programs. Thus hardware capabilities may be modified and expanded without rewriting software.

The automatic data acquisition program (AQD) begins by reading and processing a table of signal channel parameters for a given shot. The program uses this and calibration tables to set up all signal recording equipment to be used for the shot. It then digitizes a baseline and checks each digitizer for proper operation. AQD then arms for the shot.

Finally, after the shot, the program reads, calibrates and stores each waveform on the disc. The calibration process consists of:

1. Averaging to center of trace,
2. Multiplying in vertical amplifier gain, attenuations, and gauge scale factors,
3. Correcting for time base sweep nonlinearity,
4. Compensating high frequency cable losses.

After AQD has stored all the waveforms, they are available for user processing. An Interactive Data Reduction (IDR) program is used extensively for manipulating and plotting signals. This program provides the following capabilities:

1. Interactive or procedure file macro-type command execution.
2. Access data from multiple shots on either hard or floppy discs.
3. Array arithmetic operations - add, multiply, divide, square root, exponentiation, raise-to-power, minimum, maximum, average, integration, differentiation.
4. Fourier transform, convolution, deconvolution, low pass filter.
5. Single, multiple, overlaid, and windowed plots.
6. Cursor control and printout.
7. Control of all programmable hardware functions.

Fig. 7 shows an example of a waveform processed using IDR commands.

An automatic calibration program (ACL) is used to generate and maintain 7912AD and programmable attenuator calibration data. This program generates cal signals and switches them to the appropriate digitizer. It digitizes the resulting waveforms and computes calibration factors. This data is stored on disc for use by programs AQD and IDR in calibrating signal waveforms.

Accelerator shots are archived on floppy discs. This method is superior to mag tape in that it provides rapid direct access to old shots. The following information is stored for each shot:

- Shot set up header
- Calibration data
- Baseline levels
- Calibrated and uncalibrated data records
- Cable compensation functions.

Software for the PMES system is functionally similar to that for the HP computer. Many routines were directly transportable. Machine dependent subroutines were rewritten. The relatively limited capabilities of the PMES computer forced some simplifications in the software system design. Programs were written to support automatic data acquisition, interactive hardware manipulation, interactive calibration, and transfer of data to and from the HP computer. Programs have been written for the HP computer to enable interactive and automatic data transfers between the two systems.

Conclusion

The data acquisition and handling system described above is operational and supporting PBFA-I and Supermite. The 7912AD waveform recording hardware and software have been running since January 1980. The PMES system is currently being brought on line as PBFA-I is characterized. The same system will also support other small accelerators which are planned for the facility.

Figure Captions

- Fig. 1. Cut away view of PBFA-I with fixed cable plant.
- Fig. 2. Shielded jumper cable connector assembly and stripped back convoluted shield.
- Fig. 3. Data Acquisition facility main screen room hardware.
- Fig. 4. Block diagram of waveform recording system.
- Fig. 5. Multichannel Recorder block diagram.
- Fig. 6. Block diagram of typical PMES signal channel.
- Fig. 7. Data signals processed by program IDR. Vacuum interface di/dt , integral with respect to time and magnitude of Fourier transform of each in dB.

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Fig. 1. Cut away view of PBFA-I with fixed cable plant.

Fig. 2. Shielded jumper cable connector assembly and stripped back convoluted shield.

Fig. 3. Data Acquisition facility main screen room hardware.

Fig. 4. Block diagram of waveform recording system.

Fig. 5. Multichannel Recorder block diagram.

TYPICAL PMES/MONITOR CHANNEL

Fig. 6. Block diagram of typical PMES signal channel

PBFF SHOT 86 10/10/80 11:1:00

IDR READY
XFR A B
IDR READY
MUL B .3906E-9
IDR READY
FFT B
IDR READY
LOG B
IDR READY
MUL B 20.
IDR READY
LAB B FTUIBDB
IDR READY
PLO B Q2 TICS

INTEG A
IDR READY
LAB A VICURB
IDR READY
PLO A Q3

XFR A D
IDR READY
MUL D .3906E-9
IDR READY
FFT D
IDR READY
LOG D
IDR READY
MUL D 20.
IDR READY
LAB D FTUIECUR
IDR READY
PLO D Q4 TI

Fig. 7. Data signals process by by program IDR. Vacuum interface di/dt, integral with respect to time and magnitude of Fourier transform of each in dB.