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LeCROY WIRE CHAMBER SYSTEM *

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This is a report on the LeCroy wire chamber electronics system; its characteristics, design, performance, and connections to the PDP-5 computer. This report is not complete, but is intended as an explanation of the basic system. For more details, one should refer to the PDP-5 manuals for questions concerning the computer, and to the LeCroy manuals for questions concerning the LeCroy electronics. This report discusses the following subjects:

- I Basic System Components
- II Timing of Signals
- III Wire Chamber Characteristics
- IV Computer Control
- V Examples of Simple Computer Test Routines
- VI Wire Chamber Electronics Test Routine
- VII Schematics and Cable Connections.

I. Basic System

The basic LeCroy wire chamber readout system consists of the following parts:

- (a) Wire spark chambers with associated triggering supplies.
- (b) Magnetostrictive pickup devices with preamplifiers mounted near the spark chambers.
- (c) Discriminator circuits mounted in the LeCroy digitizers some distance away from spark chambers, connected to the preamplifiers by 50 ohm coaxial cable only.
- (d) Clock, gating circuits, and scalers which digitizer and store the time between the arrival of the first signal and successive signals from the preamp.
- (e) An interface which connects the LeCroy data bus to the PDP computer. This device provides suitable logic levels to both the LeCroy units and the computer. It is controlled by computer command, but has some automatic functions built into it. The data is strobed into the computer through the accumulator, one 12-bit word at a time, upon command from computer control. The presence of data ready to be transferred is signalled to the computer by computer interrupt.
- (f) The PDP-5 (and later perhaps the PDP-8) is programmable and can handle the data in a very flexible way. The biggest limitations here are lack of memory space, and lack of a good Fortran system. Because of this, the computer should be consigned to simple data-taking tasks, and computational work should be done in a larger computer. The PDP-5 can store data on magnetic tape, which can be read by IBM 7094 or 360 series computers.

II. Timing of Signals

The signal to fire the wire chambers is generated by a set of particle counters, such as scintillators with photomultiplier tubes attached, connected through a fast logic system in such a way as to select a desired type of event. This signal also should be sent to the "System Trigger" input of the interface. A -1 volt, 50 nsec long pulse is sufficient. A sequence of timing signals are generated internally, ending with an interrupt which is sent to the computer. At that time, program control will request data to be transferred. Upon completion of transfer, a "Clear" command is sent to the interface, which clears out all scalers and returns the interface to ready. A second system trigger will not be accepted until a clear signal has arrived. The sequence of internal signals consists of

- (a) BUSY - interface is "BUSY" from time of system trigger arrival to time of clear signal arrival.
- (b) CLAMP - an internal reset signal generated to hold all scalers at 0 until spark chamber noise and transients die away. This pulse can be shortened or lengthened by adjusting the pot on the front of the interface.
- (c) DIGITIZE - an internal delay of about .5 ms which allows time for all magnetostrictive signals to arrive before a computer interrupt signal is generated.
- (d) DATA AVAILABLE - a state that becomes "1" at the end of the digitize delay. It can be tested by the computer through the "SKIP-ON-DATA-AVAILABLE" Pulse.
- (e) PROGRAM INTERRUPT - the interrupt signal is generated at the end of the digitize delay, simultaneously with the DATA-AVAILABLE STATE.

For complete sequence of pulses, see the timing chart. A more complete description of computer commands is given in the section on computer functions.

FIGURE 1
TIMING CHART (not to scale)

III. Wire Chamber Characteristics

Signals which arrive from the preamps are spaced in time by the ratio of distance between wires carrying current to the velocity of sound in the magnetostrictive ribbon. This spacing in time is digitized by a 20 MHz clock which passes through gating circuits to scalers. In a given LeCroy 180 Time Digitizer Module, there are located 8 scalers, each connected, at the inputs, to the 20 MHz clock through input gating logic; and each is connected, at the outputs, to a 12-bit data bus through output gating logic. All scalers begin to count upon arrival of a first pulse, usually the "fiducial" signal. Each successive signal arrival turns off successively one scaler in sequence. Thus the contents of successive scalers contains the time of arrival of successive signals, quantized into 50 nsec units of time, after the first signal.

For sake of flexibility, switches on the front of each Time Digitizer Module can disconnect scalers from the sequence of 8 and connect them to their own inputs. Thus, one module can serve as 8 scalers in sequence, or as 4 plus 4 scalers, or as 6 and 2, 2 and 6, or 2,2,2, and 2, depending on the position of the switches.

Output gating is designed to connect sequentially each of the 8 scalers to the 12-bit data bus, upon receipt of sequential commands from the computer. This is done by suitable gating logic in the scanner section of the Time Digitizer. When more than one Time Digitizer is connected in series, the second and successive modules are strobed onto the data bus by continuing to give commands from the computer. This is achieved by the "Start Scan" and "End Scan" signals in the Time Digitizers. The "End Scan" signal of the 1st module goes to the "Start Scan" input of the 2nd module, and so forth. Thus after each 8 commands, scanner control

advances to the next Time Digitizer Module. This scheme allows for an unlimited number of modules to be read without changing any hardware.

The spatial resolution of the system is controlled by the frequency of the clock and the velocity of sound in the wire. With the clock frequency of 20 MHz and a sound velocity of 5 mm/ μ sec, this resolution is about $\pm .2$ mm. Tests of the resolution were performed using wire strips on a test bench. Adjacent wires were individually sparked a number of times, and the digitized positions stored in memory. Each time a wire was sparked, the digitized time was binned so as to form a histogram. In figure 2, we see the results obtained for a series of adjacent wires spaced 1 mm apart. The arrows show the expected positions of the wires based on interpolation between fiducials.

Often sparks will jump to more than one wire in a wire chamber. The following test was performed to see how well the electronics picks out distance between wires when the current splits onto two wires. To measure this, resistance of known values were attached to adjacent wires, allowing the ratio to be adjusted. Figure 3 shows how the position of the spark appears to move as the ratio of the currents goes from 0 in the first to 0 in the second.

Finally, the pulse-pair resolution is important. The electronics cannot resolve two adjacent wires which fire simultaneously because of the "fatness" of the signal from the preamp. It turns out that two wires about 4 mm apart can be accurately resolved.

FIGURE 2

RESOLUTION OF ADJACENT WIRES (PULSED INDIVIDUALLY, NOT SIMULTANEOUSLY)

FIGURE 3

RESPONSE TO CURRENT SPLITTING BETWEEN TWO ADJACENT WIRES.
 CURRENT RATIO = CURRENT IN #1 / CURRENT IN #1 + CURRENT IN #2.
 RELATIVE POSITION = POSITION OF SIGNAL BETWEEN WIRES #1 & #2.

V. Computer Control

In this section is a discussion of how the system can be controlled from the computer. The commands the computer uses, and examples of short routines will be given. For sake of clarity, the following terms and definitions should be referred to:

- (a) Spark Chamber Module - a single gap consisting of a frame, a set of "X" wires on one side, a set of "Y" wires on the opposite side, and associated power and fiducial connections.
- (b) Spark Chamber Plane - one half of the module; either the "X" plane or the "Y" plane.
- (c) LeCroy Module - one box of electronics consisting of 8 scalers, associated input and output gating logic, one or two discriminator boards, and switches, etc. In the later LeCroy design, a module will have only 4 scalers on a plug-in card.
- (d) Record - For each spark chamber plane, a set of scalers within the module must be allocated for storage of spark information. The number of scalers allocated can be changed by front-panel switches. Typically this number will be 4, but may also be 2, 6, or 8. The set of scalers assigned to each plane constitutes a record for that plane.
- (e) Spark - used to mean the signal generated by one spark or fiducial signal inside a chamber.
- (f) Spark Overflow - a logic level set to "1" if more sparks arrive than there is capacity for storage. (Also called Record Overflow).

- (g) Word Overflow - a scaler will continue to scale if no spark signal arrives to shut it off. Typically, if a record of length 4 sees only one "spark", all 4 scalers will overflow. (The one "spark" is the start signal, and successive sparks close off successive scalers up to 4.) Word overflow sets all scaler bits to 1. Thus a 12-bit scaler would contain (111 111 111 111) = 7777₈.
- (h) End of Record - a logic level set to "1" when the last scaler of a record is connected to the data bus through the output gates.

The computer has the following set of instructions for control and data transfer:

Table I

	<u>OP CODE</u>	<u>DESCRIPTION</u>
CLR	6774	CLEAR
ADV	6761	ADVANCE
DRD	6764	DATA READ
SDA	6762	SKIP ON DATA-AVAILABLE
SER	6771	SKIP ON END OF RECORD
SRO	6772	SKIP ON RECORD OVERFLOW
TS1	6751	TEST PULSE 1
TS2	6752	TEST PULSE 2
STG	6741	SYSTEM TRIGGER

CLR is the clear and general reset command. This puts the entire system in a state ready for an event. ADV commands the interface to connect the next scaler in line to the data-bus through gating logic. Successive ADV commands causes successive scalers to be presented to the data bus. DRD is a command which strobes the information on the data bus into the accumulator of the computer. The DRD is a logical OR operation.

Thus it is usually wise to proceed DRD by a CIA command to insure that the accumulator is clear before reading. SDA is a branching command which allows the computer to test the state of the LeCroy system. This command causes the following instruction to be skipped if the DATA-AVAILABLE state is "1". It is used in connection with the interrupt routine to let the computer find the source of the interrupt and take appropriate action. SER allows the computer to check if the scaler currently being read is end scaler in a record. SRO allows the computer to determine if a spark overflow has occurred for that record.

TS1 is a test pulse which the computer uses to check out the system. It is connected to the discriminator card and triggers the discriminator to simulate the arrival of sparks. TS2 is an additional test pulse which can be used to simulate clock pulses. The front panel toggle switch must be in the "Test" position for this pulse. The use of these two signals is illustrated later. Finally STG is an additional IOP pulse which is plugged into the system trigger input during testing routines. This also serves as a convenient scope trigger because it is located on a 50 ohm cable coming out of the front panel of the computer. (Note: Because of timing constraints, do not combine commands such as ADV DRD = 6765.)

VI. Examples of Simple Test Routines

- (a) Be sure the cable 6741 is plugged into the system trigger. The following program should give simple results:

20	CLR	6774
1	STG	6741
2	TS1	6751
3	TS1	6751
4	TS1	6751
5	TS1	6751
6	TS1	6751
7	TS1	6751
30	TS1	8751
1	TS1	6751
2	TS1	
3	SDA	6762
4	JMP*-1	5233
5	AGN ADV	6761
6	CLA	7200
7	DRD	6764
40	HLT	7402
41	JMP AGN	5235

Place the RUN-TEST switch in RUN. Set the DELAY to 0. The program should halt in cell 40 with $360 (\pm 1)_8$ in the accumulator. This is the digitized IOP time of the computer (for the PDP-5, the IOP time is about 12 ms). Press continue and the accumulator should hold the contents of the second scaler. Successive "continues" will give the contents of successive scalars.

- (b) In the previous example, the use of TS1 was to simulate arrival of spark signals which the electronics digitizes into intervals of 360_8 . To test the scalars on single pulses, the TS2 pulse can be used, provided that the Run-Test switch is in the "Test" position.

An example of such a program to do this is

20		CLR	6774
21		STG	6741
22		TS1	6751
23		SDA	6762
24		JMP*-1	5223
25		TS2	6752
26	AGN	ADV	6761
27		CLA	7200
30		DRD	6764
31		HLT	7402
32		JMP AGN	5226

Place the Run-Test Switch in "Test"; DELAY to zero, Start at 20. The computer should halt at 31 with a 1 in the accumulator. Press continue to read successive scalers. Be sure that B and D input switches are up, but C can be up or down.

The following section describes a complete test routine written specifically to test the wire chamber electronics system, using this set of commands.

VI. Wire Chamber Electronics Test Routine

This program was written with the idea that it would be used before production runs start as a complete check of performance of electronics. Each bit of each scaler is checked as well as input and output gating logic. Output is from the ASR-33 teletype unit in the form of error diagnostics and other information. The program is located on magtape, and on cards so that it may be reassembled on tape if the existing tape is lost or broken. The program starts in cell 20, and is "self-guiding"; just follow the typewriter instructions. Diagnostics other than "Test 11" are abnormal and should not appear. A little thought and understanding of the test performed and design of electronics will usually allow one to pinpoint the disease from the nature of the diagnostic. The following are

the tests and diagnostics performed:

- (1) Starting at cell 20, a set of instructions are printed on the teletype. Follow them precisely! The computer halts, expecting a number to be placed in the switch register. After placing the number of "modules" (for this test, all modules are considered to be grouped into sets of four scalers) in the SR, press continue.
- (2) The first test; after a system trigger, computer should receive an interrupt. Diagnostic: "TEST 1: INTERRUPT DID NOT OCCUR"
- (3) After interrupt, computer tests for skip-on-data-available. Diagnostic "TEST 3: SKIP-ON-DATA-AVAILABLE-DID-NOT-OCCUR"
- (4) Computer generates a CLR and checks that all scalers contain 0. Diagnostic "TEST 2:
MODULE XXXX, SCALER XXXX DID NOT CLEAR PROPERLY. SCALER CONTAINS XXXX,
COMPUTER EXPECTS 0000.
- (5) After reading last scaler of array, an ADV pulse should clear the DATA-AVAILABLE state. Diagnostic "TEST 10: COMPUTER EXPECTS LAST
MODULE END-SCAN PULSE (FINISH PULSE) TO RESET THE DATA-AVAILABLE
STATE IN THE INTERFACE"
- (6) This computer places alternately a 1 in each bit of all scalers. Then it reads the contents into the computer and compares with what should be there. Diagnostic "TEST 4: MODULE XXXX, SCALER XXXX DID
NOT SCALE PROPERLY. SCALER CONTAINS XXXX, COMPUTER EXPECTS XXXX.
- (7) Computer checks that scalers overflow properly (scale up to 7777, but not beyond) and clear to 0000 when general reset occurs. Diagnostic: "TEST 6: WORD OVERFLOW ERROR. SCALER CONTAINS XXXX, COMPUTER EXPECTS
7777. or "TEST 7: WORD OVERFLOW DOES NOT CLEAR. SCALER CONTAINS
XXXX. COMPUTER EXPECTS 0000.

- (8) To check the input gating logic, a sequence of TS1, TS2, TS1, TS2, TS1, TS2, etc. is given. This should store a 1 in the first scaler of each module, 2 in the second, 3 in the third, etc. The purpose of the test is to check that input gates open and close properly.

Diagnostic:

TEST 9: MODULE XXXX, SCALER XXXX. STEERING LOGIC ERROR AT INPUT.

SCALER CONTAINS XXXX, COMPUTER EXPECTS XXXX.

- (9) Checks that scalers do not scale if no spark signals are received.

Diagnostic: "TEST 8: MODULE XXXX, SCALER XXXX SCALES WITHOUT INPUT TRIGGER APPLIED"

- (10) After completing the above tests, the computer will type out instructions to throw switches to "RUN". The computer then sends a series of TS1 pulses in sequence, which is digitized by the Time Digitizer circuits. The results are printed out in columns. All numbers in a column should agree to ± 2 units. This test is called "TEST 11". After completing the printout, the computer halts, so the RUN-TEST switches can be placed in "TEST" again. Upon continuing, the computer repeats all tests except TEST 11. It will continue to loop, printing any error messages if errors are found, until halted by the operator.

The following pages contain a listing of the PDP-5 program, excluding the diagnostics.

SAMPLE OUTPUT FROM TEST ROUTINE. OTHER TELETYPE OUTPUT INDICATES
MALFUNCTION OF ELECTRONICS.

WIRE CHAMBER ELECTRONICS CHECKOUT

- (1) SET B&D LECROY INPUT SWITCHES UP.
- (2) CONNECT OP 6741 CABLE INTO SYSTEM TRIGGER.
- (3) SET DELAY TO ZERO.
- (4) SET RUN-TEST SWITCH TO TEST.
- (5) ENTER NUMBER OF LECROY MODULES TO BE TESTED IN SR, IN OCTAL
- (6) PRESS CONTINUE.

TEST 11: THIS SUBROUTINE DIGITIZES THE I O P CYCLE TIME OF THE
COMPUTER AND PRINTS OUT THE CONTENTS OF THE SCALERS.
SET THE RUN-TEST SWITCHES TO -RUN- AND PRESS CONTINUE.

MODULE/SCALER	1	2	3	4	5	6	7	10
0001	0360	0740	1321	1701				
0002	0360	0740	1320	1700				
0003	0361	0740	1320	1700				
0004	0360	0741	1320	1700				
0005	0357	0737	1316	1677				
0006	0360	0741	1320	1700				
0007	0360	0740	1320	1700				
0010	0360	0740	1321	1700				
0011	0360	0740	1320	1700				
0012	0360	0742	1320	1700				
0013	0360	0740	1320	1700				
0014	0360	0740	1320	1700				
0015	0360	0741	1320	1700				
0016	0361	0741	1320	1701				

RETURN THE RUN-TEST SWITCHES TO -TEST- AND PRESS CONTINUE.

```

DEF LAS 7604
DEF STL 7120
DEF ADV 6761
DEF DRD 6764
DEF SDA 6762
DEF CLR 6774
DEF STG 6741
DEF TS1 6751
DEF TS2 6752
DEF ION 6001

```

```

REM INTERRUPT CHECK
ORG 0001

```

```

1 C
2 5312 JMP CONT
ORG 0020
20 4315 JMS DIAGN
21 7200 CLA
22 7402 HLT
23 7604 LAS
24 3261 DCA NMCD
25 4652 JMSI ICNE
26 4653 JMSI ITWO
27 4654 JMSI ITHREE
30 4655 JMSI IFOUR
31 4656 JMSI IFIVE
32 4657 JMSI ISIX
33 4660 JMSI ISEVEN
34 7200 CLA
35 4246 JMS DIAG21
36 7402 HLT
37 4652 JMSI ICNE
40 4653 JMSI ITWO
41 4654 JMSI ITHREE
42 4655 JMSI IFOUR
43 4656 JMSI IFIVE
44 4657 JMSI ISIX
45 5237 JMP *-6
46 C DIAG21
47 4745 JMSI ITYPE1
50 21 0021
51 5646 JMPI DIAG21
52 100 ICNE ONE
53 200 ITWO TWO
54 274 ITHREE THREE
55 400 IFOUR FOUR
56 441 IFIVE FIVE
57 505 ISIX SIX
60 600 ISEVEN SEVEN
61 C NMCD

```

```

ORG 0100

```

```

REM SUBROUTINE ONE

```

```

REM SUBROUTINE ONE CHECKS FOR INTERRUPT AND SKIP

```

```

REM -ON-DATA-AVAILABLE MALFUNCTION

```

```

100 C CNE
101 6042 TCF TURN OFF TELETYPE INTERRUPT
102 6032 KCC
103 7201 CLA IAC
104 6714 6714 CLEAR TAPE UNIT FLAG
105 6774 CLR
106 6001 ION
107 6741 STG
110 4331 JMS SCL
111 4321 JMS DIAG1
112 6762 CCNT SDA

```

Line	Address	Label	Operation	Comments
113	4325		JMS	DIAG3
114	5700		JMPI	CNE
115	C	CIAGO		
116	4745		JMSI	ITYPE1
117	C			0000
120	5715		JMPI	DIAGC
121	C	CIAG1		
122	4745		JMSI	ITYPE1
123	1			0001
124	5721		JMPI	DIAG1
125	C	DIAG3		
126	4745		JMSI	ITYPE1
127	3			0003
130	5725		JMPI	DIAG3
131	C	SDL		
132	3342		DCA	AC
133	1343		TAD	BCC
134	7041		CIA	
135	3344		DCA	IND
136	1342		TAD	AC
137	2344		ISZ	IND
140	5337		JMP	*-1
141	5731		JMPI	SDL
142	C	AC		
143	700	BCC		0700
144	C	INC		
145	2200	ITYPE1		TYPE1

REM SUBROUTINE TWO
 REM SUBROUTINE GENERATES A GENERAL RESET AND CHECKS
 REM ALL SCALERS THAT THEY CONTAIN 0 ALSO IT CHECKS
 REM THAT A FINISH SIGNAL RESETS DATA-AVAILABLE STATE TO
 REM IF A SCALER AFTER THE LAST IS ATTEMPTED TO BE READ.
 ORG 200

200	C	TWC			
201	6774		CLR		GENERAL RESET
202	6741		STG		
203	6762		SDA		WAIT FOR DATA-AVAILABLE
204	5203		JMP	*-1	
205	7200		CLA		
206	3271		DCA	SCALER	
207	7001		IAC		
210	3272		DCA	MODULE	INITIALIZE MODULE TO 1
211	4626	NR	JMSI	INCSCI	PREPARE TO READ NEXT SCALER
212	5221		JMP	EOR	
213	6761		ADV		
214	7200		CLA		
215	6764		DRC		
216	7440		SZA		SHOULD BE 0
217	4227		JMS	DIAG2	
220	5211		JMP	NR	
221	6761	ECR	ADV		ADVANCE BEYOND LAST SCALER
222	6762		SDA		SHOULDN'T SKIP HERE IF FINISH
223	5600		JMPI	TWO	PULSE IS PRESENT
224	4233		JMS	CIAG20	
225	5600		JMPI	TWO	
226	237	INCSCI		INCSCA	
227	C	DIAG2			
230	4346		JMS	DIAG	
231	2			0002	
232	5627		JMPI	DIAG2	
233	C	DIAG20			
234	4765		JMSI	JTYPE1	
235	20			0020	
236	5633		JMPI	DIAG2C	

REM SUBROUTINE INCSCA
 REM THIS SUBROUTINE KEEPS TRACK OF WHICH SCALER IS BEIN
 REM AFTER LAST SCALER IS READ, IT ZEROS THE INDEX REGIS
 REM FOR MODULE NUMBER AND SCALER NUMBER. TO USE THIS
 REM SUBROUTINE THE COMPUTER INSTRUCTION IMMEDIATELY AFT
 REM THE CALL (JMS INCSCA) SHOULD BE THE THE STATEMENT
 REM WHICH IS EXECUTED AFTER THE LAST SCALER IS READ. T
 REM FOLLOWING STATEMENT SHOULD BEGIN THE TEST OF SCALER
 REM FUNCTION.

237	C	INCSCA			
240	72CC	CLA			
241	1271	TAD	SCALER	CHECK TO SEE IF SCALER .GT. 3	
242	7C41	CIA			
243	1266	TAD	+7		
244	751C	SPA			
245	5251	JMP	NXT	YES	
246	2271	ISZ	SCALER	NO	
247	2237	ISZ	INCSCA		
250	5637	JMPI	INCSCA	RETURN	
251	2273	ISZ	MODULE	INCREMENT MODULE	
252	720C	CLA			
253	3271	DCA	SCALER	CLEAR SCALER	
254	1273	TAD	MODULE		
255	7C41	CIA			
256	1667	TADI	INMOD		
257	751C	SPA		IS IT LAST MODULE	
260	5262	JMP	ER	YES	
261	5246	JMP	SC	NO	
262	720C	CLA		SET MODULE=1 TO INITIALIZE IT	
263	70C1	IAC		FO NEXT TIMR	
264	3273	DCA	MODULE		
265	5637	JMPI	INCSCA	RETURN	
266	7	OCT	0003	←	Should be
267	61	INMOD	NMOD		

270	1034	ITYPE2	TYPE2	
271	C	SCALER		
272	C	CCMP		
273	C	MODULE		
REM SUBROUTINE THREE PLACES A ONE IN EACH BIT OF ALL				
REM SCALERS AND CHECKS FOR ERROR ON READOUT.				
274	C	THREE		
275	7200	CLA		
276	3272	DCA	COMP	
277	3271	DCA	SCALER	
300	7001	IAC		
301	3273	DCA	MODULE	
302	7120	STL		SET LINK = 1
303	5306	JMP	**3	
304	7300	INC	CLA	CLL
305	1272	TAD	COMP	
306	7004	RAL		SHIFT ONE LEFT
307	7430	SZL		
310	5674	JMPI	THREE	ALL BITS TESTED
311	3272	DCA	CCMP	
312	3366	DCA	YNDEX	
313	6774	CLR		OPEN INPUT GATES
314	6741	STG		
315	6751	TS1		
316	6762	SDA		PAUSE UNTIL DATA AVAILABLE
317	5316	JMP	*-1	
320	6752	MCRE	TS2	PUT COUNT IN
321	2366	ISZ	YNDEX	SCALERS
322	7200	CLA		
323	1366	TAD	YNDEX	
324	7041	CIA		
325	1272	TAD	COMP	
326	7440	SZA		SCALE UP TO COMP
327	5320	JMP	MCRE	
330	4764	IRM	JMSI	INCSC2
331	5304	JMP	INC	
332	6761	ADV		READ NEXT SCALER
333	7200	CLA		
334	6764	DRD		
335	7041	CIA		CCMPARE CONTENTS
336	1272	TAD	COMP	WITH COMP
337	7440	SZA		
340	4342	JMS	DIAG4	
341	5330	JMP	IRM	
342	C	DIAG4		
343	4346	JMS	DIAG	
344	4		0004	
345	5742	JMPI	DIAG4	
346	C	DIAG		
347	7200	CLA		
350	1273	TAD	MODULE	
351	3360	DCA	**7	
352	1271	TAD	SCALER	
353	3361	DCA	**6	
354	1746	TADI	DIAG	
355	2346	ISZ	DIAG	
356	3362	DCA	**4	
357	4670	JMSI	ITYPE2	
360	C		0000	
361	C		0000	
362	C		0000	
363	5746	JMPI	DIAG	
364	237	INCSC2	INCSCA	
365	2200	JTYPE1	TYPE1	

		REM	SUBROUTINE FOUR	
		REM	SUBROUTINE FOUR CHECKS THAT SCALERS OVERFLOW (=7777	
		REM	AND THAT THE OVERFLOW CLEARS TO 0000 WHEN GENERAL	
		REM	RESET OCCURS.	
		ORG	400	
400	C			SUBROUTINE FOUR
401	7200	CLA		
402	6774	CLR		
403	6741	STG		
404	6751	TS1		OPEN ALL INPUT GATES
405	6762	SDA		
406	5205	JMP	*-1	
407	3235	DCA	CNT	CLEAR CNT
410	6752	TS2		
411	2235	ISZ	CNT	OVERFLOW ALL SCALERS
412	5210	JMP	INCR	
413	4636	IS2	JMSI	
414	5224	JMP	INCSC3	
415	6761	ADV	FORW	
416	7200	CLA		READ NEXT SCALER
417	6764	DRD		
420	7040	CMA		IS CONTENT 7777
421	7440	SZA		
422	4264	JMS	DIAG6	COMPUTER EXPECTS 7777
423	5213	JMP	IS2	
424	6774	CLR		CHECK THAT ALL WOF'S CLEAR
425	4636	IS3	JMSI	
426	5600	JMPI	INCSC3	
427	6761	ADV	FOUR	
430	7200	CLA		
431	6764	DRD		
432	7440	SZA		COMPUTER EXPECTS 0000
433	4270	JMS	DIAG7	
434	5225	JMP	IS3	
435	C	CNT		
436	237	INCSC3	INCSCA	

SUBROUTINE FIVE

437	1000	N1	REM	1000	
440	C	M1		0000	
			REM	THIS SUBROUTINE CHECKS THAT SCALERS DO NOT	
			REM	SCALE IF INPUT STEERING LOGIC GATES ARE CLOSED.	
441	C	FIVE			
442	6774		CLR		RESET
443	6741		STG		
444	6762		SDA		WAIT FOR START SCAN PULSE
445	5244		JMP	*-1	
446	7200		CLA		
447	1237		TAD	N1	
450	3240		DCA	M1	INITIALIZE M1
451	6752		TS2		
452	2240		ISZ	M1	GENERATE 6777 PULSES
453	5251		JMP	*-2	
454	4704	NSC	JMSI	INCSC4	
455	5641		JMPI	FIVE	
456	6761		ADV		
457	7200		CLA		
460	6764		DRD		
461	7440		SZA		COMPUTER EXPECTS 0000
462	4274		JMS	DIAG8	
463	5254		JMP	NSC	
464	C	DIAG6			
465	4764		JMSI	IDIAG	
466	E			0006	
467	5664		JMPI	DIAG6	
470	C	DIAG7			
471	4764		JMSI	IDIAG	
472	7			0007	
473	5670		JMPI	DIAG7	
474	C	DIAG8			
475	4764		JMSI	IDIAG	
476	10			0010	
477	5674		JMPI	DIAG8	
500	C	DIAG9			
501	4764		JMSI	IDIAG	
502	11			0011	
503	5700		JMPI	DIAG9	
504	237	INCSC4		INCSCA	

RFM
 REM THIS SUBROUTINE CHECKS OPERATION OF INPUT
 REM GATING LOGIC. CONTENTS OF SCALERS 1,2 . . .8
 REM SHOULD CONTAIN 1,2, . . .8 RESPECTIVELY.

SUBROUTINE SIX

505	C	SIX	CLR	RESET
506	6774		CLL	
507	7100		STG	
510	6741		TS1	OPEN ALL GATES
511	6751		TS2	SCALES 1 COUNT
512	6752		TS1	CLOSES FIRST GATE OF EACH MOD
513	6751		TS2	SCALES 1 COUNT
514	6752		TS1	CLOSES FIRST GATE
515	6751		TS2	
516	6752		TS1	CLOSES SECOND GATE
517	6751		TS2	
520	6752		TS1	ETC.
521	6751		TS2	
522	6752		TS1	ETC.
523	6751		TS2	
524	6752		TS1	ETC.
525	6751		TS2	
526	6752		TS1	ETC.
527	6751		TS2	
530	6752		TS1	CLOSES LAST GATE
531	6762		SDA	WAIT FOR DA
532	5332		JMP	*-1
533	7200		CLA	
534	3363		DCA	MIND CLEAR INDICES
535	4765	SLP	JMSI	INCSC5
536	5705		JMPI	SIX
537	2363		ISZ	MIND
540	6761		ADV	
541	7200		CLA	
542	6764		DRD	
543	7041		CIA	
544	1363		TAD	MIND
545	7440		SZA	
546	4300		JMS	DIAG9
547	7200		CLA	CHECK TO RE-ZERO MIND IF GRE
550	1363		TAD	MIND
551	7041		CIA	
552	1362		TAD	PLUS7
553	7510		SPA	
554	5357		JMP	ZERC
555	5336		JMP	SLP
556	7200	ZERO	CLA	RE-ZERO MIND AFTER 7
557	3363		DCA	MIND
560	5336		JMP	SLP
561	3	PLLS7	OCT	0003
562	C	MIND		0000
563	346	ICIAG		DIAG
564	237	INCSC5		INCSCA

— Should be 00

REM
 REM THIS SUBROUTINE DIGITIZES THE BASIC IOT CYCLE
 REM TIME OF THE COMPUTER.
 ORG 600

SUBROUTINE SEVEN

600	C	SEVEN		
601	4226	JMS	DIAG12	
602	7402	HLT		
603	6774	CLR		RESET
604	6741	STG		
605	6751	TS1		DIGITIZE COMPUTER IOT CYCLE
606	6751	TS1		TIME
607	6751	TS1		
610	6751	TS1		
611	6751	TS1		
612	6751	TS1		
613	6751	TS1		
614	6751	TS1		
615	6751	TS1		
616	6762	SDA		WAIT FOR DA
617	5216	JMP	*-1	
620	4232	JMS	DIAG13	
621	4642	JMSI	INCSC6	
622	5600	JMPI	SEVEN	
623	6761	ADV		
624	4236	JMS	DIAG15	
625	5221	JMP	SINK	
626	C	DIAG12		
627	4545	JMSI	ITYPE1	
630	12		0012	
631	5626	JMPI	DIAG12	
632	C	DIAG13		
633	4545	JMSI	ITYPE1	
634	13		0013	
635	5632	JMPI	DIAG13	
636	C	DIAG15		
637	4545	JMSI	ITYPE1	
640	15		0015	
641	5636	JMPI	DIAG15	
642	237	INCSC6	INCSCA	

		AUTO1	EQU	10	
			DEF	6764	
			ORG	1000	
1000	272	CI		COMP	
1001	7777	MINUS1	DEC	-1	
1002	7774	MINUS4	DEC	-4	
1003	7776	MINUS2	DEC	-2	
1004	7772	MINUS6	DEC	-6	
1005	7771	MINUS7	DEC	-7	
1006	7770	MINUS8	DEC	-8	
1007	7767	MINUS9	DEC	-9	
1010	7761	MINU15	DEC	-15	
1011	7756	MINU18	DEC	-18	
1012	7746	MINU26	DEC	-26	
1013	1410	ICC6		DO6	
1014	1422	IDC7		DO7	
1015	1430	ITRY8		TRY8	
1016	2045	ICCOUNT		CCOUNT	
1017	2012	INUM		NUMBER	
1020	2047	IDIG		DIGIT	
1021	1220	AST45		STRN45	
1022	1323	AST5		STRNG5	
1023	1240	ASTDIO		STRDIO	
1024	1257	APROP		PROPER	
1025	1331	AEND4		END4	
1026	1270	ISCA		SCACON	
1027	2000	IPRIN		PRINT	
1030	1464	ITEST		TEST	
1031	C	NCIAG			
1032	C	MCDNUM			
1033	C	SCANUM			
1034	C	TYPE2			
1035	7200	CLA			SUBROUTINE TO PRINT
1036	6046	TLS			TYPE 2 DIAGNOSTICS
1037	1634	TADI		TYPE2	CLEAR TELEPRINTER FLAG
1040	3232	DCA		MODNUM	
1041	2234	ISZ		TYPE2	
1042	1634	TADI		TYPE2	
1043	3233	DCA		SCANUM	
1044	2234	ISZ		TYPE2	
1045	1634	TADI		TYPE2	
1046	3231	DCA		NCIAG	
1047	2234	ISZ		TYPE2	
1050	4630	JMSI		ITEST	WRITE TEST NUMBER
1051	1221	TAD		AST45	
1052	3010	DCA		AUTO1	
1053	1206	TAD		MINUS8	
1054	3616	DCAI		ICCOUNT	
1055	4627	JMSI		IPRIN	WRITE 'MODULE '
1056	1232	TAD		MCDNUM	
1057	3620	DCAI		IDIG	
1060	4617	JMSI		INUM	PRINT MODULE NUMBER
1061	1206	TAD		MINUS8	
1062	3616	DCAI		ICCOUNT	
1063	4627	JMSI		IPRIN	WRITE 'SCALER '
1064	1233	TAD		SCANUM	
1065	3620	DCAI		IDIG	
1066	4617	JMSI		INUM	PRINT SCALER NUMBER
1067	1231	TAD		NCIAG	
1070	1202	TAD		MINUS4	
1071	7650	SNA	CLA		IS IT 4
1072	5335	JMP		DO4	
1073	1231	TAD		NCIAG	
1074	1203	TAD		MINUS2	

Line	Address	Operation	Mode	Destination	Comments
1075	7650	SNA	CLA	IS IT 2	
1076	5310	JMP		DO2	-27-
1077	1231	TAD		NCIAG	
1100	1204	TAD		MINUS6	
1101	7650	SNA	CLA	IS IT 6	
1102	5613	JMPI		ID06	
1103	1231	TAD		NCIAG	
1104	1205	TAD		MINUS7	
1105	7650	SNA	CLA	IS IT 7	
1106	5614	JMPI		ID07	
1107	5615	JMPI		ITRY8	
1110	1223	DO2 TAD		ASTDID	
1111	3010	DCA		AUTO1	
1112	1207	TAD		MINUS9	
1113	3616	DCAI		ICCOUNT	
1114	4627	JMSI		IPRIN	WRITE 'DID NOT '
1115	1222	TAD		AST5	
1116	3010	DCA		AUTO1	
1117	1204	TAD		MINUS6	
1120	3616	DCAI		ICCOUNT	
1121	4627	JMSI		IPRIN	WRITE 'CLEAR '
1122	1224	PRC TAD		APROP	
1123	3010	DCA		AUTO1	
1124	1207	TAD		MINUS9	
1125	3616	DCAI		ICCOUNT	
1126	4627	JMSI		IPRIN	WRITE 'PROPERLY.'
1127	1212	SCA TAD		MINU26	
1130	3616	DCAI		ICCOUNT	
1131	1226	TAD		ISCA	
1132	3010	DCA		AUTO1	
1133	4627	JMSI		IPRIN	WRITE 'SCALER CONTAINS '
1134	5343	JMP		END45	
1135	1223	CC4 TAD		ASTDID	
1136	3010	DCA		AUTO1	
1137	1210	TAD		MINU15	
1140	3616	DCAI		ICCOUNT	
1141	4627	JMSI		IPRIN	WRITE 'DID NOT SCALE '
1142	5322	JMP		PRO	
1143	6764	END45 DRD		IDIG	
1144	3620	DCAI		INUM	PRINT CONTENTS OF SCALER
1145	4617	JMSI		NDIAG	
1146	1231	TAD		MINUS4	
1147	1202	TAD		MINUS4	
1150	7650	SNA	CLA	WANT 'COMPUTER EXPECTS '	
1151	5356	JMP		CONT4	YES
1152	1201	TAD		MINUS1	NO
1153	3616	DCAI		ICCOUNT	
1154	4627	JMSI		IPRIN	PRINT PERIOD
1155	5634	JMPI		TYPE2	
1156	1225	CONT4 TAD		AEND4	
1157	3010	DCA		AUTO1	
1160	1211	TAD		MINU18	
1161	3616	DCAI		ICCOUNT	
1162	4627	JMSI		IPRIN	WRITE 'COMPUTER EXPECTS '
1163	1600	TADI		CI	
1164	3620	DCAI		IDIG	
1165	4617	JMSI		INUM	PRINT NUMBER EXPECTED
1166	1201	TAD		MINUS1	
1167	3616	DCAI		ICCOUNT	
1170	4627	JMSI		IPRIN	PRINT PERIOD
1171	5634	JMPI		TYPE2	

			ORG	1540
1540	7777	JMIN1	DEC	-1
1541	7771	JMIN7	DEC	-7
1542	777C	JMIN8	DEC	-8
1543	7767	JMIN9	DEC	-9
1544	7753	MINU21	DEC	-21
1545	7752	JMIN22	DEC	-22
1546	7742	MINU30	DEC	-30
1547	7741	MINU31	DEC	-31
1550	774C	JMIN32	DEC	-32
1551	7732	JMIN38	DEC	-38
1552	1C31	JNDIAG		NDIAG
1553	272	JCCMP		CCMP
1554	1127	JSCA		SCA
1555	200C	JPRIN		PRINT
1556	2045	JCCUNT		CCUNT
1557	160C	AST6		STRNG6
1560	1626	AST7		STRNG7
1561	1665	AST8		STRNG8
1562	1733	AST9		STRNG9
1563	121C	ATST		STRTST
1564	7777	FGUR7		7777
1565	4	J4	OCT	4
1566	26C	J26C		260
1567	271	ISIND		SCALER

1410	1357	CC6	ORG	1410	
1411	3010		TAD	AST6	
1412	1345		DCA	AUTO1	
1413	3756		TAD	JMIN22	
1414	4755		DCAI	JCCUNT	
1415	1364		JMSI	JPRIN	WRITE '. WORD OVERFLOW
1416	3753		TAD	FOUR7	ERROR'
1417	1365		DCAI	JCOMP	
1420	3752		TAC	J4	
1421	5754		DCAI	JNDIAG	
1422	1360	CC7	JMPI	JSCA	
1423	3010		TAD	AST7	
1424	1347		DCA	AUTO1	
1425	3756		TAD	MINU31	
1426	4755		DCAI	JCCUNT	
1427	5754		JMSI	JPRIN	WRITE 'WORD OVERFLOW
1430	1752	TRY8	JMPI	JSCA	DOES NOT CLEAR'
1431	1342		TADI	JNDIAG	
1432	7650		TAC	JMIN8	
1433	5241		SNA CLA		IS IT 8
1434	1752		JMP	CC8	
1435	1342		TADI	JNDIAG	
1436	7650		TAD	JMIN9	
1437	5252		SNA CLA		IS IT 9
1440	7402		JMP	CC9	
1441	1361	CC8	HLT		STOPS HERE IF DIAGNOSTIC
1442	3010		TAD	AST8	NO. IS NOT 4,2,6,7,8,OR 9
1443	1351		DCA	AUTO1	
1444	3756		TAC	JMIN38	
1445	4755		DCAI	JCCUNT	
1446	3753		JMSI	JPRIN	WRITE ' SCALES WITHOUT
1447	1365		DCAI	JCOMP	INPUT TRIGGER APPLIED'
1450	3752		TAD	J4	
1451	5754		DCAI	JNDIAG	
1452	1362	CC9	JMPI	JSCA	
1453	3010		TAC	AST9	
1454	1350		DCA	AUTO1	
1455	3756		TAD	JMIN32	
1456	4755		DCAI	JCCUNT	
1457	1767		JMSI	JPRIN	WRITE '. STEERING LOGIC
1460	3753		TADI	ISIND	ERROR AT INPUT.'
1461	1365		DCAI	JCOMP	
1462	3752		TAD	J4	
1463	5754		DCAI	JNDIAG	
1464	C	TEST	JMPI	JSCA	
1465	1362				SUBROUTINE TO WRITE TEST NO.
1466	3010		TAD	ATST	
1467	1341		DCA	AUTO1	
1470	3756		TAD	JMIN7	
1471	4755		DCAI	JCCUNT	
1472	1752		JMSI	JPRIN	WRITE 'TEST '
1473	1366		TADI	JNDIAG	
1474	6041		TAD	J260	
1475	5274		TSF		
1476	6046		JMP	*-1	
1477	7200		TLS		PRINT DIAGNOSTIC NO.
1500	1340		CLA		(DECIMAL)
1501	3756		TAC	JMIN1	
1502	4755		DCAI	JCCUNT	
1503	5664		JMSI	JPRIN	PRINT COLON
			JMPI	TEST	

VI. The following schematics related to the Wire Chamber system are included.

- (1) LeCroy Model 180 Time Digitizer
- (2) Interface unit.
- (3) Magnetostrictive preamps.
- (4) Cable Connections.

SM7473N FLIP-FLOP A-B
 7474 FLIP-FLOP C
 7475 NAND GATES D,E,F
 7476 FLIP-FLOP W

QND	VOLTS	RESET
11	14	2.6
7	14	5.10
7	14	-
7	14	4.9

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LECROY RESEARCH SYSTEMS CORP.
 IRVINGTON-ON-HUDSON, N. Y.

DRAWN SG	CHECKED	JOB	DATE 4-18-67
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MODEL 180
INPUT ROUTING LOGIC

REFERENCE 40967

TRUTH TABLE

A	B	C	D	E	F	G	H	I	J	K	L	M	N	O	P	Q	R	S	T	U	V	W	X	Y	Z
1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

$H^4 - H^{11}$ FF'S AND GATES NOT SHOWN:
SAME AS $H^2 + H^3$

THREE ADDITIONAL CHANNEL
PAIRS SAME AS ABOVE.

	GND	VOLTS	RESET
740001 NAND GATES E+F	7	14	—
820 FLIP-FLOP $H^0 - H^1$	7	14	4, 9
820 FLIP-FLOP $H^2 - H^{14}$	7	14	5, 10
7400 UNLABELED NAND GATES	14	7	—

* STROBED TO READ DATA

SEE PIN CONNECTION CODE TABLE FOR OUTPUT
CONNECTOR PIN NUMBERS

LITCOY RESEARCH SYSTEMS CORP			
IRVINGTON ON HUDSON, N.Y.			
DRAWN 90	CHECKED	DATE 5-23-67	
MODEL 180 SCALER SECTION			
REFERENCE			50967

NOTE:

ALL PNP'S - 2N3640
NPN'S - 2N3583
DIODES - 1N4148
G₁, G₂ - EACH 1/2 SN7420N
G₃, G₄, G₅ - EACH 1/2 SN7410N
Y₁, Y₂, Y₃, Z - EACH 1/2 SN7473N

	GND	VOLTS
MMND GATES G ₁ - G ₈	7	14
FFS Y ₁ , Y ₂ , Y ₃ , Z	11	14

LITCOY RESEARCH SYSTEMS CORP.			
Model S.G.	Order	Rev	Date 4-12-67
MODEL 180 BS			
BUILT-IN SCANNER			
REV. 11-3/66-67			10667

LECROY RESEARCH SYSTEMS CORP. IRVINGTON, N. J.			
DRAWN SG	CHECKED	JOB	DATE 5-22-67
MODEL 180 XT 20 MHZ CRYSTAL OSCILLATOR			
REFERENCE	SHOP COPY		50867

W.C. PREAMP

ALL 0.022 μ f-10%-USCC-NO. C10A223K

ALL 100pf-10%-USCC-NO. C10A10IK

DATA BUS

Pin #	Bit #
A	2 ⁰
B	2 ¹
C	2 ²
D	2 ³
E	2 ⁴
F	2 ⁵
H	2 ⁶
J	2 ⁷
K	2 ⁸
L	2 ⁹
M	2 ¹⁰
N	2 ¹¹
P	2 ¹² (overflow - 12 Bit)
R	2 ¹³
S	2 ¹⁴ (overflow - 14 Bit)

CONTROL/MISCELLANEOUS

Pin#	Function
m	- Spare reset (not used)
n	- Reset/Enable
p	- Control Bus
r	- FINISH (tied through) (Return of ES)
s in	- Start Scan
s out	- End Scan
t	- Test Pulse 1
u	- End of Plane
v	- Spark overflow
w	- Inhibit (not used) TEST PULSE 2
x	- Ground

-39-

X

LECROY RESEARCH SYSTEMS CORP.			
IRVINGTON-ON-HUDSON, N. Y.			
DRAWN	CHECKED	JOB	DATE 4-10-67
<p>Pin Connection Code Amphenol Connector 201302-3 Model 180 Series Digitizers</p>			
REFERENCE			#

WIRE CHAMBER INTERFACE

TO COMPUTER

(Amphenol No. 201302-3)

A		2 ¹¹
B		2 ¹⁰
C		2 ⁹
D		2 ⁸
E		2 ⁷
F		2 ⁶
H		2 ⁵
J		2 ⁴
K		2 ³
L		2 ²
M		2 ¹
N		2 ⁰
P		
R		TS2
S		TS1
T		
U		
V		
W		
X		
Y		
Z		
a		
b		
c		
d	>	ADV
e		
f	>	SDA
h		
j	>	DRD
k		
m	>	SER
n		
p	>	SRO
r		
s	>	CLR
t		INT BUS
u		SKP BUS
v		
w		
x		CND

CABLE CONNECTIONS

TO DIGITIZER

(Amphenol No. 201302-3)

A		2 ⁰
B		2 ¹
C		2 ²
D		2 ³
E		2 ⁴
F		2 ⁵
H		2 ⁶
J		2 ⁷
K		2 ⁸
L		2 ⁹
M		2 ¹⁰
N		2 ¹¹
P		WOF
R		
S		
T		
U		
V		
W		
X		
Y		
Z		
a		
b		
c		
d		
e		
f		
h		
j		
k		
m		
n		RST
p		CONTROL BUS
r		END SCAN
s		SS
t		TS1
u		EOR
v		ROT
w		TS2
x		GND

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