Lawrence Berkeley Laboratory

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Engineering & Technical Services Division

Presented at the IEEE 1980 Nuclear Science Symposium,
Orlando, FL, November 5-7, 1980; and to be published in
IEEE Transactions on Nuclear Science

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A MICROCOMPUTER

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October 1980

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A TIME PROJECTION CHAMBER DIGITIZER*
TEST SYSTEM USING A MICROCOMPUTER

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Abstract

A small computer system for testing digitizers, control cards, and backplanes was developed at the Lawrence Berkeley Lab to be used in the Time Projection Chamber (TPC) Detector. The objective of this development was to provide a low cost test system for fast debugging, maintenance, a quality control by outside vendors who fabricated these units as well as Laboratory personnel. When the system was delivered to the vendors, it consisted of the computer programming and documentation necessary to do a complete checkout of approximately 20,000 signal channels. To obtain this low cost system (totaling \$1400) a commercial microcomputer with 16K of memory and a printer (40 characters per line, 30 characters per second) were selected. This paper describes the overall test system and programming features including the linking capabilities of the "debug" program. It, also, describes the various interfacing techniques that were used to obtain hardcopies.

Introduction

This test system was designed to check the Charge-Coupled Device (CCD) digitizing electronics for the Time Projection Chamber (TPC) Detector.¹ However, its present use has been expanded to include testing and debugging Pole-Tip and Cylindrical Calorimeter digitizers and control boards, including their respective backplanes. And due to its flexibility, the system will become part of a facilities operation for maintaining the above electronics for the PEP-4 experiment.²

Design Considerations

The system was designed to meet a number of criteria. First, it had to be low cost because the unit would be shipped to an off-site vendor. The vendor would use the system to perform testing, fast debugging, and quality control on the digitizers and control modules. Essentially, the computer would be dedicated to the fabrication process and not readily available for use by laboratory personnel. Since the vendor could be located far from the laboratory, the system also had to be reliable and easy to operate. Another requirement was that actual checkout of a board would not require a highly trained electronic technician, contrary to debugging a defective board. Lastly, the system had to be able to exercise every circuit to detect defective components in less than two minutes.

System Hardware

Figure 1 shows the hardware part of the system with the computer communicating with the test units and power supply via the interface. The interface unit is connected to the memory Extension port which contains all of the signals from the 6502 Microprocessor. Hardcopy is obtained from a printer (40 characters per line, 300 baud) connected to the IEEE 488 Interface Port.³ Hardcopy may also be obtained from other printers and teletype units capable of operating from the IEEE-488 Bus. Programs are loaded into the computer via a tape cassette units connected to one of two available ports.

When purchased the Commodore PET† microcomputer contained 16K of memory; however, it has been expanded to 32K at a cost of \$80.00. For an additional \$48.00 an IC called "TOOLKIT"† was purchased and installed which added ten new BASIC commands. The computer has five different input/output ports: Memory Expansion, parallel User's Port, 1st and 2nd Cassette Interfaces, and IEEE-488 Interface.

System Software

The System's software is composed of two programs called "Digitizer Test" and "Debug" that are written in BASIC and the 6502 Assembly Language. These programs are written to maximize the chances of detecting and pinpointing bad components on digitizers and control boards.

Execution of the Digitizer Test program begins by turning on the voltages and checking the currents of a newly fabricated digitizer card. If any current is not within the expected values, the test is stopped after turning off the voltages and printing an error message of actual and expected current values. Passing the power check causes the program to begin the Lower Limit RAM (LLRAM) test.

The LLRAM test program writes two test patterns into the Lower Limit RAM to exercise each bit at each subaddress in the LLRAM. If the patterns read back from the LLRAM are not identical to the patterns written into the LLRAM, a message "FAILED LLRAM TEST" appears on the printed sheet. The patterns read back, then, should be compared with the test patterns sent to the LLRAM. Figures 2 and 3 are the two different test patterns used to test the LLRAM. Successful completion of both the current and the LLRAM tests is mandatory before beginning the five digitization tests.

*This work was supported by the Division of Physical Research of the U.S. Department of Energy under contract No. W-7405-ENG-48.

† Reference to a company or product name does not imply approval or recommendation of the product by the University of California or the U.S. Department of Energy to the exclusion of others that may be suitable.

Hardware setup of TPC Digitizer Test System

Figure 1.

TEST PATTERN #1 (LLRAM)								
SUBADDRESS	LL7	LL6	LL5	LL4	LL3	LL2	LL1	LL0
0	1	0	1	0	1	0	1	0
1	0	1	0	1	0	1	0	1
2	0	0	0	0	0	0	0	0
3	1	0	1	0	1	0	1	0
4	0	1	0	1	0	1	0	1
5	0	0	0	0	0	0	0	0
6	1	0	1	0	1	0	1	0
7	0	1	0	1	0	1	0	1
8	0	0	0	0	0	0	0	0
9	1	0	1	0	1	0	1	0
10	0	1	0	1	0	1	0	1
11	0	0	0	0	0	0	0	0
12	1	0	1	0	1	0	1	0
13	0	1	0	1	0	1	0	1
14	0	0	0	0	0	0	0	0
15	1	0	1	0	1	0	1	0

Fig. 2

TEST PATTERN #2 (LLRAM)								
SUBADDRESS	LL7	LL6	LL5	LL4	LL3	LL2	LL1	LL0
0	0	1	0	1	0	1	0	1
1	1	0	1	0	1	0	1	0
2	1	1	1	1	1	1	1	1
3	0	1	0	1	0	1	0	1
4	1	0	1	0	1	0	1	0
5	1	1	1	1	1	1	1	1
6	0	1	0	1	0	1	0	1
7	1	0	1	0	1	0	1	0
8	1	1	1	1	1	1	1	1
9	0	1	0	1	0	1	0	1
10	1	0	1	0	1	0	1	0
11	1	1	1	1	1	1	1	1
12	0	1	0	1	0	1	0	1
13	1	0	1	0	1	0	1	0
14	1	1	1	1	1	1	1	1
15	0	1	0	1	0	1	0	1

Fig. 3

The next five tests were designed to check the digitization portion of the digitizer card by applying a voltage level (0V-6V) to each of 16 CCD channel inputs. A card may pass one or more of the tests but fail the others. Should it fail any of the tests, a message describing the test number and the information read back (received) from the digitizer is printed out for analysis. As the card passes each test, a message will be printed announcing the test number passed.

Tests #1 and #2 check the upper (511) and lower (15) digitized values, respectively. Tests #3 and #4 were designed to check the ability of the digitizers LLRAM to act as discriminators against the 16 CCD inputs. For Tests #3 and #4 the LLRAM is set to the value 127. For test #3 a signal level of 140 units is applied to the odd numbered CCD inputs, and a signal level of 115 units is applied to the even numbered CCD inputs. Only the odd numbered channels should have the value 140 ± 5 , while the even numbered channels should have the value 0. In test #4 the signal levels are reversed whereby a signal level of about 115 units is applied to the odd numbered CCD inputs, and a signal level of 140 units is applied to the even numbered CCD inputs. Now only the even numbered channels should have a value of 140 ± 5 and the odd channels should have the value 0.

The correct operation of the tests will result in printed messages "PASSED DIGITIZATION TEST No. 1,2,3, 4, and 5", respectively. Failure to pass any of the tests will be so indicated, and the improper results will be printed out which should be compared with the respective test patterns shown in Figures 4,5,6, and 7.

Digitization Test #1

DPR,SA,DATA	1	0	511
DPR,SA,DATA	1	1	511
DPR,SA,DATA	1	2	511
. . .	.	.	subaddresses
. . .	.	.	3 thru 12 are
. . .	.	.	implied here
DPR,SA,DATA	1	13	511
DPR,SA,DATA	1	14	511
DPR,SA,DATA	1	15	511

Fig. 4

Digitization Test #2

DPR,SA,DATA	1	0	$*15 \pm 5$
DPR,SA,DATA	1	1	15 ± 5
DPR,SA,DATA	1	2	15 ± 5
DPR,SA,DATA	1	3	15 ± 5
DPR,SA,DATA	1	4	15 ± 5
DPR,SA,DATA	1	5	15 ± 5
DPR,SA,DATA	1	6	15 ± 5
DPR,SA,DATA	1	7	15 ± 5
DPR,SA,DATA	1	8	15 ± 5
DPR,SA,DATA	1	9	15 ± 5
DPR,SA,DATA	1	10	15 ± 5
DPR,SA,DATA	1	11	15 ± 5
DPR,SA,DATA	1	12	15 ± 5
DPR,SA,DATA	1	13	15 ± 5
DPR,SA,DATA	1	14	15 ± 5
DPR,SA,DATA	1	15	15 ± 5

*These DATA values will fluctuate around a value of 15 units with typical statistical fluctuations for the different subaddresses which is expected in a digitizer of the type being tested.

Fig. 5

DIGITIZATION TEST #3 AND #4

Digitization Test #3

DPR,SA,DATA	1	1	** 140 ± 5
DPR,SA,DATA	1	3	140 ± 5
DPR,SA,DATA	1	5	140 ± 5
DPR,SA,DATA	1	7	140 ± 5
DPR,SA,DATA	1	9	140 ± 5
DPR,SA,DATA	1	11	140 ± 5
DPR,SA,DATA	1	13	140 ± 5
DPR,SA,DATA	1	15	140 ± 5
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0

Fig. 6

Digitization Test #4

DPR,SA,DATA	1	0	** 140 ± 5
DPR,SA,DATA	1	2	140 ± 5
DPR,SA,DATA	1	4	140 ± 5
DPR,SA,DATA	1	6	140 ± 5
DPR,SA,DATA	1	8	140 ± 5
DPR,SA,DATA	1	10	140 ± 5
DPR,SA,DATA	1	12	140 ± 5
DPR,SA,DATA	1	14	140 ± 5
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0
DPR,SA,DATA	0	0	0

**The actual number printed may be typical numbers such as; 141, 137, 140, 139, etc, in some such random manner.

Fig. 7

Test #5 introduces a half level amplitude (2.5V) signal to all CCD signal inputs to the digitizer card. The LLRAM is set to inhibit all data from being stored in the buffer memory. Should any information whatsoever be recorded, the data pattern will be printed so that it can be compared with the correct pattern to determine the faulty circuit/component.

TPC DIGITIZER BOARD DEBUG PROGRAM

The Digitizer Board Debug Program is a routine that runs on the PET connected to the board test stand. It is useful in debugging a board that has failed the test routine. The Debug Program allows the user to link together in arbitrary order a number of subroutines that perform various operations on the digitizer board. This allows one to set

up a set of operations that can be used to check a suspected problem on the board. The sequence of commands can be executed once, or repeated on demand or repeated continuously.

The Debug Program is loaded from the tape unit in the usual way. When the program is "RUN", it starts with an announcement and gives the operator the choice of skipping a print out of instructions.

The program then asks for a command string. The command string is entered from the keyboard and is terminated by a carriage return. The format of the command string is

COMMAND/COMMAND/...../COMMAND

The program checks for validity of the commands. If it cannot interpret the command it prints an error message as well as the command string that it has and waits for corrections. These corrections may be made by retyping the entire string or by using the cursor editing of the PET to correct the string.

When the string is correct the program sets up the subroutine linkage and executes the string. At the completion of the string it stops, asking for the operator to enter R or C. An R will repeat the string. Typing a C allows a new command string to be entered. Note, if the last command in the string is "REPT" (see next section) the string does not complete, since it repeats at that point. An "S" typed during this execution will stop the string at the end of the next pass and the operator will be presented with the usual R/C choice. A detailed description of each of the commands follows.

Commands

Note: the slash "/" is not required at the end of the string.

POWER:

ON/ Turns on the power supply and issues a Reset.

OFF/ Turns off power supply and after 1 sec. silences the alarm.

RDI/ Reads power supply current.

PTI/ Does RDI/ and then prints results on the screen.

LOWER LEVEL RAM:

LDLL/(sub address)/(value)
Loads the LLRAM at the sub address with the value specified. If the address is greater than 15 it loads all 16 addresses (0 thru 15).

RDLL/(sub address)
Reads the value in the LLRAM at the specified address. If the address is greater than 15 it reads all addresses (0 thru 15).

PTLL/(sub address)
Does RDLL/(sub address) and prints the results on the screen.

DIGITAL TO ANALOG CONVERTER (DAC) FOR INPUT TO BOARD

SDAC/(value)

Sets the DAC to the value given. If the value is greater than 255 it sets the input to the DAC to its high range value by setting the input to the DAC to 255 and the over range flag to the DAC to 1. All channels then should digitize to 511.

PTDAC/ Reads and prints on the screen the input to the DAC as well as the status of the over range flag and odd/even percent settings.

SEV/(%) Sets the even numbered inputs to either 100% or 80% of the DAC setting.

SOD/(%) Sets the odd numbered inputs to either 100% or 80% of the DAC setting.

DIGITIZER COMMAND

DIG/ Initiates a digitize cycle.

RDDA/ Reads the data from the 16 channels.

PTDA/ Does a RDDA/ and then prints the results on the screen.

DRDIG/ Generates two digitizing cycles. But reorder of 2nd cycle is suppressed leaving data from 1st cycle in Data Rams and data from 2nd cycle in Data Registers.

DRDIGPT/ Does a RDDA and prints results on screen from both digitizing cycles.

DRDIGFR/ Generates two digitizing cycles but does not suppress reordering of data from 2nd cycle.

CONTROL COMMANDS

REPT/ This command sends the program back to the beginning of the string. It continues repetition of the string until the operator types an "S". It then stops the command sequence in the usual way at the end of the next pass.

M/ Prints a menu of the commands on the screen with a very brief explanation of each.

MP/ Same as M/ except prints on the Printer. (Note, at the end of this print, the operator must type any key to continue. This message appears on the printer and can be missed).

COMMAND DEFAULTS

1. On initialization, the DAC=0 with over range flag set to 0 with even and odd each set to 100%.
2. When a command that requires a numeric argument is the last command of a string, and if the argument is not given the program assumes zero for the value. For example:

LDLL/16 loads all LLRAM subaddresses with zero while LDLL loads only subaddress 0 with 0.

EXAMPLES OF COMMAND STRINGS

ON/PTI/OFF Turns on power supply, reads and
 prints the power supply current and
 turns it off.

ON/LDLL/16/0 Turns on power, sets all LLRAM loca-
 tions to zero.

DIG/REPT Starts the digitization cycle over
 and over until an S is typed.

SDAC/128 Sets the input to the digitizer at
 approx. 2.5 volts.

DIG/PTDA Digitizes, reads and prints the data.

Acknowledgment

The author wishes to express his sincere thanks to the four persons who participated in this project. For defining system test requirements Mich Nakamura provided valuable advice. Professor Leroy Kerth helped tremendously with the software development, especially with the Debug routine. To Stephen Smiriga for his expertise in the design of the interface board to the computer. And, lastly, to Joe Ortiz for assembling and testing the power unit and associated control circuitry.

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