The Unofficial AMPLEX Owner's Manual *

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Purpose

The AMPLEX chip is an AMplifying multipLEXing, CMOS technology device. It is an analog signal processor, designed at CERN¹ for use with silicon microstrip detectors. However, its application is not limited to conventional microstrips and it is being used in various detector systems. AMPLEX design goals included modest power consumption and reasonable speed.

The main drawback of the chip seems to be a lack of documentation. This report will attempt to fill this void by providing a summary of the properties of the AMPLEX chip, a brief synopsis of how it functions, and most importantly an explanation of how to make it operate in a practical circuit. The information in this paper pertains to the application of the AMPLEX chip to microstrip detectors for the electron beam at Brookhaven National Laboratory's Accelerator Test Facility. Detector design was carried out in the Instrumentation Division. Details of the driving circuit and some information on the inner workings of the AMPLEX chip came directly from CERN² and from the paper by E. Beuville et al³.

The author is in no way connected with CERN, nor is he attempting to promote the AMPLEX chip; he is merely interested in making the chip work and in making it easier for others who might wish the same. Some knowledge of the interior of the chip will help in understanding the process of amplifying and shaping signals, so that is where this paper begins.

¹ Jarron, Pierre and Erik Heijne

² Jarron, Pierre and Erik Heijne, "AMPLEX16 - CERN UA2: Some Practical Details", CERN ECP Division, CH-1211, Geneva 23.

³ Beuville, Eric, Kurt Borer, Enrico Chesi, Erik H. M. Heijne, Pierre Jarron, Bohdan Lisowski and Simon Singh, "AMPLEX, a Low-Noise, Low-Power Analog CMOS Signal Processor for Multi-Element Silicon Particle Detectors", Nuclear Instrumentation and Methods in Physics Research, A288 (1990), pp. 157-167.

Figure 1: AMPLEX Conceptual Schematic

Commonly Used Symbols

Charge Amplifier

C_f	Feedback Capacitor
I_{POTA}	Bias Current
POTA	Positive Operational Transconductance Amplifier
R_f	Feedback Resistor
V_{Gf}	Gate Feedback Voltage (aka V_{BT})
V_{BT}	Bias Transistor Voltage (aka V_{Gf})

Shaping Amplifier

C_{diff}	Differentiation Capacitor
C_{fs}	Feedback Capacitor
I_{NOTA}	Bias Current
NOTA	Negative Operational Transconductance Amplifier
R_{fs}	Feedback Resistor

Track & Hold

C_h	Hold Capacitor
SWH	Hold Switch (Transistor)

Multiplexer

MUX	Multiplex
SWM	Multiplexer Switch (Transistor)

Table 1: Commonly Used Symbols

What's Inside?

We will analyze the AMPLEX by following a signal from its origin through the various components. Until the final multiplexing stage, all of the channels are comprised of duplicate circuits. The first stage is the charge amplifier (*See Figure 1*), or Positive Operational Transconductance Amplifier (POTA). In general, a detector deposits charge on the gate of the first transistor. The capacitor, C_f , makes the amplifier into an integrator. If the input signal to the amplifier is a current spike corresponding to a detected event, the integral of the spike is a step. In our case, the spike is not ideal, so the integral is more sigmoid in nature. The other component in the feedback loop is a transistor that functions as a feedback resistor. The value of the resistance is variable, based upon bias voltage applied to the gate. The recommended voltage is -4 V (more on this later) which corresponds to a feedback resistance of about $100\text{ M}\Omega$. The other input parameter is the bias current, I_{B-POTA} (more on this later, also).

The second stage is the conjugate of the first stage, namely a Negative Operational Transconductance Amplifier (NOTA), with bias current noted at I_{B-NOTA} . In this stage, both the feedback resistance and capacitance are fixed values of R_{fs} and C_{fs} , respectively. More interesting to operation is the differentiating capacitor, C_{diff} . Through differentiation, the signal is transformed back into a pulse, so that the net effect is one of shaping. The initial impulse is projected towards a gaussian and is positively peaked when the input spike is a positive one. Specifically, the peaking time is approximately 500-700 ns.

These stages are amplifiers, as well, so there is a net gain in signal strength. The POTA stage converts charge to voltage. The output voltage is directly proportional to the collected charge, q , and inversely proportional to the feedback capacitance. The NOTA stage has a gain factor equal to the ratio of the differentiation capacitance to the feedback capacitance. The final form of the output voltage is:

$$V = \frac{q}{C_f} \times \frac{C_{diff}}{C_{fs}} \approx \frac{q}{1\text{pF}} \times \frac{6\text{pF}}{.6\text{pF}} \times \frac{\text{mV} \cdot \text{pF}}{\text{fC}} \approx 10\ q \ \frac{\text{mV}}{\text{fC}}$$

The actual gain given by CERN² is 5 mV/fC , which is close to our approximation. Much of this discrepancy can be explained by losses, especially by those in the unity gain buffer. The maximum output voltage for any given input signal is about 350 mV, which translates into 70 fC as the saturation input level, or, more precisely, the edge of the linear regime of the response curve. To keep below the saturation level with a factor of safety, all circuit designs should use about 50 fC as the saturation level. This figure corresponds to 312,500 electrons per pulse.

The pulse which exits the shaping amplifier is relatively short, with an occupation time of $2 \mu s^4$. The characteristic that is important to us is the pulse height, rather than the duration. Since the sixteen output channels will be multiplexed (read out in sequential order), the pulse height must be stored prior to readout. This component is called track & hold, and is the third stage in the AMPLEX chip. The system will begin its operation in track mode and, as the signal grows, the charge that is stored on the hold capacitor, C_h , will increase. While the pulse increases with time (before the 500 ns peak time) a signal is introduced at the hold switch. The signal is connected to the gate of a transistor, which turns the transistor off, i.e. opens the switch. The hold capacitor will now "store" the previous value (the peak) through a unity gain buffer.

At this point, all sixteen channels are holding a given voltage, depending on how much charge was collected on each line. The multiplexing stage introduces a clock pulse that sequentially closes each switch into the analog output. One might envision the multiplexing stage as a railroad yard with sixteen side tracks onto the main line. Each storage track holds coal cars, filled to a prescribed level. One by one, the cars are added until a complete train is formed. The amount of coal in each car is directly related to the amount of charge collected by each line.

It is important to note that the hold signal must be provided throughout the entire multiplexing operation. Once the multiplexing has been completed, the hold signal is removed and the AMPLEX will return to track mode. Also, a clear signal (sometimes called a reset signal) is provided to reset all registers so that the next pulse starts the counters at one.

This concludes the portion of the paper concerned with the internal workings of the AMPLEX chip. The previous material is relatively easy to locate, while the remainder of this report deals with the more elusive and less understood process of implementing the AMPLEX chip, as well as the engineering problems one might encounter along the way.

⁴ Puiz, F. "Operation of AMPLEX with DRAMS and control card." October 28, 1989.

Pin Layout

Now that we have discussed the actual components inside the AMPLEX chip, we can move on to a topic which is more relevant to applications: connecting the pins to a circuit board. The figure below is a top view of the chip, with each pin numbered. The following page contains a list with each pin and its name.

Figure 2. Pin Layout

Pin	Name	Description
1	Sub.	Substrate
2	IN1	Input 1
3	IN2	Input 2
4	IN3	Input 3
5	IN4	Input 4
6	IN5	Input 5
7	IN6	Input 6
8	IN7	Input 7
9	IN8	Input 8
10	IN9	Input 9
11	IN10	Input 10
12	IN11	Input 11
13	IN12	Input 12
14	IN13	Input 13
15	IN14	Input 14
16	IN15	Input 15
17	IN16	Input 16
18	V _{SS}	Negative Voltage (Analog)
19	TI	Test all Inputs
20	V _{B1}	Test Bias Voltage
21	I _{B-POTA}	Bias Current (Charge Amplifier)
22	CL IN	Clock In
23	CL OUT	Clock Out
24	CLR	Clear
25	OUT MUX	Multiplex Output
26	NC	No Connection
27	NC	No Connection
28	GND _{DIG}	Ground (Digital)
29	V _{SS-DIG}	Negative Voltage (Digital)
30	V _{DD-DIG}	Positive Voltage (Digital)
31	I _{B-NOTA}	Bias Current (Shaping Amplifier)
32	T/H	Track & Hold Signal
33	V _{BB}	Test Bias Voltage
34	V _{BT}	Bias Transistor Voltage
35	GND	Ground (Analog)
36	V _{DD}	Positive Voltage (Analog)

Table 2. Pin Names

Figure 3: Chip Wiring Diagram Schematic

More than Just a Pin Number

This discussion follows a pin-by-pin commentary of the schematic on the previous page, which outlines all of the electronics surrounding the AMPLEX chip. First we can tackle the easy pins: those numbered 2 through 17, which are inputs 1 through 16. Each pin should be connected either directly (DC coupled) or through a capacitor (AC coupled) to its respective silicon strip on the detector itself. The detector, which by now you have probably already designed, should be capable of functioning in a domain with a maximum of 400 nA of leakage current. Higher leakage current in a detector which is DC coupled will bias the input transistor to turn off and operation of the channel will fail. AC coupled detectors can operate independently of leakage current, however the Johnson noise will eventually limit the detector leakage current that can be tolerated.

Depending of the type of detector and the type of event, the input to each AMPLEX channel can vary over quite a wide range. In an earlier section, it was mentioned that a maximum height of the charge spike that can be handled is about 300,000 electrons, with some margin for error. If the experiment will produce more than this threshold, a current divider should be inserted before each AMPLEX input. As a rough estimate, the input impedance is about 3 k Ω . Therefore the signal attenuation into the AMPLEX would be on the order of the attenuation resistance divided by the total impedance. Remember, the AMPLEX chip was designed to relay information with regard to minimizing ionizing particles, and not to large currents of electrons. For example, an attenuating resistor of 300 Ω will cause the input current to be attenuated by a factor of eleven:

$$\frac{300\Omega}{300\Omega + 3k\Omega} = \frac{1}{11}$$

One must also consider the transient characteristics of such an element. If a resistor is added to the circuit with a capacitor, the time constant (the product of the resistance and the capacitance) must be greater than the time constant of the charge collector of the AMPLEX chip.

Next, we concentrate on the "useless" pins. These connections are of two types. Included in the first group are pins 26 and 27, which simply aren't used. The second group consists of pins 19, 20, and 33. The "Test All Inputs" connection is used for chip testing and not in actual applications, and may be grounded. V_{B1} and V_{BB} are most likely direct connections to bias voltages on various internal transistors. During testing, these nodes might be used to force transistors into operational states. For our purposes, we would like to isolate this variable; however, shunting it to ground would also force all bias voltages to zero, causing the AMPLEX to cease functioning. Rather, these pins should be connected to ground through a 10 μ F capacitor and a .1 μ F capacitor in parallel. The small capacitor filters out noise, while the larger capacitor serves as a low frequency filter.

There are also several sets of power and ground lines. Positive voltage (V_{DD}) is provided to the AMPLEX in two locations. The first is at the analog input, through a $100\ \Omega$ resistor. The other is through a $220\ \Omega$ resistor at the digital input. The analog input serves the amplifier stages, while the digital input serves the multiplexing stage. The negative voltage (V_{SS}) is wired in exactly the same fashion, and all inputs should have a filter capacitor of $.1\ \mu F$. Both analog and digital grounds are connected, obviously, to ground. Standard CMOS operation suggests that the substrate plate be connected to the lowest available potential, namely V_{SS} .

To insure proper feedback resistance in the charge amplifier, the feedback resistor (transistor) at pin 24 requires at steady voltage of $-.4\ V$. The easiest way to ensure this voltage is to set up a simple voltage divider between ground and V_{SS} . This may be achieved with $51\ k\Omega$ and $4.7\ k\Omega$ resistors, for example. The use of large resistances ensures a minimal steady state current flow through the components and reduces heat generation. Filtering capacitors are needed at V_{BT} , also. The topic of power consumption and heat generation is a very interesting one. This aspect is particularly important to any application that might be used in vacuum, though to our knowledge, no one has yet built an AMPLEX system to be run in vacuum. The overall current flow into the chip is very small, since the input is a high impedance FET gate. In fact, the chip itself uses only one to two milliwatts per channel.

It is recommended that the bias currents into the amplification stages be $50\ \mu A$ and $10\ \mu A$ for the charge and shaping amplifiers, respectively. To achieve a steady current, a resistor is connected between the bias input and the already filtered voltages. The charge amplifier is a NOTA and requires positive current from the V_{DD} node through a $560\ k\Omega$ resistor, while the shaping amplifier is a POTA and requires negative current from the V_{SS} node through a $220\ k\Omega$ resistor. Here, too, filter capacitors should be used. It has become local practice to use multilayers on the motherboard. By placing power planes between ground planes, the PC board can be used as a filtering capacitor.

Finally, the multiplexed output, the track & hold signal, and all three timing signals (clock in, clock out, and clear) deserve separate attention, and are discussed in subsequent sections.

System Overview

Along with the AMPLEX chip, CERN has developed two CAMAC cards that may be used to control and interpret the chip. The DRAMS serves as the computer interface for the analog signals from AMPLEX chip. The acronym DRAMS stands for Digital Readout for Analog Multiplex Signals. The control card provides many of the timing signals used to clock the system. The task of interfacing all of this electronic equipment to a computer is not trivial. Currently, there is a CERN report⁵ and computer code that is available with the cards. This report includes a detailed description of the interface between the CAMAC and the computer and is beyond the scope of this report.

There are still several control elements that are required, in addition to the CAMAC cards. These small circuits are usually designed into the AMPLEX motherboard. Below is a block diagram that summarizes all of the required components.

Figure 4: System Block Diagram

⁵Chesi, E., P. Martinengo, and A. Racz. "DRAMS: Digital read-out for Analog Multiplexed Signals." March 6, 1990.

Timing Considerations

You have been given a bit of information regarding the timing considerations for the AMPLEX chip from the discussion of the multiplexing stage. However, there are more intricacies that need to be addressed in order to operate the chip successfully. First, one must examine the control card, as shown in *Figure 5*.

Figure 5: AMPLEX Control Card

The Control Card is a card with various inputs, outputs, and controls. First we should examine the three inputs:

Start Read	This is the trigger that starts the entire process, the origin of which is the event trigger that controls the operation of the experiment.
Conversion Pulses	Conversion pulses are used by the DRAMS module itself. Even among experienced users, this function is and remains obscure. My guess is that input could be used as a forced clock for the control card.
Reset	The signal that all ADC has been accomplished.

The control card also outputs four signals:

AMPLEX Clock	This clock is the master clock for the AMPLEX chip. At its present location, it is provided at NIM logic levels (0 V for zero state and -0.8 V for one state). The CMOS technology AMPLEX chip requires logic levels of 0 V and -5 V. Clearly, a level shift will need to be performed. See "Correcting the Clock and Clear".
AMPLEX Clear	This is the clear signal to reset all of the shift registers in the AMPLEX. Again, this signal requires a logic level shift.
Conversion Pulses	The DRAMS module needs its own "clock" to know when to sample the analog output from the AMPLEX chip. These pulses, generated at TTL levels, are used for this purpose.
Busy	While conversion is taking place, a busy signal is provided for computer control input. There is also a busy light.

Finally, the module has two trimpots to adjust:

Multiplexer Frequency	This adjustment controls the frequency at which the AMPLEX will multiplex its channels. The maximum frequency is 2 MHz.
Clock/Conversion Delay	The DRAMS module must see the conversion pulses at the same time as it receives the AMPLEX multiplexed readout. Since the AMPLEX chip might be several meters from the Control Card, while the DRAM module is usually mounted next to the Control Card, an artificial delay to negate the effect of long cables can be introduced.

Correcting the Clock and the Clear

There are two outputs from the Control Card that go directly to the AMPLEX chip: the clock and clear pulses. The Control Card produces these pulses at the appropriate times, but not at the appropriate levels. The standard output is called NIM Fast logic while the AMPLEX chip itself is looking for pulses in shifted CMOS levels. The NIM level has the advantage of being low voltage, and hence, has a quick rise time. So, what we need is a black box that converts NIM to CMOS (*Figure 6*).

Figure 6: NIM to CMOS Concept

Figure 7 contains a schematic of the circuit used for level shifting. The NIM level signal enters from the right side, through the connector, which has a terminator to ground as one would expect. The next stage is comprised of three diodes, one of which is tied down to ground with the other two connected serially up to ground. This simple configuration is protection for the circuit. If any signal other than NIM is given at the input, i.e. greater than .7 V or less than -1.4 V, then the current is shunted to ground. Also included is a 100Ω resistor that acts as a current limiter in the case of an improper input signal.

The important stage is the transistor stage. The PNP transistor is normally off, when the input voltage is zero. If the transistor is off, then the current through the collector resistor is zero, and the voltage at the collector is that of V_{SS} . The emitter is tied to ground through a Shottkey diode, which has an intrinsic voltage of about .3 V. Therefore if the input voltage falls below -.3 V (-.8 V of NIM logic is more than ample), then the transistor turns on. At this point, approximately 3 mA of current drives the collector to ground.

A model for use with the circuit analysis program PSPICE is included in *Table 3*, with its output in *Figure 8*. The signal is inverted and noise and delay have been added. It is easy to square the wave off while inverting it by running the signal through an inverter. However, the inverter must be connected to ground on the high side and to V_{SS} at the negative terminal, instead of to V_{DD} and to ground, as usual.

Figure 7: Clear or Clock Level Shifter

CLRCLOCK.CIR: Clear or Clock Level Shifter

```

Rin      IN      B      100

Q        OUT     B      E      Q2N3640
Ra       E       VDD     1.2k
Rb       OUT     VSS     1.8k
D1       E       0       MBD201

Vin      IN      0       PULSE (0V -0.8V 50ns 1ps 1ps 50ns 200ns)

Vdd      VDD     0       DC 5.0
Vss      0       VSS     DC 5.0

.tran     1ns     200ns

.probe

.model    Q2N3640      PNP(Is=545.6E-18 Xti=3 Eg=1.11 Vaf=100 Bf=59.22
+                      Ne=1.5 Ise=0 Ikf=50m Xtb=1.5 Br=1.438 Nc=2 Isc=0 Ikr=0
+                      Rc=3.75 Cjc=2.77p Mjc=.1416 Vjc=.75 Fc=.5 Cje=2.65p
+                      Mje=.3083 Vje=.75 Tj=4.123n Tf=118.5p Itf=.5 Vtf=3 Xtf=6
+                      Rb=10)

.model    MBD201       D(Is=1.684p Rs=.1 Ikf=0 N=1 Xti=3 Eg=1.11 Cjo=2.034p
+                      M=.2771 Vj=.75 Fc=.5 Isr=4.301n Nr=2 Bv=20 Ibv=10u)

```

Table 3: Clear or Clock SPICE Model

Clear or Clock Level Shifter

Figure 8: Clear or Clock Simulation

Creating the Track & Hold

The track & hold procedure for the AMPLEX chip is, quite possibly, the most difficult to fully understand. In general, the system should be in track mode until the event trigger occurs. At this point the hold signal should be given so that the AMPLEX chip will switch from tracking the various values of the channels (discharging a capacitor when the voltage falls) to hold a peak value (restricting the ability of a capacitor to discharge).

The track & hold is actually the gate of a transistor inside the AMPLEX, so the voltage at this point is rather critical. To ensure proper switching between modes, we must adjust this voltage so that whenever the voltage is above the signal voltage the system will track and whenever the voltage is lower than the signal, then the system will hold the signal at the peak value. In other words, we would like a signal that switches from V_{SS} to V_{DD} , in as short of a time as possible. Since all control for this trigger comes from circuitry that the user must build and not from the control card itself, it is beneficial to use NIM logic levels. So, again we need a level shifter, but in this case the waveform looks like the following:

Figure 9: NIM to Rail Concept

Figure 10 contains a design for the track & hold circuit. As with the clock or clear level shifters, the signal enters from the right, through some simple protection devices. The first stage of the circuit is similar to the clock or clear level shifters, except for some resistor values. In review, zero volts on input gives a bottom rail output and negative voltage yields an output voltage around zero. The difference in resistor values for this circuit, however, ensures that this latter voltage is slightly positive.

Next, this signal enters a second transistor stage, of NPN type. The Shottkey diode holds the base voltage above the collector by about 0.3 volts. When a negative pulse comes in from the first stage, the transistor switches to the off state so that the collector is pulled to the top rail of V_{DD} . When a potential greater than the Shottkey voltage is provided at the base, the transistor will switch to an on state, causing the collector voltage to fall. The collector will not fall all of the way to V_{SS} , since there will be some residual voltage across the transistor.

A spice model for this circuit is provided in *Table 4* and its simulation in *Figure 11*. Notice on the figure that the switching time is only about 20 ns on the falling edge, while the rising edge lasts for almost 50 ns. Also notice that the bottom rail is approximately -4.7 V, as expected. The issue of rail voltage for the track & hold circuit is far from a conclusion. The rail voltages play an important role in holding the correct voltage for each channel. For this purpose, it is a good idea to allow the rail to be connected to either the standard plus and minus five volts supply lines for the AMPLEX chip or to be powered by some external, variable source. Remember that adjusting supply voltages may shift quiescent operating points for the transistors and may also require resistor value tuning.

Contrary to the clock and clear level shifters, the signal is correctly polarized so one does not need to run it through an inverter. Without the ability to use an inverter, however, the signal will retain its slow rise and fall edges. Even though it is not known exactly when the level shifter will switch from track to hold and then back again, this should not be a problem. Timing will need to be calibrated to an optimal output, primarily through trial and error, using delay modules in conjunction with the event trigger signal.

Figure 10: Track & Hold Level Shifter

TRAKHOLD.CIR: Track & Hold Level Shifter

```

Rin      IN      B1      100

Q1       B2      B1      E1      Q2N3640
R1a      E1      VDD      1.0k
R1b      B2      VSS      680
D1       E1      0        MBD201

Q2       OUT     B2      VSS     Q2N3646
R2       OUT     VDD      470
D2       B2      OUT     MBD201

Vin      IN      0        PULSE (0V -0.8V 50ns 1ps 1ps 50ns 200ns)

Vdd      VDD     0        DC 5.0
Vss      0       VSS     DC 5.0

.tran     1ns     20ns

.probe

.model   Q2N3640      PNP(Is=545.6E-18 Xti=3 Eg=1.11 Vaf=100 Bf=59.22
+                      Ne=1.5 Ise=0 Ikf=50m Xtb=1.5 Br=1.438 Nc=2 Isc=0 Ikr=0
+                      Rc=3.75 Cjc=2.77p Mjc=.1416 Vjc=.75 Fc=.5 Cje=2.65p
+                      Mje=.3083 Vje=.75 Tr=4.123n Tf=118.5p Itf=.5 Vtf=3 Xtf=6
+                      Rb=10)

.model   Q2N3646      NPN(Is=1.017f Xti=3 Eg=1.11 Vaf=100 Bf=85.99 Ne=2.048
+                      Ise=34.11p Ikf=.2617 Xtb=1.5 Br=3.587 Nc=2 Isc=0 Ikr=0
+                      Rc=1.75 Cjc=4.256p Mjc=.1053 Vjc=.75 Fc=.5 Cje=8.359p
+                      Mje=.3504 Vje=.75 Tr=5.32n Tf=289.3p Itf=.35 Vtf=5 Xtf=2
+                      Rb=10)

.model   MBD201       D(Is=1.684p Rs=.1 Ikf=0 N=1 Xti=3 Eg=1.11 Cjo=2.034p
+                      M=.2771 Vj=.75 Fc=.5 Isr=4.301n Nr=2 Bv=20 Ibv=10u)

```

Table 4: Track & Hold SPICE Model

Track & Hold Level Shifter

Figure 11: Track & Hold Simulation

The Output Signal

With each AMPLEX chip sending an output synchronous with the clock pulses, we need a method to combine all of the signals into a single analog output line. This task is accomplished most easily with a summing amplifier. The feedback resistor on the amplifier is taken as $33\text{ k}\Omega$, while each leg of the AMPLEX output is fed through $22\text{ k}\Omega$. Also included in the feedback is a voltage divider in parallel with a capacitor. The function of the capacitor is to filter out any clock noise. This capacitance might range from one to a hundred picofarads, depending on the clock speed. To first order, we can determine the gain of such a device by multiplying the two gains together:

$$A = \frac{33\text{ k}\Omega}{22\text{ k}\Omega} \times \frac{12\text{ k}\Omega}{3.3\text{ k}\Omega} \approx 5\frac{1}{2}$$

The circuit developed is shown in *Figure 12*, followed by its SPICE code in *Table 5*, and output from the simulation run in *Figure 13*. By examining the plot, two facts become evident. First, we see that the linear regime of operation covers the range from plus to minus 350 mV, exactly the calculated saturation level of the AMPLEX output. The second point concerns the true gain of the circuit. The negative slope denotes an inverting configuration, as expected, and the slope of the line is approximately $7\frac{1}{2}$, which is not far from the above approximation.

Figure 12: Output Amplifier

OUTPUT.CIR: Output Amplifier

```

Rin      IN      INV      22k

Rf1      INV     F        33k
Rf2      F       OUT     12k
Rf3      F       0       3.3k
Cf       F       OUT     40p

R        NONINV   0       18k
C        NONINV   0       10u

X1       NONINV   INV     VDD  VSS  OUT  LF356/LT

Vin      IN      0

Vdd      VDD     0       DC 5.0
Vss      0       VSS     DC 5.0

.dc      lin     Vin     -500m 500m 10m

.probe

.include lintech.lib

```

Tabel 5: Output Amplifier SPICE Model

Figure 13: Output Amplifier Simulation

Figure 14: Complete Circuit

Putting the Pieces Together

Now that we have discussed all of the separate controlling circuits for the AMPLEX chip, we can now consider connecting the circuits together with more than one chip. In fact there are very few detectors that have only 16 channels, so daisy chaining AMPLEX chips is a necessity.

Figure 14 contains a schematic for using two or more chips. Each chip uses its own sources for bias currents, supply voltages, and bias voltages as well as has its own filtering capacitors located as close as possible to the chip itself. The controlling circuits are shared among all chips, as long as that number is no more than a dozen or so. Some control lines are shared via a common bus. Lines of this type include the clear signal and the track & hold signals. The output signal from each chip is fed through an individual resistor before entering the line to the summing amplifier. The clock signal is fed serially into the AMPLEX chips, not in parallel. So, the clock signal enters the first AMPLEX at the "clock in" pin. The output from the "clock out" pin is fed into the "clock in" on the second chip, and so on. In this manner, a chain of AMPLEX chips will function as one giant multiplexer chip, without requiring any supplemental equipment.

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END

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