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**ANALYSIS AND EVALUATION IN THE PRODUCTION PROCESS AND
EQUIPMENT AREA OF THE LOW-COST SOLAR ARRAY PROJECT**

Quarterly Report for Period October 1979—January 1980

By
M. Wolf

July 1980

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Solar Energy

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ANALYSIS AND EVALUATION
IN THE PRODUCTION PROCESS

AND EQUIPMENT AREA

OF THE

LOW-COST SOLAR ARRAY PROJECT

Contract No. NAS-7-100-954796

Quarterly Report October 1979 to January 1980
(DRD Line Item 6)

Subject: Metallization Pattern Design and Solar
Cell Efficiency.

July 1980

M. Wolf

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Summary

The solar cell metallization processes show a wide range of technical limitations, which influence solar cell performance. These limitations interact with the metallization pattern design, which is particularly critical for large square or round cells. To lay the basis for a process capability-cost-solar cell performance-value evaluation and trade-off study, the theoretical background of the metallization design-solar cell performance relationship was examined. The following conclusions have arisen therefrom.

1. Attention to the metallization structure becomes particularly important, as the cell size becomes larger. In fact, it has been shown that the voltage drop in a grid line, and consequently the power loss, is proportional to the square of the grid line length. Consequently, grid line lengths significantly above 2.5 cm should be avoided. As a result, large area - square or round - cells will need a periodic grid line structure with multiple bus lines.
2. Since the sheet resistance for each level in the hierarchy of components for the current paths (front layer, grid line, bus line) needs to be considerably below that of the preceding level, in order to be effective, the bus lines in such large area cells have to be of substantially greater thickness than obtainable by metal deposition processes, if shading is to be kept within reasonable bounds. Thus, the reinforcement of the bus lines by interconnectors or wires is the logical answer.

3. The power output losses due both to the voltage drop from series resistance and to the shadowing by the front metallization structure, can be held to acceptably low levels relatively easily. This level can be 5% of maximum power output for all of these losses combined for a 10cm x 10cm cell. This requires a relatively fine grid line system of, for instance, 1.54mm spacing (65 grid lines) and 25 μ m line width. This is well within the capabilities of several types of current metallization processes.

4. It has often been thought that the power dissipation in the resistive elements of a solar cell is not the only cause of loss of output power. A "mismatch" connected with the exponential current-voltage characteristic was expected to cause an additional power loss. It can be shown, however, that the energy dissipated in the series resistance element is actually by far the dominant energy loss. In fact, a rematching of the load to reduce the current from that giving maximum power in the "ideal" cell without series resistance, can result in a slightly greater power output than would correspond to the maximum power output of the ideal cell minus the energy dissipated in the series resistance.

5. The above finding indicates that the previous analyses which sought to minimize the power dissipation in the series resistance, have pursued a valid approach.

6. The end point voltage drops on metallization lines of constant width and on tapered lines ending in zero width are identical, if the total area shaded by these lines is equal. Thus, on first look, there would appear to be no advantage to the use of tapered grid lines. However, the voltage drop effective for the power dissipation, is $2/3$ of the end point

voltage drop for the parallel grid lines, and only $1/2$ for the tapered grid lines.

7. The lowest voltage drop in grid lines causing equal shading, is found in lines arranged normal to the bus lines, rather than slanted.

8. Grid structure optimization leads only to the grid line width to spacing ratio. This ratio depends primarily on the length of the grid line, its sheet resistance, and the current density. With this ratio, a smaller line width gives better performance, but is technologically and economically limited.

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I. Introduction.

Not only does the cost of the metallization process need to be considered, but also its effect on cell performance. So far, data on solar cell performance in dependence on the metallization process used are difficult to ascertain, or even non-existent, and the few available data are, in many cases, overshadowed by other process variables which are not connected with the metallization. Generally, it seems that more attention needs to be paid to the influences of the metallization processes on cell performance, since cell performance and the "value" (competitive price) are closely interrelated. One of the metallization connected parameters which strongly influences cell performance, is the metallization pattern design, often called "grid line design". It is more readily open for analysis than other aspects of the metallization process/performance relationship. Nevertheless, a lot of misunderstanding of the metallization pattern/performance relationship seems to exist. Therefore, this subject will be treated here in somewhat more detail.

The "grid line design" influences cell performance both through the series resistance of the solar cell which it is designed to reduce, and through the coverage of otherwise light sensitive areas by opaque metal layers, which the grid design causes. Different processes used for metal deposition and pattern generation impose various limits to the design options available here.

Along the path of the current through the solar cell, voltage drops occur due to several components of series resistance. In the base region, such voltage drops result from current flow in the semiconducting material essentially normal to the plane of the light-exposed surface, and from flow in the metallization layer behind the semiconductor, essentially parallel to that surface. In the front region, all current flow occurs essentially parallel to the junction plane, in the semiconductor from the point of injection to the nearest grid line, then within the metal of the grid lines, and finally in the metal of the major contact bars or "bus lines", causing voltage drops in all of these elements. There can be additional voltage drops in the semiconductor/metal interfaces (contact resistance) which are very process dependent and often not well controllable. Since "good processing" should result in minimal contact resistance, it is neglected in the following considerations.

The front metallization pattern covers a portion of the exposed solar cell area, which effectively results in a loss of light generated current, and consequently, power output. The design parameters of the front metallization pattern include direction, spacing, width, and thickness, both for the grid lines, and for the bus bars. A good cell design is one which includes a proper compromise between front area metal coverage and series resistance power loss, such that both will cause only small reductions of cell performance. Fundamental to obtaining low losses from both series resistance and metal coverage is using metallization of low sheet resistance R_{sh} :

$$R_{sh} = \frac{1}{\sigma \cdot d} \left[\Omega \right]; \quad (1)$$

Low sheet resistance requires, firstly, the choice of a metal of as high a conductivity σ as is practically - and economically - selectable. This "selection rule" also tends to favor processes which permit attaining the "bulk conductivity" of the selected metal, rather than some lower, process-dependent value of conductivity, as is, for instance, experienced with the powder-deposition and sintering processes. The second element of sheet resistance is the thickness d of the metal layer, which also should be as large as practical. With most metal-deposition processes, however, limitations exist with respect to the thickness practically attainable, be it because of problems in pattern definition or with stress in the deposited layer, which can result in its separation from the semiconductor. Where this limitation occurs, the length dimension of the metal conductor usually has to be restricted, since the other alternative, increasing its width, would entail greater "shadowing" and consequently, power loss. This other alternative results from the fact, that equal voltage drop is obtained from a constant "width-thickness-product" (cross-section) of the metal conductor, all other parameters being constant. The shadowing problem leads to the "real estate rule":

Any unnecessary area coverage should be avoided at all reasonable cost, since the cell area is most valuable real estate. It is so valuable, as considerable expense has gone into semiconductor purification, growth of a high-perfection crystal, and fabrication of a device of potentially high performance, and since further, substantial area-related costs will be incurred in encapsulation and array installation. As with other "high-value real estate", the consequence is the rule to build high rather than wide.

Where such grid-line length restrictions are encountered with the simultaneous desire for the use of larger cell dimensions, it becomes necessary to apply "bus lines" which need to have a much lower sheet resistance than the grid lines in order to be effective. In general, this lower sheet resistance will mean greater thickness.

In addition to low sheet resistance and narrow grid line width, a relatively close spacing of the grid lines is generally required, in order to keep the voltage drop within the semiconductor of the front region at acceptable levels. The values achievable for the three parameters, metal thickness, width, and center-to-center spacing of the lines, depend on the pattern resolution capabilities of the metallization process chosen, and thus involve a process-cost/cell-performance trade-off. For the back layer, the metal thickness, its area coverage and, if not complete, the geometry of the metallization pattern, as well as the number, location, and size of the interconnector pick-up points, similarly influence cell efficiency.

The metallization pattern design is much more sensitive in large area solar cells than in small cells. While small cells are quite forgiving to mistakes in grid structure design - very small cells do not even need any grid-patterned contact system - careless design of the contact geometry in large cells can lead to serious performance loss. This will be illustrated in a simple way in the following section. In the other sections, the analytical background to proper metallization design will be presented.

FIG. 1 Four Types of Front Contact Pattern Investigated.

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II. The Impacts of Metallization Pattern Design in 10 cm x 10 cm Solar Cells: Illustrative Examples.

To illustrate the impacts of metallization design on efficiency and process cost-effectiveness, seven metallization systems, including four different patterns, were evaluated for the resistive voltage drop and the area coverage. In the remaining three variants, the influence of the metal sheet resistance, as it would result from different process-parameters or process options, was considered. For this purpose, the thickness of the metallization, assumed to be copper of bulk conductivity, was varied from 5 μm thickness to 10 μm , simultaneously for both the front and the back metallization. In the final variant, the most favorable pattern geometry has also been evaluated with a metal layer as it would result from screen printing and sintering a silver paste, resulting in 10 μm thickness after firing. The study was based on the 10 cm x 10 cm cell size which seems to emerge as a standard size for large area cells. The differences in the 4 types of grid line patterns are illustrated in Fig. 1.

Pattern Type 1 uses 4 busses with equal spacing (2.5 cm ϕ - ϕ), placed normal to the grid pattern of parallel lines, and parallel to one of the sides of the 10 cm x 10 cm square cells. The width of the bus lines is 1 mm (40 mil). Each pair of adjacent busses is joined near one edge of the cell to form two attachment points for interconnectors to an adjacent cell in the module. The busses are assumed to be formed simultaneously with the grid line metallization, and consequently

Table I.

The Physical Parameters of the Seven Metallization Cases Used as Illustrative Examples.

CASE (COLUMN #)	1	2	3	4	5	6	7
PATTERN TYPE (Fig. 1)	1	2	2	3	3	4	4
BASE: BULK:							
RESISTIVITY (Ωcm)	3	→	1	→	→	→	→
THICKNESS (μm)	300	→	200	→	→	→	→
CONTACT:							
METAL THICKNESS (μm)	5	→	10	→	→	→	→
PICK-UP POINTS	1	→	2	→	→	4	→
FRONT: DIFFUSED LAYER							
SHEET RESISTANCE (Ω)	35	→	→	→	→	→	→
METAL:	Cu	→	→	→	→	→	PRINTED Ag
THICKNESS (μm)	5	→	10	→	→	→	10 (FIRED)
GRID LINE							
SPACING (mm)	4	→	2	→	→	→	→
WIDTH (μm)	127	→	75	→	→	→	127
BUS LINES							
NUMBER	4	1	→	4	→	→	→
WIDTH (mm)	1	→	→	0.25	→	0.64	→
PICK-UP WIRES							
NUMBER	-	→	→	2	8	4	→
GAUGE	-	→	→	26	→	22	→
DIAMETER (mm)	-	→	→	0.405	→	0.644	→

to be of the same material and the same thickness as these (5 μm). The center-to-center spacing of the grid lines is 4 mm (160 mil), their width 127 μm (5 mil) (Table I). The back of the cell has been assumed to be fully metallized, with one attachment point for an interconnector to the next cell located in the center of the cell. This general cell configuration is similar to some now on the market.

Once the geometry is defined, the voltage drops can be determined which result from the various series-resistance components in the cell. The first concerns the base region itself. Its resistance is given by:

$$R_B = \rho \frac{d_B}{A} ; [\Omega] \quad (2)$$

With a semiconductor resistivity ρ of 3 Ωcm , and a base region thickness d_B of 300 μm , the resistance is $9 \cdot 10^{-2} \Omega \text{cm}^2$ for the unit cell area. For the entire cell of area $A = 100 \text{ cm}^2$, R_B is $9 \cdot 10^{-4} \Omega$. The corresponding voltage drop at a maximum power point current of 3 A for the whole device will then be 2.7 mV, or approximately 0.5 percent of the expected maximum power point voltage.

For the back surface metallization with copper of bulk resistivity and 5 μm thickness, the sheet resistance R_{sh} is 3.2 m Ω . With uniform injection of the current over the entire back surface, the effective current flow within the metal layer is only one half of the total current extracted from the back contact. This could also be expressed as an effective resistance of the back contact metallization of 1.7 m Ω . However, the current is usually extracted from a small area to which an interconnector

FIG. 2 Two Backside Metallization Patterns considered.

to the adjacent cell is attached, rather than from a strip pick up uniformly attached along the entire length of one of the sides of the cell. The effective resistance value discussed would be appropriate for this latter arrangement. For the small area pick-up mentioned first, the spreading resistance has to be taken into account. Its value is given by:

$$R_{sp} = \frac{R_{sh}}{\pi} \left\{ \frac{\ln \frac{r}{a}}{1 - \left(\frac{a}{r}\right)^2} - \frac{1}{2} \right\}, \quad (3)$$

Assuming the interconnector to be attached in the center of the wafer with a circular joint of radius $a=1.5$ mm, the spreading resistance would be 3.3 m Ω (Fig. 2a). This spreading resistance value leads to a voltage drop of approximately 5 mV.

The sheet resistance of the front layer $R_{sh,FL}$ is assumed to be 35 Ω , the value generally used in modern shallow-diffused silicon solar cells. With the current path to the nearest grid line extending over half the clear spacing S between adjacent grid lines, and with uniform current injection into the layer occurring over this distance resulting in another factor of 2 , the effective resistance R_{FL} of the front layer itself attains the value given by:

$$R_{FL} = \frac{R_{sh,FL}}{4} \frac{S}{W}, \quad (4)$$

In this relationship, W is the total length of the grid line to the nearest bus line, or half the clear spacing between adjacent bus lines. The voltage drop in the front sheet is then given by the product of the resistance value given by equation (4)

and the current contributed from half of the space between adjacent grid lines, that is the area $\frac{S}{2} \cdot W$:

$$\Delta V_{FL} = j \cdot R_{sh,FL} \cdot \frac{1}{8} S^2 ; \quad (5)$$

It may be noted that the voltage drop is proportional to the square of the total length of the current path in the given sheet. This is characteristic for all current flow in sheet structures in the cell, and it emphasizes the need to keep the length of each of the current paths adequately small.

The effective resistance R_{GL} of the grid line itself is similarly given by:

$$R_{GL} = R_{sh,GL} \cdot \frac{W}{2} \cdot \frac{1}{T_{GL}} ; \quad (6)$$

and the voltage drop in the grid line due to the current collected from an area equal to $S \cdot W$ is given by:

$$\Delta V_{GL} = j \cdot R_{sh, GL} \cdot \frac{1}{2} \frac{S}{T_{GL}} W^2 ; \quad (7)$$

The 4 mm line spacing of the Type 1 grid pattern thus results in a voltage drop of 21 mV within the diffused layer. Using bulk resistivity of copper, 5 μ m grid line thickness, and 127 μ m line width, a 2.5 mV drop is found for the grid lines themselves.

Relationships corresponding to those for the grid lines (eq. (6) and (7)) apply for the bus lines, with the effective bus line resistance R_{BL} given by:

$$R_{BL} = R_{sh,BL} \cdot \frac{L}{2} \cdot \frac{1}{T_{BL}} ; \quad (8)$$

and the voltage drop in the bus line, with current collected from an area equal to $2W \cdot L$, being expressed by:

$$\Delta V_{BL} = j R_{sh,BL} \frac{W}{T_{BL}} L^2 ; \quad (9)$$

In equations (8) and (9), L expresses the length of the side of the solar cell, which is parallel to the bus line, assuming the bus line length to equal the length of this side. With the $5 \mu\text{m}$ thickness of the bus lines and their 1 mm width, the resistance of the bus lines is considerable, resulting in a voltage drop of 129 mV for the current flow of 0.75 A per bus line of pattern Type 1.

The voltage drops discussed here for the front layer and the metallization are the maximum voltages, appearing, for a grid line as an example, between the connection point to the bus line and the farthest point of the given grid line. The "effective voltage drop" which constitutes a weighted average, depends on the shape of the grid line, as will be discussed in section IV. For lines of uniform width, as well as the front layer itself and the back metallization, in the case of full coverage, the factor of $2/3$ is to be applied to the maximum voltage drop. For uniformly tapered lines reaching zero width at the farthest point, the factor is $1/2$. For pattern type I with uniform width grid and bus lines, the sum of all effective voltage drops, including those in the base region and the back contact, is 108 mV , or approximately 21% of the maximum power point voltage of the ideal cell with zero resistance.

Table II.

The Voltage Drops and Front Area Shading by Metal for the Seven Cases of Table I.

CASE (COLUMN #)	1	2	3	4	5	6	7
PATTERN TYPE	1	2	2	3	3	4	4
VOLTAGE DROP (mV)							
BASE: CONTACT	5	→	2.9	→	→	→	→
BULK	2.7	→	0.6	→	→	→	→
FRONT: DIFFUSED LAYER	21	11.1	4.9	→	→	→	→
GRID LINES	2.5	106.9	61	1.0	→	→	1.65
BUS LINES	129	15.1	15.1	15.6	0.97	0.96	0.95
WIRE	0	→	→	8.6	2.8	0	→
TOTAL EFFECTIVE: (mV)	108	95	56.5	22.7	8.9	7.1	7.5
AS % OF V_{MAX} , IDEAL	21	18.3	10.9	4.3	1.7	1.4	1.5
AREA COVERAGE (cm² = %)							
GRID LINES	3.18	4.02	3.6	→	→	→	6.1
BUS LINES	4.0	0.97	0.98	→	→	2.5	2.5
WIRES	0	→	→	0.7	2.8	0	→
TOTAL	7.2	5.0	4.6	5.3	7.4	6.1	8.6

This value is clearly intolerably high. In addition, the grid lines and the bus lines cover 3.2 and 4.0 percent, respectively, of the frontal area of the cell. For the cell with metallization design Type I, the combined series resistance related power loss, including the front area coverage, thus amounts to approximately 28% of the potential power output (Table II).

As equations (6) and (8) show, the maximum voltage drop is proportional to the square of the path-length of the current in the respective conductor. In order to limit a given voltage drop, it is therefore important to limit the path length for the current. Since in the first metallization pattern, Type 1, the main voltage drop occurred in the bus lines, the remedy would be shortening their length. This consideration leads to the pattern design Type 2, where there is only one bus line, running along one edge of the cell (Fig. 1 p. 5). The number of pick-up points, two, on the front has been maintained from Type I, so that the average path length in this main bus line is now reduced from 10 cm to $2\frac{1}{2}$ cm, with a resulting decrease of the voltage drop in this element from 129 mV to 15 mV. Simultaneously, the grid line spacing has been reduced from 4 mm to 3 mm (Table I, p. 7). The back metallization has been maintained as before. As a consequence of the reduced grid line spacing, the voltage drop in the front layer itself has been reduced from 21 mV to 11 mV. Because of the increase of the length of the grid lines, however, and in spite of the reduced current flow in each one of them, their voltage drop has grown from 2.5 mV to 107 mV.

In consequence, the total effective voltage drop for the cell is 95 mV. Simultaneously, the increase in the number of grid lines has increased their area coverage from 3.2 to 4%, while the coverage by bus lines has been reduced to 1%, yielding a total area coverage of 5%. (Column 2 of Table II, p. 13).

While the change in metallization pattern from Type 1 to Type 2 brought significant reductions in both voltage drop and area coverage, the series resistance power loss is still much higher than acceptable. In the next step, the Type 2 pattern has been maintained, but a number of refinements have been assumed, in order to reduce the voltage drop. All metallization has been increased in thickness from 5 to 10 μm , which is about the maximum thickness reliably obtainable by various deposition methods. The resistivity of the base material has been decreased from 3 to 1 Ωcm , and the thickness of the base region from 300 to 200 μm , in order to reduce the base voltage drop (Table I, p.7). For the same reason, the number of pick-up points on the base contact has been increased to 2. This number also corresponds to the number of pick-up points on the front of the cell, and it provides redundancy. Also, the base pick-up points have been moved from the center of the cell to one edge of the cell (nearest to the adjacent cell), and they have been shaped as semicircles of 4 mm diameter. Their effective spreading resistance is 1.1 m Ω . Outside of the spreading resistance region, the metallization sheet is effectively two times 5 cm wide and 8 cm long each half leading to one of the contact points (Fig. 2b, p. 9).

The additional resistance of this metallization sheet is $2.7 \text{ m}\Omega$, so that the total resistance is $3.9 \text{ m}\Omega$ for each half of the back metal layer. Because of the uniformly distributed injection into the metal layer, only one half of this total resistance is effective. Since each pick-up point carries only one half of the total cell current, the back metallization voltage drop is 3.9 mV , for a total base region voltage drop of 3.5 mV .

In addition to these base region refinements, the grid line spacing has been further decreased from 3 to 2 mm, with a simultaneous decrease in the width of the grid lines from 127 to $75 \text{ }\mu\text{m}$, so as not to increase the area covered by grid lines (Table I, p. 7). This reduced gridline spacing gives a voltage drop of 4.9 mV in the front layer itself. Simultaneously, the reduced current flow in each grid line, together with their increased thickness, yields a grid line voltage drop of 61 mV . Taking also account of the voltage drop in the main bus line (15 mV), a total effective voltage drop for the entire cell of 56.5 mV is now obtained, for a power loss of approximately 11%. At the same time, a small reduction of the metal coverage in front (4.6%) has been achieved as a result of the slightly decreased grid line width (Column 3 of Table II, p. 13).

Since the major voltage drop is now incurred in the grid lines, the logical next step is to decrease their length. A way of accomplishing this is by distributing the bus line again to four lines, directed normal to the grid lines (Type 3 in Fig. 1, p. 5). The average center-to-center spacing of these busses is 2.5 cm

The interconnectors to the adjacent cell are now running over the top of the cell for most of its length, serving simultaneously as pick-ups from the 4 bus lines, as shown by the open and solid wide lines, respectively, in the Type 3 pattern illustration. All other metallization features have been kept constant. The grid line voltage drop has been reduced to 1 mV without additional area coverage, but an additional 8.6 mV drop is now incurred in the interconnect wires, which are assumed to be of 26 gauge (B & S) which corresponds to 0.4 mm diameter. The total effective voltage drop now is 22.7 mV, or 4.3% of the ideal maximum power point voltage. Because an additional area is covered (0.7%) by the 2 interconnect wires, the total area coverage by metal has increased to 5.3% (Column 4 of Tables I and II, p. 5 and p. 13, respectively).

Since the largest voltage drop in the Type 3 pattern is in the bus lines, the number of pick up wires has, for a trial, been increased from 2 to 8, mindful of the L^2 rule for the bus lines. The other features of the Type 3 pattern have been maintained. This change resulted in a decrease of the bus line voltage drop from 16 mV to 1 mV, and that in the pick-up wires from 8.6 mV to 2.6 mV, with a consequent total effective voltage drop of now 8.9 mV, for a 1.7% total series resistance power loss. While this could be considered as a tolerable level, the increased number of pick-up wires now shade 2.8% of the frontal area, for a total shaded area of 7.4%, a value significantly larger than considered acceptable.

As the number of pick-up wires used in the previous trial seems excessive, their number has subsequently been again reduced to 4. Also, since there occurs some unnecessary shading by both bus lines and pick-up wires, the pattern has been rotated by 90° , so that the pick-up wires run now on top of the bus lines (Type 4 in Fig. 1, p.5). This, in effect, constitutes a reduction of the sheet resistance of the bus lines through a thickness increase. In fact, by slightly increasing the diameter of the pick-up wires to 22 gauge (0.64 mm diameter), the bus line voltage drop could be maintained at the same value as in the prior arrangement, although only half the number of pick-up wires is used. Simultaneously, the additional voltage drop in the pick-up wires is eliminated (Column 6 of Table II, p. 13). Consequently, the total effective voltage drop is 7.1 mV, corresponding to 1.4% power loss. In this approach, the bus line area coverage has been increased to 2.5%, but no additional area coverage by pick-up wires is incurred. Thus, the total front area coverage by metallization is 6.1% (Column 6 of Table II, p. 13).

The use of printing methods for application of the metallization pattern has recently found widespread interest because of potentially very low processing costs. For this reason, the grid and bus line pattern Type 4 which was just discussed with plated-copper metallization, has also been evaluated for a screen-printed thick film silver system. Use of this system entails two restrictions. First, the minimum line width attainable with thick film screen printing has been projected to

127 μm , although 254 μm is currently the minimum practical line width. In contrast, line widths of less than 75 μm are readily attainable now with various other plating methods. This necessitates larger area coverage with screen printing. The second restriction is that the sintered metal layers have a higher resistivity than the bulk metal, or plated layers. With the practically attainable maximum thickness of 10 μm for a single screen printed layer after firing, the sheet resistance becomes limited by the generally experienced conductivity of the paste-deposited and sintered silver, which is about 30% of its bulk conductivity (Column 7 of Table I, p. 5). With this, the grid line voltage drop is increased to 1.65 mV for a total effective voltage drop in the cell of 7.5 mV corresponding to 1.5% power loss (Column 7 of Table II, p. 13). Because of the greater grid line widths, the total area coverage is increased to 8.6%. Together, this entails a power output reduction by 2.6% incurred in switching from the plated copper to the screen-printed silver metallization system.

In a solar cell idealized to zero series resistance and zero front area coverage, a maximum-power-point current of 33 mA cm^{-2} and a maximum-power-point voltage of 0.52 V would correspond to current technology, for a power output of 17.2 mW. Assuming the series resistance to effect only the output voltage by reduction from the ideal maximum-power-point voltage with the effective voltage drop, and the area coverage to affect only the maximum-power-point current in proportion to the unshaded front area, a table of power output per unit cell area for the seven different

Fig. 3: Four curves representing the relationships between the value of solar cells and solar modules, respectively, and the efficiency of the modules. Both are expressed in dollars/m² (left hand scale) and dollars/peak Watt (right hand scale). The value is determined by the equal price of the energy delivered from the array. The reference module value is 0.683\$/W(peak) at a module efficiency of 14% (circles), with an 0.201\$/W(peak) encapsulation and module assembly price, using a ratio of 0.933 between module efficiency to encapsulated cell efficiency. The array installation price is 60\$/m², with an array packing factor of 0.95. All these base data are DOE/JPL 1986 goals for single crystal silicon cells.

The array installation price determines the slope of the module value curves, the module encapsulation and assembly cost the differences in the pivot-point values (circles) and in the slopes between the module and cell-value curves.

Table III.

Output Power (Efficiency) and Solar Cell Values for the Seven Metallization Cases of Table I.

CASE (COLUMN #)	1	2	3	4	5	6	7
PATTERN TYPE	1	2	2	3	3	4	4
APPROX. OUTPUT VOLTAGE V_{MAX} (V)	0.412	0.425	0.463	0.497	0.511	0.513	0.513
APPROX. CURRENT DENSITY J_{MAX} (mA cm ⁻²)	30.64	31.36	31.50	31.27	30.57	31.00	30.19
APPROX. POWER OUTPUT P (mW cm ⁻²)	12.6	13.3	17.6	15.5	15.6	15.9	15.5
CELL VALUE \$/m ²	55	62	78	88	90	93	88
\$/W	0.403	0.443	0.505	0.54	0.545	0.554	0.54

metallization cases can be generated (Table III). Because of the use of 100 mW cm^{-2} peak insolation, the power output numbers represent simultaneously the efficiency numbers. Using the curve of solar cell value as function of module efficiency (Fig. 3) which was described in the Fourth Quarterly Report of this project, cell values can be assigned to the different cell metallization systems, based on their differences in module efficiency. A perhaps somewhat optimistic factor of 0.9 has been used in converting from the bare cell efficiencies to module efficiencies. As Table III shows, the cell values vary from \$93 per m^2 to below \$60 per m^2 for the less carefully designed systems. Even the \$5/ m^2 difference in value between the copper plated and the silk screened metallization of Type 4 is large enough to permit use of a significantly more costly process to accomplish a metallization pattern of narrower lines than achievable by screen printing.

FIG. 4 Simplified Lumped-Constant Equivalent Circuit of the Solar Cell.

III. The Influence of Series Resistance on Solar Cell Performance.

1. A single lumped series resistance.

Because of the exponential I-V characteristic of the junction of the solar cell, all considerations of series resistance become complicated. Consequently, some of the effects of series resistance are not thoroughly explored, and a good deal of confusion seems to persist in the technical community. A small effort has, therefore, been spent on trying to clarify some of the simpler points. As Fig. 4 shows, the solar cell with a single lumped series resistance can generally be represented by a constant current generator which delivers the light generated current I_L , in parallel with an ideal diode which drains off part of this current as the "diode current" I_D . Consequently, the remaining current I is available for passage through the solar cell terminals to an outside circuit which is represented by the load resistance R_L in Fig. 4:

$$I = I_D - I_L ; \quad (10)$$

$$I_D = I_0 \left(e^{BV_D} - 1 \right) \approx I_0 e^{BV_D} ; \quad (10a)$$

With: $B = q/kT$.

The solar cell with series resistance can be considered as an ideal solar cell without series resistance, having imaginary terminals across which the "diode voltage" V_D appears, as indicated in Fig. 4. This ideal solar cell is then connected to an external resistance R_S , which represents the single lumped series resistance of the cell, and which leads to the real solar cell

FIG. 5 Current - Voltage Characteristics of the Solar Cell Without and With Series Resistance (a), and of the Output Power Without Series Resistance (b).

terminals. The voltage V appears across these terminals, and the adjusted external load resistance R_L is connected to them. Thus, the ideal solar cell would see the combined load resistance:

$$R'_L = R_S + R_L ; \quad (11)$$

and its maximum power output would be $I \cdot V_D$, where the current I and the voltage V_D are designated as $I_{mp, R=0}$ and $V_{mp, R=0}$ in Fig. 5a. Thus, that IV characteristic in Fig. 5a on which the point $V_{mp, R=0}$, $I_{mp, R=0}$ lies, is the characteristic of the ideal solar cell without series resistance.

On the real terminals, after the series resistance R_S , that characteristic applies which is represented by the curve going through the point $V_{mp, R}$ and $I_{mp, R}$ (Fig 5a). At each current point, the voltage V_R on this characteristic is reduced from that of the ideal solar cell by the voltage drop $I \cdot R_S$ in the series resistance:

$$V_R = V_D + I R_S ; \quad (12)$$

Thus, for the maximum power point current $I_{mp, R=0}$ on the ideal diode, the voltage $V_{mp, R=0} - I_{mp, R=0} \cdot R_S$ appears at the terminals of the device after the series resistance. Note that all terminal currents I are negative according to eq. (10) and Fig. (5a).

The power output of the solar cell is given by the product of current and voltage at each point of the IV characteristic. Thus, for the device with series resistance, the power output at any terminal voltage V_R is given by:

$$P = IV_R = V_R I_{oe}^{BV_D} - V_R I_L ; \quad (13)$$

with V_D as it appears at the ideal diode terminals according to eq. (12). The power output P as function of the terminal voltage V_R has the form shown in Fig. 5b. The maximum power available from the device is indicated by P_{mp} . The derivative of the power output with respect to the terminal voltage V_R is given by:

$$\frac{dP}{dV_R} = I + V_R \frac{dI}{dV_R} = I + BV_R I_0 e^{BV_D} ; \quad (14)$$

and, in order to find the maximum power point voltage V_{mp} , this derivative is set equal to 0.

The interesting part is, that introduction of relationship (12) into the left hand part of eq. (13) leads to:

$$P = IV_D + I^2 R_s ; \quad (15)$$

which shows that the available power output at the terminals is the power output from the ideal solar cell reduced by the power dissipated in the series resistance. The power output according to eqs. (13) and (15) appears as a negative quantity, while the dissipated power is a positive quantity. It should also be noted that the derivative $\frac{dI}{dV}$ is a positive quantity, although I is a negative quantity in the range of interest. The current I_D which flows through the diode junction, is also positive. Thus, for the idealized solar cell with zero series resistance, the maximum output attainable is:

$$\begin{aligned} P_{mp, R=0} &= I_{mp, R=0} V_{mp, R=0} \\ &= \left(I_0 e^{BV_{mp, R=0}} - I_L \right) V_{mp, R=0} ; \end{aligned} \quad (16)$$

with all concerned quantities indicated by subscript $R=0$.

For the real solar cell with a single lumped-constant resistant R_s , however, the maximum power output is:

$$\begin{aligned} P_{mp,R} &= I_{mp,R} V_{mp,R} \\ &= I_{mp,R} \left(V_{D,mp} + I_{mp,R} R_s \right) ; \end{aligned} \quad (17)$$

or

$$P_{mp,R} = V_{D,mp} \left[I_0 e^{BV_{D,mp}} - I_L \right] + I_{mp,R}^2 \cdot R_s ; \quad (17a)$$

Here, $V_{D,mp}$ is the voltage which appears across the idealized solar cell for maximum power out of the real terminals. The question is, whether maintaining the maximum power output from the idealized device also delivers maximum power into the properly adjusted load resistance R_L (eq.11), or whether deviating from the point at which the idealized solar cell itself supplies maximum power will actually deliver more power into the load. The latter statement means, that the power output from the ideal device would decrease less rapidly than the power dissipated in the load resistance, as this deviation from the ideal device maximum power point occurs. This can be readily tested by use of the derivative of the maximum power output from the real device with load resistance:

$$\begin{aligned} \frac{dP_{mp,R}}{dV_{D,mp}} &= \frac{dP_{mp,R=0}}{dV_{D,mp}} + \frac{d}{dV_{D,mp}} \left(I_{mp,R}^2 \cdot R_s \right) \\ &\approx 2 I_{mp,R} R_s \frac{dI_{mp,R}}{dV_{D,mp}} ; \end{aligned} \quad (19)$$

This equation contains basically two terms according to those of eq. (17a), where the first term was derived from the maximum power point of the idealized device. Now, the maximum power output from the idealized device has been found by setting its derivative with respect to the voltage equal to zero. Thus, a deviation from the maximum power value at small changes of the voltage can only be of very small magnitude. The dissipated power, however, changes with the first derivative of the current, and will thus be much larger. As remarked above, the derivative $\frac{dI}{dV}$ is positive and is multiplied in the second term of eq. (19) with the maximum power point current itself which is a negative quantity. Thus, the change in power output from the real device terminals with a change in voltage is a negative quantity, indicating an increase in the available power output. Consequently, the optimum operating point of the solar cell with series resistance is at a voltage which is slightly greater than given by $V_{mp,R=0} - I_{mp,R=0} \cdot R_s$, and the power output thus obtainable will be slightly greater than that of the solar cell matched for a terminal voltage equal to the ideal maximum-power-point voltage minus the voltage drop in the series resistance, as indicated by the horizontal arrow in Fig. 5a. The related, commonly used way of analyzing the solar cell by considering the matched case of the idealized device and reducing the power output by the dissipation in the series resistance results in a slightly smaller than optimum power output. Since the differences in power output are small, most results obtained this way should be justifiable, but it will be good to keep in mind that these analyses actually

are worse-case approximations. In the following discussions, this same approach will also be used for reasons of simplicity.

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2. The effect of different solar cell elements operating at differing voltages.

The treatment of series resistance as a single lumped constant element, as carried out in the preceding section, is quite appropriate for series resistance components through which the entire cell current flows. This is the case with the contact resistance and the bulk resistance of the base region. Other series resistance components, however, cause differing voltages to appear across various parts of the pn junction. These are the voltage drops caused in the back metallization, and in the sheet resistance of the front layer, as well as the voltage drops occurring in the grid lines and the bus lines.

When various parts of the solar cell operate at different junction voltages, one might expect that differing current contributions are made from these parts of the solar cell, according to eqs. (10). In the single lumped constant representation, the reduction in output power was shown to be at most the power dissipated in the resistive component, and influences of the exponential nature of the I-V characteristic to be slightly beneficial rather than detrimental. When parts of the cell operate at differing voltages, however, the situation is different. The losses expected in this case will be termed "mismatch losses".

In order to investigate the magnitude of such potential mismatch losses, it was assumed that the cell operates essentially

FIG. 6 Parallel Arrangement of three Identical Solar Cells with Different Series Resistances.

in the maximum power point condition at an average voltage drop across the resistive elements, and that the deviations of the junction voltage from the average at the individual parts of the solar cell will be both in the positive and negative directions. To simulate this case in a simple manner, a model was devised which consists of 3 identical solar cells, which are connected in parallel over 3 different series resistances to a common external load (Fig. 6). The series resistance of cell 1 was called R_{s1} , and those of cells 2 and 3 were considered to be larger and smaller than R_{s1} by equal amounts ΔR :

$$R_{s2} = R_{s1} + \Delta R ; \quad (20a)$$

$$R_{s3} = R_{s1} - \Delta R ; \quad (20b)$$

It was thought that such a symmetrical arrangement might best illustrate the existence of the expected mismatch losses.

The power output of the 3 parallel connected cells can be expressed as:

$$P_{out} = (I_1 + I_2 + I_3)V = \left\{ I_o \left[e^{\frac{B(V - I_1 R_{s1})}{V_T}} + e^{\frac{B(V - I_2 R_{s2})}{V_T}} + e^{\frac{B(V - I_3 R_{s3})}{V_T}} \right] - 3I_{J1} \right\} V ; \quad (21)$$

with:

$$V - I_1 R_{s1} = V_{mp, R=0} ; \quad (22)$$

or

$$V = V_{mp, R=0} + I_1 R_{s1} ; \quad I_1 < 0. \quad (22a)$$

In the subsequent parts of this section, $V_{mp,R=0}$ will be written simply as V_{mp} .

The $I \cdot R$ voltage drops across the 3 series resistances will be of unequal magnitude, as expressed by:

$$I_2 R_2 > I_1 R_{s1} > I_3 R_{s3} ; \quad (23)$$

While the common terminal voltage for all 3 solar cells is assumed to be the maximum power point voltage V of the real cell 1, the voltage across the ideal solar cell 1, exclusive of series resistance, is its maximum power point voltage V_{mp} , as expressed in eq. (22).

Combining eqs. (21) and (22a) leads to the form:

$$P_{out} = \left[I_o e^{\frac{BV_{mp}}{V}} \left(1 + e^{\frac{B(I_1 R_{s1} - I_2 R_{s2})}{V}} + e^{\frac{B(I_1 R_{s1} - I_3 R_{s3})}{V}} \right) - 3I_L \right] V ; \quad (24)$$

which can be, for adequately small differences in the voltage drops over the 3 different series resistances, expressed by first order approximation:

$$P_{out} = \left\{ I_o e^{\frac{BV_{mp}}{V}} \left[1 + 1 + B(I_1 R_{s1} - I_2 R_{s2}) + 1 + B(I_1 R_{s1} - I_3 R_{s3}) \right] - 3I_L \right\} V ; \quad (25)$$

Segregating appropriate terms leads to:

$$P_{out} = \left[3 \left(I_o e^{\frac{BV_{mp}}{V}} - I_L \right) + I_o e^{\frac{BV_{mp}}{V}} B (I_1 R_{s1} - I_2 R_{s2} + I_1 R_{s1} - I_3 R_{s3}) \right] V ; \quad (25a)$$

which, after application of eq. (22a) takes the form:

$$= 3I_{mp} V_{mp} + 3I_{mp}^2 R_{s1} + B(I_1 R_{s1} - I_2 R_{s2} + I_1 R_{s1} - I_3 R_{s3}) I_o e^{\frac{BV_{mp}}{V}} V ; \quad (26)$$

In this form, the first two terms give the sum of the maximum power output of the 3 idealized solar cells, reduced by 3 times the dissipation in the average series resistance value R_{s1} . The remaining terms indicate the deviation from this simplified model.

The differences in the actual voltage drops which are expressed in these remaining terms on the third right hand side of eq. (26), can be transformed as in eq. (27a) and (27b):

$$I_1 R_{s1} - I_2 R_{s2} = (I_1 - I_2) R_{s1} - I_2 \Delta R = (I_1 - I_2) (R_{s1} + \Delta R) - I_1 \Delta R ; \quad (27a)$$

$$I_1 R_{s1} - I_3 R_{s3} = (I_1 - I_3) R_{s1} + I_3 \Delta R = (I_1 - I_3) (R_{s1} - \Delta R) + I_1 \Delta R ; \quad (27b)$$

and to:

$$I_1 - I_2 \approx BI_0 e^{\frac{BV}{V_T}} \left[-R_{s1} (I_1 - I_2) + (I_2 - I_1) \Delta R + I_1 \Delta R \right] . \quad (28)$$

Finally, the differences in the terminal currents of solar cells 2 and 3 against that of cell 1 can be expressed as:

$$I_1 - I_2 = FI_1 (1 - F) ; \quad (29a)$$

and:

$$I_1 - I_3 = -FI_1 (1 + F) ; \quad (29b)$$

with:

$$F = \frac{BI_D \Delta R}{1 + BI_D R_{s1}} ; \quad (30)$$

Introducing these forms into eq. (26) permits expressing the output power in the simpler form:

$$P_{out} = 3(I_1 V_{mp} + I_1^2 R) + 2FR \left\{ \frac{\Delta R}{R} - F \right\} I_1 B I_O e^{BV_{mp}} (V_{mp} + I_1 R) ; \quad (31)$$

The actual dissipation in the three series resistances of differing magnitude is given by:

$$P_{Diss} = I_1^2 R_{s1} + I_2^2 R_{s2} + I_3^2 R_{s3} ; \quad (32)$$

By combining eq. (26), (29 a and b), (30), and (32), the expression for P_{Diss} can be transformed into one containing only the current I_1 , the average resistance R , and the difference in the series resistance values ΔR :

$$P_{Diss} = 3I_1^2 R + 2I_1^2 \left[(3F^2 + F^4)R - 2F(1 + F^2)\Delta R \right] ; \quad (33)$$

The power output P_{out} actually transferred into the load resistance, as given by eq. (31), plus the power dissipated, according to eq. (33), should add up to the maximum power output available from the three "ideal devices", unless there are "mismatch losses". In the latter case, the sum of the power output plus the dissipated power would be expected to be smaller than the "ideal" maximum power output. This hypothesis shall be tested in the following.

Since the power output into the load resistance is given by the IV product, where I is a negative quantity, this power output also appears as a negative quantity. The dissipated power which is a positive quantity, thus will actually have to be subtracted from the power output to form the larger negative quantity of the ideal power, as is done for eq. (34) which combines eqs. (31) and (33):

$$\begin{aligned}
P_{out} - P_{Diss} = & 3I_1 V_{mp} + 4I_1^2 \left[F(1+F^2) \Delta R - \left(\frac{3}{2}F^2 + \frac{1}{2}F^4 \right) R \right] \\
& + 2F R \left(\frac{\Delta R}{R} - F \right) I_1 B I_o e^{BV_{mp}} V_{mp} \\
& + 2F R \left(\frac{\Delta R}{R} - F \right) B I_o e^{BV_{mp}} I_1^2 R ; \quad (34)
\end{aligned}$$

and which can readily be simplified to the form:

$$\begin{aligned}
P_{out} - P_{Diss} = & 3I_1 V_{mp} + 2 F \left(\frac{\Delta R}{R} - F \right) B I_o e^{BV_{mp}} R \cdot I_1 V_{mp} \\
& + 2 \left\{ 2(F+F^3) \frac{\Delta R}{R} - 3F^2 - F^4 + F \left(\frac{\Delta R}{R} - F \right) B I_o e^{BV_{mp}} R \right\} I_1^2 R ; \quad (35)
\end{aligned}$$

The first term on the right hand side of eq. (35) represents the expected maximum power output from the three idealized solar cells, disregarding the series resistance voltage drop. The remaining part of the right hand side of eq. (35) represents the expected potential mismatch losses. This remaining part is the only quantity of further interest. It will, from here on, be evaluated for its magnitude. Since it is attributable to the two cells #2 and 3, it shall be designated as $2\Delta P$:

$$P_{out} - P_{Diss} = 3I_1 V_{mp} + 2\Delta P ; \quad (36)$$

Combining terms, expressing the quantity V_{mp} in the exponent by the relationship (22), and approximating the exponential factor with the exponent $B I_1 R$ by the Tailor expansion broken off after the linear term, leads to the expression:

$$\Delta P = F^2 \left\{ (1 - BI_1 R) I_1 V_{mp} + \left[\frac{2}{BI_D R} - BI_1 R + \left(\frac{2}{BI_D R} + 1 \right) F^2 \right] I_1^2 R \right\} ; \quad (37)$$

with $F = \frac{BI_D \Delta R}{1 + BI_D R}$

The first term in the large brackets on the right hand side of eq. (37) contains what might be expected as the "mismatch losses". This term is, however, negative, and consequently means an increase in maximum power output rather than a reduction. The second term on the right hand side, containing the square brackets, is connected with the dissipation loss, and turns out to be generally positive, which means increased dissipation. The first term in the square bracket is the dominant term by far.

Entering numbers into eq. (37), such as a series resistance R of 0.25Ω , and a ΔR of 0.1Ω , a terminal current $I_1 = 3 \cdot 10^{-2} A$ (as for a 1 cm^2 cell), and a saturation current $I_0 = 2.8 \cdot 10^{-12} A$, it turns out that the ΔP becomes 5.4% of the $I^2 R$ loss. The ΔP is negative, however, which means that the power output obtainable from the three solar cells in combination is slightly greater than that which would correspond to the maximum power output from the three ideal solar cells, reduced by the $I^2 R$ losses in the three differing series resistance.

FIG. 7 Grid Line Configurations.

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IV. The Voltage Drop in Uniform Width or Tapered Grid Lines.

The width of the grid line at the distance ℓ from its connection to the bus line is given for the grid line of uniform width by (Fig. 7a):

$$T_{PGL}(\ell) = T_{GL} ; \quad (38)$$

and for the tapered grid line by (Fig. 7b):

$$T_{TGL}(\ell) = 2T_{GL} \frac{W-\ell}{W} ; \quad (39)$$

For the tapered grid line, the width at the connection to the bus line is set equal to $2 \times T_{GL}$, so that the total area shaded by the tapered grid line equals that shaded by the grid line of uniform width $T_{GL}W$. The voltage drop over the length element $d\ell$ of the gridline is then given by the product of the resistance of this length element and the current flowing in the grid line at this distance from the bus connection:

$$dV = R_{sh} \frac{d\ell}{T(\ell)} \cdot j_{mp}(W-\ell)S ; \quad (40)$$

where R_{sh} is the sheet resistance of the grid line. Substituting either eq. (38) or (39) for $T(\ell)$, and integrating eq. (40) from zero to W gives the voltage drop $V(W)$ to the end point of the grid line:

$$V(W) = j_{mp} R_{sh} \frac{S}{2T_{GL}} W^2 ; \quad (41)$$

This "end point voltage drop" is the voltage drop which occurs

FIG. 8 Voltage Drop along a Uniform Width and a Tapered Grid Line, respectively. Note that the end-point ($l=W$) voltage drops are equal, when both grid lines cover identical areas ($T_{GL} \cdot W$).

over the entire length of the gridline. It signifies, how much higher the junction voltage is at the farthest point from the bus line, than it is at the connecting point to the bus line.

Although this end point voltage drop is the same for both the tapered and the uniform width grid line, the voltage distribution along the length of the two types of grid lines varies (Fig. 8). For the uniform width grid line, the voltage drop $V(\ell)$

$$V_{PGL}(\ell) = V(W) \left[2 \frac{\ell}{W} - \left(\frac{\ell}{W} \right)^2 \right] ; \quad (42)$$

increases more rapidly near the connection to the bus line than that of the tapered grid line which rises linearly over the length of the grid line:

$$V_{TGL}(\ell) = V(W) \frac{\ell}{W} ; \quad (43)$$

In correspondence to this increasing voltage drop along the grid line, a varying voltage exists across the pn junction, and the diode current will vary accordingly. Thus, one would expect a complicated relationship for finding the effective maximum power point in a device with such varying junction voltage, considering the exponential nature of the IV characteristic. This is indeed the case, and an attempt to derive a manageable solution has so far only resulted in lengthy and non-transparent expressions.

However, in consequence of the discussions in section III-2, in which this case was modelled in a very simplified approach by 3 solar cells connected in parallel over three different series resistances, it was found adequate to evaluate the dissipation occurring in each type of grid line. Integration of the dis-

sipated power contributions along the grid line according to:

$$P_{Diss} = \int_0^W I(\ell) dV = \int_0^W j_{mp} (W-\ell) S dV ; \quad (44)$$

utilizing eq. (40) with either eq. (38) or (39), yields the total power dissipated in the uniform width or the tapered grid line, respectively. Equation (45) gives the result for the uniform width grid line:

$$P_{Diss,PGL} = \frac{2}{3} V(W) \cdot j_{mp} SW ; \quad (45)$$

showing that the power dissipation equals 2/3 times the end point voltage $V(W)$ times the total current flow through the grid line. For the tapered grid line:

$$P_{Diss,TGL} = \frac{1}{2} V(W) \cdot j_{mp} SW ; \quad (46)$$

the factor 2/3 is replaced by 1/2. Thus, the "effective voltage drop" is 2/3 or 1/2 of the end-point voltage drop for the uniform width or the tapered grid line, respectively. Consequently, the tapered grid line has a slight advantage with respect to solar cell performance over the uniform width grid line.

It should be noted, however, that a truly tapered grid line, ending in a zero width end point, is practically impossible to produce. Therefore, the actually fabricated tapered grid lines are a compromise between the truly tapered and the uniform width grid line. Their effective voltage drop will thus be between 1/2 and 2/3 of the end point voltage.

A situation equivalent to that just discussed with respect to the grid lines also exists in the bus lines, in the semiconducting front layer, and in the back metallization. With the possible exception of the bus lines, they all are represented by analogues to the "uniform width grid lines" equations. The bus lines may be tapered, but where they are reinforced by an overlaid wire, they act like uniform width lines.

In the semiconducting front layer, the voltage drop occurs between the edge of the grid line and a line halfway between two adjacent grid lines. This line is at the end-point voltage relative to the voltage existing at the nearest points on the adjacent grid lines, assuming a parallel grid system. The drops in the various components - bus lines, grid lines, front layer - thus add up to a different voltage at each portion of the junction area. However, as shown in Section III, the "effective junction voltage" can be determined from the terminal in the various resistive components present in the device.

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V. Grid Structure Optimization.

1. By maximizing power output, based on simultaneous optimization of series resistance and shading losses, only an optimum grid-line-width to grid-line-spacing ratio can be determined. It is approximately:

$$\frac{T}{S} \approx W \left(\frac{j_L R_{sh, GL}}{2(V_{mp} + \frac{1}{B})} \right)^{\frac{1}{2}}; \quad (47)$$

with $R_{sh, GL}$ being the grid line sheet resistance and j_L the light generated current density ($B=q/kT$). W is the grid line length, or half the bus line spacing. Otherwise, choosing the grid line width as small as technologically possible and economically practical helps to increase performance.

2. Orientation of the grid lines normal to the bus lines results in a lower voltage drop, at equal shading, than arranging the grid lines slanted.

3. The derivations of the analytical relationships underlying the above statements, and their discussion will be included in the next quarterly report.

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VI. Conclusions.

Low loss metallization systems are now technically feasible, and their design can be handled with adequate accuracy. Thus, the techno-economic trade-off between practical processes and the resulting performance of the solar cells, with the consequent influence on solar cell value, can now be made. They will be examined in the subsequent quarterly reports.

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VII. Plans

Continue evaluation of metallization process options.

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VIII. New Technology

No new technology was developed during this quarter.