MASTER

CADMIUM SULFIDE - COPPER SULFIDE
HETEROJUNCTION CELL RESEARCH

Quarterly Progress Report

March 1 - May 31, 1980

XS-9-8309-1

November 1980

Institute of Energy Conversion
University of Delaware
Newark, Delaware 19711

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States nor any agency thereof, nor any of their employees, makes any warranty, expressed or implied or assumes any legal liability or responsibility for any third party's use or the results of such use of any information apparatus, product or process disclosed in this report, or represents that its use by such third party would not infringe privately owned rights.

Supported by the Solar Energy Research Institute, Report No. XS-9-8309-1-03

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

1. Abstract

A complete statistical analysis of the yield of CdS/Cu₂S cells produced by the standard processes is presented. Progress has been made on producing (CdZn)S films with the appropriate properties to yield high efficiency cells. Further studies of capacitance and transient-capacitance are reported. Defects in electron beam deposited glass are shown to be responsible for lack of effective sealing against atmospheric attack.

DISCLAIMER

This book was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

24B

2. Table of Contents

Page

1. Abstract	1
2. Table of Contents	2
2.1 List of Illustrations	3
3. Introduction	5
4. Cell Production, Analysis and Testing	6
4.1 Development CdS/Cu ₂ S Solar Cells	6
4.2 Development (CdZn)S/Cu ₂ S Solar Cells	21
4.3 Electro-Optic Analysis and Modeling	36
4.4 Encapsulation for Improved Stability	57
5. References	64
6. Appendix	65

2.1

LIST OF ILLUSTRATIONS

- Figure 1 CuCl Deposition System.
- Figure 2 Scanning Electron Micrographs x2000. (a) Nickle-Iron Substrate.
(b) Copper Plated Ni-Fe. (c) (CdZn)S on Zinc/Copper Plated Ni-Fe.
- Figure 3 Total Reflectance from Zinc Plated Copper and Zinc/Copper Plated Ni-Fe.
- Figure 4 Stacked Source for (CdZn)S.
- Figure 5 Flow Chart Showing the Available Options for the Deposition of (CdZn)S Films.
- Figure 6 Current-Voltage Curve for (CdZn)S/Cu₂S Cell #1.0353.111 Tested Under Sunlight.
- Figure 7 Capacitance Error of Measuring Circuit as a Function of Conductance. Actual measurements taken only at less than 2mS.
- Figure 8 Schematic cross sections of wet-process and dry-process CdS/Cu₂S cells after substantial heat treatment, showing effect of illumination on the depletion region.
- Figure 9 Dark Capacitance as a function of DC bias for solution (2.0899.113) and solid state (2.0899.112) process cells. Heat treated 45 hours at 150°C in H₂.
- Figure 10 Partial energy band diagram and charge density (both schematic) for a CdS/Cu₂S heterojunction, where quasi-Fermi level E_F crosses impurity level E_{T1} at χ_{T1} , varying as DC bias is changed from zero to reverse bias V_R . Change in depletion width w is slowed by loss of electrons from impurity level.
- Figure 11 The same conditions as Figure 10 except that E_F lies above impurity level E_{T2} for DC bias between zero and V_R . The change in w is faster.
- Figure 12 Capacitance decay at temperatures indicated. Cell 21065.111 under blue excitation until $t = 0$, and in dark for $t > 0$.
- Figure 13 Data from Figure 12 for the four lowest temperatures. C_0 = capacitance at $t \leq 0$, C_{00} = dark capacitance.
- Figure 14 Scanning Electron Micrograph of 16 second zinc plated copper; (a) as plated copper and (b) after brassification heat treatment.
- Figure 14 Scanning Electron Micrograph of 8 second zinc plated copper; (c) as plated copper and (d) after brassification heat treatment.
- Figure 14 Scanning Electron Micrograph of 4 second zinc plated copper;

(e) as plated copper and (f) after brassification heat treatment.

Figure 15 Glass Encapsulated micro-cell.

Figure 16 Loss in Short Circuit Current for Bare and Encapsulated Cells.

Figure 17 Defects observed on the glass films. Marker = $7\mu\text{m}$.

3. Introduction

Work on the production of an enhanced open circuit voltage CdS/Cu₂S cell described in the previous reports (1,2) has been continued. Because the relative increase in open circuit voltage is small (~6%) it became essential to determine the range of performance that could be expected from the standard cell production processes. Statistical information on this is presented. It has proved impossible to date to achieve an improved efficiency for CdS/Cu₂S cells using the enhanced open circuit voltage obtained with the planar junction cell. Losses in current and fill factor always exceed the gain in voltage.

Substantial progress has been made with (CdZn)S/Cu₂S solar cell. Improved film properties have led to higher efficiencies and also improvements in the stability of the current-voltage curves. An efficiency of 9% has been achieved in sunlight testing. The improvement over previous values is mainly due to achieving higher currents than previously recorded for mixed sulfide cells.

Detailed analysis of the influence of substrate reflectivity and anti-reflection coatings are presented. Further work on capacitance and transient capacitance measurements are given and some differences between solution and solid state cells are described.

Encapsulation using the electron beam deposited glass has continued. Edge defects, probably caused by the actual deposition procedures, have been shown to prevent good hermetic sealing.

4. Cell Production, Analysis and Testing

A major effort during the previous quarter was directed at establishing the limiting efficiency achievable with CdS/Cu₂S cells made on vapor deposited CdS by various processes. The full statistical analysis of those efforts is presented in this report.

Significant progress is reported for (CdZn)S/Cu₂S cells which have occurred because of improvements in the quality of the (CdZn)S films.

4.1 Development CdS/Cu₂S Solar Cells

Further refinements have been made in the production of cells using the solid state reaction to form Cu₂S. A major cell production effort using standard cell production techniques has been carried out from which the sensitivity of the cell efficiency to the various production parameters can be assessed.

Formation of Cu₂S By Means of a Solid State Reaction

A new system for the formation of Cu₂S by evaporation of CuCl has been developed. A dual chamber graphite source bottle similar to the CdS source is used rather than a quartz crucible previously employed. A complete description of the source design and characteristics can be found in Reference 3. The CuCl evaporation takes place with the CdS substrate held at 150°C. The reaction

takes place rapidly when the CuCl contacts the CdS. Reproducibility and uniformity of cells fabricated in this system are superior to those obtained previously.

A schematic of the essential components of the CuCl deposition system is shown in Figure 1. The source bottle is heated by a tantalum heater and the temperature is controlled by a thermocouple located in the wall of the bottle. The CdS samples are mounted on a copper plate that is radiatively heated by a tantalum heater similar to that used in the CdS system. The temperature is controlled from a thermocouple mounted on the copper plate. The evaporation rate and thickness of the CuCl are recorded using a quartz crystal monitor.

The procedure is:

1. Samples are cleaned and mounted on the copper plate.
2. The CuCl source material is prepared by the standard HCl-acetone method and approximately 3gm is added to the source bottle.
3. The system is pumped to a pressure of 1×10^{-6} torr.
4. The source is heated to 440°C and held at temperature for a minimum of five minutes before opening the shutter. The average deposition rate at this source temperature is nominally $400 \text{ \AA}/\text{sec}$. The substrate is simultaneously heated to 150°C .
5. The shutter is opened and CuCl is deposited to the required thickness.
Note: Pressure during deposition is 5 to 10×10^{-6} torr.
6. The source and substrate are allowed to slowly cool in the vacuum system until the source temperature is below 400°C , dry N_2 gas is then passed through the system to cool the source and substrate rapidly.
7. The substrate is removed from the system and CdCl_2 and excess CuCl

CuCl DEPOSITION SYSTEM

Figure 1. CuCl Deposition System

are rinsed from the sample with a 0.1 molar solution of NaCl and finally in D.I. water. The sample is then dried with a flow of nitrogen or argon gas.

All dry and wet-dry cells for Task 1 were processed using this system. The cell results are a clear demonstration of the reproducibility of this process. A problem with the graphite source bottle was identified during this period. The graphite is porous to the liquid CuCl and build-up of CuCl was found at the base of the heater. To correct this problem, a copper source bottle is being developed which has the additional advantage of fixing the stoichiometry of the CuCl.

The results of using this improved process with and without the subsequent addition of thin layers of copper will be described in the next progress report.

Reproducibility of Standard CdS/Cu₂S Solar Cells and Sensitivity to Production Parameters.

The standard CdS substrate evaluation process (SEP) produced 90 cells with AR coatings from 30 substrates during this period. Each substrate produced from one to four cells in this process. The substrates were grown under various conditions, but were all etched in 25% HCl for 30-40 seconds and barriered for 10 seconds in the standard CuCl bath. The cells made were optimized with H₂ or vacuum heat treatments and given either a single layer Ta₂O₅ or double layer TiO_x/SiO₂ AR coating.

The range of substrate formation conditions utilized are given below:

Zn plating time	4	or	8 sec.
CdS source temperature	900	to	1010°C
CdS substrate temperature	210	to	240°C
CdS deposition rate	0.6	to	2.0 μ m/min
CdS thickness	23	to	36
CdS resistivity	1	to	28 Ω -cm
CdS photoluminescence ratio	.2	to	1.3

All of the 30 substrates yielded at least one cell with an efficiency of 7.25% or greater as tested under ELH simulation at 87.5 mW/cm²

Maximum Efficiency (%)	# of Substrates	Yield (%)
over 8.5	15	50
over 8.0	23	77
over 7.5	29	97

The range of substrate conditions that gave cells over 8% in efficiency are as follows:

Zn plating time	4	or	8 sec.
CdS source temperature	910	to	1010°C
CdS substrate temperature	210	to	240°C
CdS deposition rate	0.6	to	2.0 m/min
CdS thickness	23	to	36 μ m
CdS resistivity	1.3	to	28 Ω -cm
CdS photoluminescence ratio	0.3	to	0.9

Within the ranges used no clear correlation between cells over 8% efficiency and the substrate growth conditions can be detected. (See Table 1.)

An examination of the yield of cells from the SEP process with respect to efficiency reveals the following distribution:

Maximum Efficiency (%)	# of Cells	Yield (%)
over 8.5	18	19
over 8.0	36	38
over 7.5	64	67
over 7.0	82	86

Table 2 shows the ranking of all the cells and their efficiency.

If the cells are further divided into the two types of antireflection coatings used (single layer Ta_2O_5 and double layer TiO_x/SiO_x), it is found that the yield is better for single layer AR. (See Tables 3 and 4.)

Single Layer AR (Total of 47 Cells)

Maximum Efficiency (%)	# of Cells	Yield (%)
8.5	14	30
8.0	25	534
7.5	35	74
7.0	41	87

Double Layer AR (Total of 48 Cells)

Maximum Efficiency (%)	# of Cells	Yield (%)
8.5	4	8
8.0	11	23
7.5	29	60
7.0	41	85

Also, the number of cells that "failed" during the AR coating is larger for the double layer AR than the single layer (by "failed", we mean cells whose efficiency was reduced by the AR coating.)

Thirteen cells failed the double layer AR. (27%)

Five cells failed the single layer AR. (11%)

Table 5 and 6 show the cell yield when the failures are removed.

Single Layer AR (42 Cells)

Maximum Efficiency (%)	# of Cells	Yield (%)
8.5	14	33
8.0	25	60
7.5	35	83
7.0	39	93

Double Layer AR (35 Cells)

8.5	4	11
8.0	11	31
7.5	28	80
7.0	34	97

In conclusion, it is found that within a broad range of preparation conditions there is no obvious sensitivity to the substrate processing parameters. However, there is a correlation between both efficiency and yield and the type of AR coating used. From this data, it is obvious that the single layer Ta_2O_5 AR coating is the better procedure to use.

If the AR process had been totally reliable approximately 95% of the cells would be over 7% efficiency using the standard cell production process.

SUBSTRATE	EFFICIENCY RANK	Zn PLATING TIME (sec)	CdS SOURCE TEMP. (°C)	CdS SUBSTRATE TEMP. (°C)	CdS GROWTH RATE (μ/min)	CdS THICKNESS (μ)	CdS RESISTIVITY (Ω-cm)	CdS PHOTO LUMINESCENCE RATIO	MAXIMUM EFFICIENCY (%)
21113	1	4	990	220	1.3	29.8	11.8	.4	8.98
21105	2	8	990	230	1.1	31.0	6.6	.7	8.85
21114	3	4	1000	220	1.4	29.2	12.3	.4	8.82
21122	4	4	930	220	.8	23.4	14.4	.3	8.81
21102	5	8	990	230	1.3	26.7	7.2	.6	8.80
21094	6	8	1000	240	1.0	26.3	12.8	.4	8.77
21110	7	8	1010	220	1.8	33.2	2.6	.5	8.75
21119	8	4	1000	220	1.5	31.8	5.6	.3	8.73
21127	9	4	995	220	1.1	25.3	23.3	.5	8.69
21128	10	4	995	220	1.4	28.7	11.3	.6	8.68
21106	11	8	990	210	1.1	32.4	3.3	.8	8.61
21092	12	8	1000	225	1.1	25.	18.9	.6	8.55
21109	13	8	1000	220	1.1	30.7	5.8	.9	8.53
21108	14	8	1000	210	1.6	35.8	1.3	.3	8.51
21112	15	4	1000	220	1.4	32.7	4.5	.5	8.50
21120	16	4	1010	220	2.0	32.1	22.1	.3	8.44
21088	17	8	1000	240	1.0	26.0	13.8	.6	8.35
21101	18	8	1000	210	1.5	30.3	3.8	.9	8.35
21131	19	4	980	220	1.0	24.5	28.3	.4	8.34
21125	20	4	1000	220	1.3	30.1	11.3	.9	8.15
21103	21	8	980	220	1.4	35.0	3.3	.6	8.14
21115	22	4	910	210	.6	29.8	9.2	.4	8.09
21111	23	4	1000	220	1.5	31.0	12.5	.4	8.01
21100	24	8	1000	230	1.2	29.2	7.0	1.0	7.99
21093	25	8	1000	225	1.4	28.3	7.2	.8	7.96
21095	26	8	990	225	1.1	26.8	11.8	.4	7.85
21085	27	8	995	225	1.1	27.0	1.0	1.0	7.84
21121	28	4	900	220	.7	28.2	12.9	.2	7.68
21130	29	4	980	220	1.2	32.2	8.2	.2	7.59
21087	30	8	1010	225	1.0	27.8	16.5	1.3	7.25

TABLE 1.

Substrates Ranked with Respect to Maximum Efficiency Cell Produced from SEP Process

EFFICIENCY			
RANK	SUBSTRATE	CELL	EFFICIENCY(%)
1.	21113.	.112	8.78
2.	21105.	.114	8.85
3.	21114.	.114	8.82
4.	21122.	.114	8.81
5.	21102.	.111	8.80
6.	21102.	.113	8.79
7.	21094.	.111	8.77
8.	21110.	.112	8.75
9.	21119.	.111	8.73
10.	21114.	.112	8.72
11.	21127.	.113	8.69
12.	21128.	.111	8.68
13.	21106.	.112	8.61
14.	21106.	.114	8.57
15.	21092.	.112	8.55
16.	21109.	.112	8.53
17.	21108.	.112	8.51
18.	21112.	.114	8.50
19.	21122.	.112	8.45
20.	21120.	.113	8.44
21.	21088.	.111	8.35
22.	21101.	.113	8.35
23.	21131.	.111	8.34
24.	21108.	.114	8.32
25.	21113.	.114	8.30
26.	21092.	.114	8.25
27.	21088.	.113	8.24
28.	21106.	.113	8.24
29.	21125.	.114	8.15
30.	21103.	.111	8.14
31.	21110.	.114	8.14
32.	21125.	.111	8.13
33.	21115.	.112	8.09
34.	21105.	.112	8.07
35.	21108.	.111	8.02
36.	21111.	.114	8.01
37.	21100.	.111	7.99
38.	21093.	.111	7.96
39.	21102.	.114	7.93
40.	21125.	.113	7.93
41.	21092.	.113	7.91
42.	21120.	.114	7.90
43.	21120.	.111	7.88
44.	21085.	.113	7.85
45.	21085.	.113	7.84
46.	21110.	.113	7.83
47.	21131.	.112	7.82
48.	21120.	.112	7.81
49.	21085.	.111	7.80
50.	21093.	.113	7.80
51.	21093.	.114	7.78
52.	21092.	.111	7.72
53.	21088.	.114	7.71
54.	21103.	.113	7.69
55.	21093.	.112	7.68
56.	21121.	.113	7.68
57.	21106.	.111	7.66
58.	21115.	.111	7.66
59.	21085.	.114	7.65
60.	21088.	.112	7.65

TABLE 2. SEP Process Cells Ranked with Respect to Efficiency

EFFICIENCY			
RANK	SUBSTRATE	CELL	EFFICIENCY(%)
61.	21100.	.113	7.62
62.	21130.	.114	7.59
63.	21103.	.114	7.56
64.	21121.	.114	7.51
65.	21121.	.111	7.48
66.	21131.	.113	7.45
67.	21103.	.112	7.44
68.	21131.	.114	7.42
69.	21110.	.111	7.38
70.	21100.	.112	7.34
71.	21095.	.111	7.29
72.	21112.	.112	7.28
73.	21108.	.113	7.26
74.	21087.	.114	7.25
75.	21101.	.112	7.16
76.	21087.	.112	7.15
77.	21121.	.112	7.13
78.	21101.	.114	7.05
79.	21115.	.114	7.04
80.	21109.	.113	7.02
81.	21085.	.112	7.00
82.	21109.	.111	7.00
83.	21123.	.113	6.98
84.	21109.	.114	6.93
85.	21101.	.111	6.84
86.	21102.	.112	6.66
87.	21127.	.112	6.54
88.	21087.	.113	6.43
89.	21130.	.112	6.14
90.	21087.	.111	6.09
91.	21130.	.111	5.62
92.	21105.	.111	5.52
93.	21100.	.114	5.35
94.	21105.	.113	4.72
95.	21111.	.112	4.56

TABLE 2. Continued: SEP Process Cells Ranked with Respect to Efficiency

EFFICIENCY			
RANK	SUBSTRATE	CELL	EFFICIENCY (%)
1.	21113.	.112	8.98
2.	21105.	.114	8.85
3.	21114.	.114	8.82
4.	21122.	.114	8.81
5.	21110.	.112	8.75
6.	21119.	.111	8.73
7.	21114.	.112	8.72
8.	21127.	.113	8.69
9.	21128.	.111	8.68
10.	21106.	.112	8.61
11.	21106.	.114	8.57
12.	21109.	.112	8.53
13.	21108.	.112	8.51
14.	21112.	.114	8.50
15.	21122.	.112	8.45
16.	21120.	.113	8.44
17.	21131.	.111	8.34
18.	21108.	.114	8.32
19.	21113.	.114	8.30
20.	21125.	.114	8.15
21.	21110.	.114	8.14
22.	21125.	.111	8.13
23.	21115.	.112	8.09
24.	21105.	.112	8.07
25.	21111.	.114	8.01
26.	21125.	.113	7.93
27.	21120.	.114	7.90
28.	21120.	.111	7.88
29.	21095.	.113	7.85
30.	21131.	.112	7.82
31.	21120.	.112	7.81
32.	21121.	.113	7.68
33.	21115.	.111	7.66
34.	21130.	.114	7.59
35.	21121.	.114	7.51
36.	21121.	.111	7.48
37.	21131.	.113	7.45
38.	21131.	.114	7.42
39.	21112.	.112	7.28
40.	21121.	.112	7.13
41.	21115.	.114	7.04
42.	21128.	.113	6.98
43.	21109.	.114	6.93
44.	21127.	.112	6.54
45.	21130.	.112	6.14
46.	21130.	.111	5.62
47.	21111.	.112	4.56
->			

TABLE 3. SEP Process Cells with Single Layer AR Ranked with Respect to Efficiency

EFFICIENCY RANK	SUBSTRATE	CELL	EFFICIENCY(%)
1.	21102.	.111	8.80
2.	21102.	.113	8.79
3.	21094.	.111	8.77
4.	21092.	.112	8.55
5.	21088.	.111	8.55
6.	21101.	.113	8.35
7.	21092.	.114	8.25
8.	21088.	.113	8.24
9.	21104.	.113	8.24
10.	21103.	.111	8.14
11.	21108.	.111	8.02
12.	21100.	.111	7.99
13.	21093.	.111	7.96
14.	21102.	.114	7.93
15.	21092.	.113	7.91
16.	21085.	.113	7.84
17.	21110.	.113	7.83
18.	21085.	.111	7.80
19.	21073.	.113	7.80
20.	21093.	.114	7.78
21.	21092.	.111	7.72
22.	21088.	.114	7.71
23.	21103.	.113	7.69
24.	21093.	.112	7.68
25.	21104.	.111	7.63
26.	21085.	.114	7.65
27.	21088.	.112	7.65
28.	21100.	.113	7.62
29.	21103.	.114	7.56
30.	21103.	.112	7.44
31.	21110.	.111	7.38
32.	21100.	.112	7.34
33.	21095.	.111	7.29
34.	21108.	.113	7.26
35.	21087.	.114	7.25
36.	21101.	.112	7.16
37.	21087.	.112	7.15
38.	21101.	.114	7.05
39.	21109.	.113	7.02
40.	21085.	.112	7.00
41.	21109.	.111	7.00
42.	21101.	.111	6.84
43.	21102.	.112	6.66
44.	21087.	.113	6.43
45.	21087.	.111	6.09
46.	21105.	.111	5.52
47.	21100.	.114	5.35
48.	21105.	.113	4.72

->

TABLE 4. SEP Process Cells with Double Layer AR Ranked with Respect
to Efficiency

EFFICIENCY			
RANK	SUBSTRATE	CELL	EFFICIENCY (%)
1.	21113.	.112	8.92
2.	21105.	.114	8.85
3.	21114.	.114	8.82
4.	21122.	.114	8.81
5.	21110.	.112	8.75
6.	21119.	.111	8.73
7.	21114.	.112	8.72
8.	21127.	.113	8.69
9.	21128.	.111	8.68
10.	21106.	.112	8.61
11.	21106.	.114	8.57
12.	21109.	.112	8.53
13.	21108.	.112	8.51
14.	21112.	.114	8.50
15.	21122.	.112	8.45
16.	21120.	.113	8.44
17.	21131.	.111	8.34
18.	21108.	.114	8.32
19.	21113.	.114	8.30
20.	21125.	.114	8.15
21.	21110.	.114	8.14
22.	21125.	.111	8.13
23.	21115.	.112	8.09
24.	21105.	.112	8.07
25.	21111.	.114	8.01
26.	21125.	.113	7.93
27.	21120.	.114	7.90
28.	21120.	.111	7.88
29.	21095.	.113	7.85
30.	21131.	.112	7.82
31.	21120.	.112	7.81
32.	21121.	.113	7.68
33.	21115.	.111	7.66
34.	21130.	.114	7.59
35.	21121.	.114	7.51
36.	21121.	.111	7.48
37.	21112.	.112	7.28
38.	21121.	.112	7.13
39.	21115.	.114	7.04
40.	21128.	.113	6.98
41.	21109.	.114	6.93
42.	21130.	.112	6.14

->

TABLE 5. SEP Process Cells with Single Layer AR and "Failed" Cells
Removed Ranked with Respect to Efficiency

EFFICIENCY RANK	SUBSTRATE	CELL	EFFICIENCY (%)
1.	21102.	.111	8.80
2.	21102.	.113	8.79
3.	21094.	.111	8.77
4.	21092.	.112	8.55
5.	21089.	.111	8.35
6.	21101.	.113	8.35
7.	21092.	.114	8.25
8.	21088.	.113	8.24
9.	21106.	.113	8.24
10.	21103.	.111	8.14
11.	21100.	.111	8.02
12.	21100.	.111	7.99
13.	21093.	.111	7.96
14.	21102.	.114	7.93
15.	21092.	.113	7.91
16.	21085.	.113	7.84
17.	21110.	.113	7.83
18.	21085.	.111	7.80
19.	21093.	.113	7.80
20.	21093.	.114	7.78
21.	21092.	.111	7.72
22.	21088.	.114	7.71
23.	21093.	.112	7.68
24.	21106.	.111	7.66
25.	21085.	.114	7.65
26.	21088.	.112	7.65
27.	21100.	.113	7.62
28.	21103.	.114	7.56
29.	21110.	.111	7.38
30.	21100.	.112	7.34
31.	21085.	.111	7.29
32.	21087.	.114	7.25
33.	21087.	.112	7.15
34.	21085.	.112	7.00
35.	21087.	.113	6.43
->			

TABLE 6. SEP Process Cells with Double Layer AR and "Failed" Cells
Removed Ranked with Respect to Efficiency

4.2 Development of (CdZn)S Solar Cells

The major advance this quarter has been in the quality of the (CdZn)S films which has resulted in improved cell performance. An efficiency of over 9% in sunlight has been achieved. Some studies of the influence of zinc on the Cu₂S formation process are reported and the effect of using a variety of substrates and deposition sequences on the resulting (CdZn)S film are described.

Material Analysis

The material analysis effort during the past quarter has been directed toward the investigation of the morphology of solution grown Cu₂S formed on the various substrates, (CdZn)S structures and an investigation for zinc gradients in the (CdZn)S films using photoluminescence as the probe. Results indicate that the Cu₂S morphology realized on bilayer films (i.e., (CdZn)S on CdS) deposited on copper substrates is not unlike that observed on CdS films⁽⁴⁾. The bilayer films generally did not exhibit the small grain regions which gave rise to the small sub-micron size semi-spherical Cu₂S intrusion morphology. Additionally, a similar Cu₂S morphology is observed for bilayer films deposited on nickel iron substrates, having appropriate zinc/copper plated interlayers. Preliminary device data indicate that utilization of the nickel iron substrate yields high efficiency (>8%) devices exhibiting better V_{OC} stability than achieved with films on copper substrates.

The existence of excessive amounts of zinc under the Cu₂S layer has been reported using atomic absorption spectroscopy and Auger analysis⁽⁵⁾. An investigation was conducted to determine if the excess zinc was being incorporated

in a way that it would increase the zinc concentration of the (CdZn)S film. To probe this effect, the shift in the exciton emission peak, which is known to shift to shorter wavelengths as the zinc concentration is increased,⁽⁶⁾ was utilized. Substrate 1-308 was used for the investigation and exhibited an as-grown exciton peak from the free surface at 470nm corresponding to a zinc concentration of 14%. A Cu₂S layer was formed on the surface by immersion in a boiling, saturated CuCl solution for 180 seconds as had been done by Burton⁽⁵⁾. It was estimated that the equivalent Cu₂S thickness formed in that time was in the range of 3-5 μm . The Cu₂S layer was subsequently removed using KCN and the emission spectra of the new surface measured. The exciton peak had shifted to a longer wavelength (475nm) corresponding to a zinc concentration of 10%. This result indicates that any excess zinc remaining under the Cu₂S after its formation does not become incorporated as part of the solid solution of (CdZn)S. However, the data do suggest that there is a through thickness compositional gradient with the zinc content decreasing towards the copper substrate.

Table 7 summarizes the results of an experiment to determine if the through thickness compositional gradient was evident in the as-grown film and if there was any lateral compositional gradients in the film. Shifts in the exciton peak as a function of etching time in HCl (25% at 60°C) indicated that there were indeed through thickness composition gradients. At a distance of 10 μm from the surface of the 23 μm thick (CdZn)S film (Substrate #1-308) the zinc concentration fell to about 10%. However, the data indicate that within experimental error there was no lateral compositional gradient across the 8 cm square (CdZn)S surface. Thus, although the concentric source creates a point source of Zn, Cd and S, and consequently lateral homogeneity across the film, variation in the

Zn to Cd ratio occurs as a consequence of inadequate rate control and leads to in-depth compositional gradients. Presently, some preliminary effort is being directed toward an alternative source design which will assure both lateral and in-depth compositional homogeneity.

TABLE 7
Zinc Concentration as a Function of Position
and Depth in (CdZn)S Film #1.308.

<u>Location on Substrate</u>	<u>Distance from as-grown Surface (μm)</u>	<u>Zinc Concentration</u>
Corner	0	14
Center	0	14
Side A	0	14
Side B	4.0	12
Side C	5.3	11
Side D	10.8	10

Materials Fabrication

As indicated previously⁽²⁾ optimization of cells prepared on NiFe substrate required the development Zn/Cu covering layers which would provide the proper morphology and substrate reflection. Figure 2 shows the SEM micrographs of the surfaces of a) NiFe substrate, b) NiFe substrate with 4 μm of electroplated copper, and c) (CdZn)S grown on the zinc-plated ($\sim 0.5 \mu\text{m}$), copper-plated NiFe substrate. It is particularly significant that the grain structure of the (CdZn)S films is uniform (average size 1-2 μm) in contrast to early (CdZn)S

(a)

(b)

Figure 2. Scanning Electron Micrographs x2000. (a) Nickle-Iron Substrate. (b) Copper Plated Ni-Fe.

(c)

Figure 2. Scanning Electron Micrographs x2000. (c) (CdZn)S on Zinc/Copper Plated Ni-Fe.

films on NiFe plated with a thin layer of copper ($\sim 1\mu\text{m}$) which exhibited very small grains. The copper plating was accomplished using first a Rochelle cyanide strike bath, followed by a CuSO_4 plating bath.

Figure 3 shows a comparison of the reflectivity spectrum for a zinc-plated ($\sim 0.5\mu\text{m}$), copper-plated ($\sim 4.0\mu\text{m}$) NiFe substrate with the spectrum for zinc-plated ($\sim 0.3\mu\text{m}$) copper (rough side.) Both spectra were taken on samples which had been heat-treated in vacuum for a time sufficient to insure that no further change would occur in the respective spectrum as a consequence of the interdiffusion of zinc and copper. A solar weighted average reflectance from the NiFe/Cu/Zn substrate was 78% as compared to 75% from the Cu/Zn substrate. Data from Cu_2S cells prepared both on CdS and (CdZn)S layers grown on high reflecting NiFe/Cu/Zn substrates will be presented in a later section.

In order to routinely use NiFe as the substrate, two specific technical problems will need to be addressed. Firstly, the process to produce the desired copper-plated NiFe has been problematic, and will require adequate development time to make it highly reliable. Secondly, owing to the poorer thermal conductivity of NiFe, there are temperature gradients across the substrate.

Table 8 shows substrate temperature data gathered at three points along the 10.8 cm diagonal during substrate heat-up. The data was compiled on three types of substrates: NiFe, NiFe with $4\mu\text{m}$ of plated copper, and electroformed copper. The data indicate temperature difference on the NiFe up to 102°C between the substrate corner and the substrate center. Conversely, the difference in temperature across the copper substrate is 8°C from corner to center, and about 29°C from

Figure 3: Total Reflectance from Zinc Plated Copper and Zinc/Copper Plated NiFe.

corner to center for the $50\mu\text{m}$ thick NiFe substrate plated on both sides with $4\mu\text{m}$ of copper. Presently a modified substrate holder assembly is being designed to minimize thermal gradients across the substrate.

Figure 4 shows a schematic drawing of newly designed "stack" source. This source, which has the same outer dimensions as the conventional CdS source, was designed to reduce the heat load, and consequently the pressure during (CdZn)S film growth. Additionally, it can be used interchangeably with the CdS source and thus can be used in the CdS growth system. This new source will be evaluated during the next quarter.

TABLE 8

Temperature distribution on various metal substrates ($^{\circ}\text{C}$).

<u>SUBSTRATE</u>	<u>CORNER</u>	<u>MID-POINT</u>	<u>CENTER</u>
Ni-Fe ($50\mu\text{m}$)	202	279	304
Ni-Fe ($50\mu\text{m}$) Cu ($4\mu\text{m}$)	202	225	231
Cu ($37\mu\text{m}$)	203	207	211

Cells on Bi-layer Films (CdZn)S/CdS on Copper.

Cu_2S formed by the wet process was utilized for the purpose of evaluating the various (CdZn)S-substrate structures. Table 9 shows device characteristic data for bi-layer CdS-(CdZn)S/ Cu_2S cells prepared on zinc-plated copper substrates. The bi-layer films were grown sequentially without breaking vacuum between the deposition of the separate layers. SEM micrographs indicate a tendency toward the bimodal distribution of grains on films for which the (CdZn)S layer is thicker than $10\mu\text{m}$.

- 29 -

upper orifice disk

quartz wool plug

ZnS chamber

lower orifice disk

CdS chamber

thermocouple well

STACKED SOURCE FOR (CdZn)S

FIGURE 4

For those films whose (CdZn)S layer is less than $10\mu\text{m}$, the grain structure is uniform (typical size $1-2\mu\text{m}$) and the light generated currents are 15-20% greater. The relatively low V_{OC} for 1-336-12 may be because the thin ($5\mu\text{m}$) (CdZn)S layer has been shunted by some areas where the Cu_2S junction is with CdS. As was the case with earlier bi-layer films on copper, these devices exhibited open circuit voltages which decayed with time.

TABLE 9
Cell results on CdS/(CdZn)S bilayers

Piece #	Thickness (μm)				Maximum	
	CdS	(CdZn)S	Zn	($\Omega\text{-cm}$)	V_{OC} (mV) @ 20 mA/cm^2	J_L (mA/cm^2) @ 100 mW/cm^2
10332-11	24	12	.06	21.9	.589	16.3
10333-11	24	14	.11	2.6	.600	16.3
10334-11	18	13	.10	4.8	.601	13.1
10335-11	18	10	.14	11.3	.609	16.3
10336-12	17	5	.12	7.2	.570	19.2
10337-11	32	7	.08	1.6	.579	19.0
10338-11	22	6	.06	2.6	.583	19.7

Cell on NiFe.

Table 10 shows the data from cells prepared on a CdS film grown on zinc plated ($0.3\mu\text{m}$)-copper plated ($4.0\mu\text{m}$)-NiFe, having the same properties as described in the earlier section. This film was grown in Evaporator I, using the conventional CdS source, to a thickness of $30\mu\text{m}$ and had a resistivity of

6.3 ohm.cm. The devices were fabricated using Cu_2S formed by the conventional wet process standard gridding, and no A-R coating. The cell data indicate that with an A-R coating state-of-the-art light generated currents could be realized on NiFe substrates which have been properly optimized for light economy and morphological structure.

TABLE 10
Cell Tests (Simulator)

<u>Cell #</u>	<u>V_{oc}(Volts)</u>	<u>J_L (mA/cm²) @ 100 mW/cm²</u>	<u>FF(%)</u>	<u>η(%)</u>
1-343-221	•508	21.2	70.8	7.6
1-343-222	•508	22.8	68.3	7.9

Table 11 shows the data from cells prepared on a $25\mu\text{m}$ thick $\text{Cd}_{1-x}\text{Zn}_x\text{S}$ ($x = .11$) film with a resistivity of 18 ohm-cm which was grown on a zinc/copper plated NiFe substrate prepared as previously described. The devices were fabricated using Cu_2S formed by the wet process, standard gridding, and a Ta_2O_5 anti-reflection coating. The device testing was conducted under natural sunlight conditions at the collimated intensities shown in the table. These cells exhibit currents which are comparable to the highest values observed in $(\text{CdZn})\text{S}/\text{Cu}_2\text{S}$ solar cells. Furthermore, these cells exhibited no change in V_{oc} after three minutes of illumination in the IEC simulator.

TABLE 11
Cell Tests (Outdoor)

<u>Cell #</u>	<u>V_{oc}(Volts)</u>	<u>J_L (mA/cm²) @ 100 mW/cm²</u>	<u>FF(%)</u>	<u>η (%)</u>	<u>Int. (mW/cm²)</u>
1-347-113	•581	21.4	69.8	8.7	85.7
1-347-114	•589	21.2	68.3	8.5	84.2

Plan for Material and Device Fabrication

Figure 5 shows a schematic of the options presently available for each of the first four layers of the six-layer (CdZn)S/Cu₂S device (grids and A-R not included.) For the purposes of planning an effort to achieve the most efficient (CdZn)S/Cu₂S device during the final quarter of the contract, it is necessary to select the process for each layer which is under control, reproducible, and optimized with respect to the other layers and the operation of the device as a whole.

To the extent that the preparation of the proper copper-coated, NiFe substrate is still under development, and since there are difficulties maintaining constant temperature over the substrate during film growth, the NiFe option was rejected for the present. Furthermore, since experience with sputtered ITO was somewhat limited and the results inconclusive, this option was also rejected for the present. Thus the first two layers were selected to be the matte side of the copper sheet with an 8 second zinc plate.

Both the single layer and bilayer approaches are considered potentially fruitful, although some very recent results with single layer films indicate that a uniform distribution of suitable grain sizes can be realized without resorting to the bilayer structure. With regard to Cu₂S formation, evaporated Cu₂S and dry process are presently rejected because of limited experience and low light generated currents respectively, although the former has yielded devices with stable open circuit voltages. Both the wet-on-dry and the conventional wet Cu₂S formation processes will be considered. The results of Task I will be factored in the ongoing decision-making process. The gridding will be conventional followed by a Ta₂O₅ anti-reflection layer.

Figure 5. Flow Chart Showing the Available Options for the Deposition of (CdZn)S Films

Some initial results are available on devices prepared as described above. Figure 6 shows the I-V curve of a cell prepared on a $27\mu\text{m}$ thick $\text{Cd}_{1-x}\text{Zn}_x\text{S}$ ($x = .23$) film with a resistivity of 16 ohm.cm. The grain structure of this film indicated no evidence of the bimodal distribution of grain sizes. This development was attended by a vendor change for the ZnS powder, and a comparative analysis of elemental impurity content is presently being sought. The device was fabricated using Cu_2S formed by the wet process, standard gridding and a Ta_2O_5 anti-reflection coating. The device was tested under natural sunlight at a global intensity of 85.6 mW/cm^2 . The light generated current pro-rated to 100 mW/cm^2 was 19.3 mA/cm^2 . The conversion efficiency of 9.1% is the highest achieved to date in a $(\text{CdZn})\text{S}/\text{Cu}_2\text{S}$ solar cell. The open circuit voltage of the cell was found to decay 13 mV from its initial value after three minutes of illumination in the IEC simulator.

During the upcoming quarter continued effort will be spent to further improve device efficiency using the selected set of fabrication processes. Additionally an evaluation of the stack source will be undertaken.

area=0.99cm²

intensity=85.6mW/cm² (global)

V_{oc}=0.633V

J_{sc}=16.45mA/cm²

FF=74.6%

Eff=9.1%

IEC80317

Figure 6. Current-Voltage Curve for (CdZn)S/Cu₂S
Cell #1.0353.111 Tested Under Sunlight

4.3 Electro-Optic Analysis and Modeling

The principal activity in analysis has been directed to the study of phot capacitance and capacitance. In addition, the EBIC study of solid state CdS/Cu₂S cells has been progressing. Considerable area-to-area variation in EBIC response has been noted and attempts are being made to develop a convincing quantitative theory.

The influence of zinc plating thickness and type of anti-reflection coating is reported to augment the data given in the previous quarterly report.⁽²⁾ Accuracy of capacitance measurements of solar cells.

These are based on the assumption that the cell may be represented by an equivalent circuit of a parallel resistor and capacitor. Systems used for these measurements are sensitive to the AC conductance of the cell, G , and require the phase angle $\theta = \tan^{-1}(\omega C/G)$ to remain constant or, at least, to vary in a known manner. In cells with $G \gg \omega C$, even small errors in θ can result in large errors in C .

In order to quantify this effect in the circuit described previously⁽²⁾ readings were taken on a standard capacitor in parallel with a variable resistor. Although the results can be expressed in terms of θ error, a more immediately useful quantity is capacitance error ΔC as it depends on measured G . This is shown in Figure 7, where it is clear that ΔC is nearly independent of C between 1 nF and 100 nF.

These results show that, because G is small in typical CdS/Cu₂S cells in the dark, it is not necessary to correct C for θ error, provided the DC bias is limited to about the range $-2 \text{ v} \leq V \leq +0.2 \text{ v}$. Under high illumination intensity.

Figure 7: Capacitance Error of Measuring Circuit as a Function of Conductance. Actual measurements taken only at less than 2mS.

a ΔC correction is needed for some cells, especially near the extremes of the quoted voltage range. For voltages farther from zero, ΔC can become so large that the interpretation of C is questionable. Measurements in such cells will be avoided in these voltage ranges.

Wet-process versus dry-process cells.

In a recent report on a related contract⁽⁷⁾ it was shown that intrusions of Cu_2S penetrate to a depth of $\sim 2\mu\text{m}$ between the CdS grains in $\text{CdS}/\text{Cu}_2\text{S}$ cells when the solution method ("wet process") is used to produce the Cu_2S barrier, but not where the solid-state method ("dry process") is used. The larger junction area produced in the wet-process cells is expected to be accompanied by a proportionally larger capacitance. Differences in C - V behavior are expected as well, because of differences in junction geometry and possibly because of differing response to heat treatment (HT).

Measurements of dark capacitance of cells with minimal HT (HT0) made by the two processes show $C(\text{wet})/C(\text{dry}) \sim 3$. This may give the approximate ratio of junction areas, and is consistent with the analysis by A. Rothwarf⁽⁸⁾. In order to quantify this behavior more closely, sets of cells were made on the same substrate (2.0899), four by the wet process and four by the dry process. Capacitance measurements were made on one of each of these after subsequent HT's each of 16 hr. at 150°C in H_2 . Table 12 gives some of the results.

TABLE 12

Effect of heat treatment (HT) on capacitance of Wet- and dry-process CdS/Cu₂S cells on the same substrate. Each HT was 16 hr. at 150°C in H₂.

C/A in nF/cm²

	cell 2.0899.113 (wet)		cell 2.0899.122 (dry)		$\frac{C(\text{wet})}{C(\text{dry})}$	
	C _{dark} /A	C _{AM1} /A	C _{dark} /A	C _{AM1} /A	dark	AM1
HT1	26.3	56.3	17.2	44.7	1.53	1.26
HT2	17.9	49.5	15.6	40.8	1.15	1.21
HT3	13.6	46.9	14.3	37.5	0.95	1.25
HT4	11.1	39.7	10.7	32.1	1.04	1.24

Increasing HT seems to equalize the effective junction area of the two types of cell in the dark. After HT1, C(wet)/C(dry) drops to ~ 1.5 , and after later HT's, the ratio becomes approximately one. Under AM1, in contrast, this ratio remains nearly constant at ~ 1.25 for HT1 to HT4. Figure 8 illustrates a possible mechanism, in which some of the excess junction area of the wet-process cell does not contribute to the capacitance at AM1, because deeper parts of the Cu₂S intrusions are not illuminated. This would produce a non-uniform electric field along the junction, with possible effects on current collection.

Decrease with HT of C_{dark} and C_{AM1} is approximately proportional in the dry-process cell, while C_{AM1} decreases noticeably more slowly than C_{dark} in the wet-process cell. This presumably reflects the relatively smaller decrease of depletion width in the wet cell, shown schematically in Figure 8.

Figure 8: Schematic cross sections of wet-process and dry-process CdS/Cu₂S cells after substantial heat treatment, showing effect of illumination on the depletion region.

The most striking difference in the two cells was in their C-V behavior in the dark. It has often been noticed that C_{dark} in conventional (wet-process) cells is nearly constant with V , at least in such a range as $-1 \text{ V} < V < +0.1 \text{ V}$. It is observed in the dry-process cell, however, that C_{dark} can show a fairly rapid decrease over a range of near reverse bias. Figure 9 shows this effect after HT3 as a plot of $(A/C_{\text{dark}})^2$ versus V for the two cells for which a complete set of measurements were taken.

While the wet-process cell 2.0899.113 shows C_{dark}/A almost constant at 13.7 nF/cm^2 in the range $-1.04 \text{ V} < V < +0.10 \text{ V}$, the dry-process cell 2.0899.122 has C_{dark}/A approximately constant at 13.2 nF/cm^2 at zero or near-forward bias, and at 10.1 nF/cm^2 for $V < .75 \text{ V}$. Between these ranges, especially for $-.68 \text{ V} < V < +.16 \text{ V}$, the capacitance of the latter cell varies so as to give a straight line in Figure 9. The data in this region give an effective donor density

$$N_D^* = \frac{2/q\epsilon\epsilon_0}{\text{slope}}$$

of $1.9 \times 10^{15} \text{ cm}^{-3}$ and a diffusion voltage (from the intercept) of $V_D = 0.61 \text{ V}$. The latter is in good agreement with the expected value.⁽⁹⁾ This agreement contrasts with the results from typical (wet-process) cells, where V_D^* , the extrapolated intercept, can be 1.5 V or more.⁽¹⁰⁾

Similar differences in C-V behavior in the dark were observed in cell 2.0899.113 and .122 after HT2, HT3, and HT4. Gradual changes in the limits of the region of large slope and of the value of the slope were seen in cell 2.0899.122, but not all the measurements were precise enough to quantify this.

IEC80312

Figure 9: Dark Capacitance as a function of DC bias for solution (2.0899.113) and solid state (2.0899.112) process cells. Heat treated 45 hours at 150°C in H₂.

Future measurements will be made with computer control of voltage increments and time allowed for C to come to a steady state, so that the results can be refined.

In order to explain the difference in C-V behavior of wet-versus dry-process cells, two possibilities need to be explored. The first is the effect of the sharp edges of the bottoms of the intrusions in the wet-process cells, shown schematically in Figure 8. Electric field near these areas may vary so as to weaken the dependence of C on V.

The second possibility is that energy levels of the charge compensator introduced into the CdS by HT may be different in wet- and dry-process cells. Figures 10 and 11 illustrate this difference schematically, showing change in energy band structure and charge distribution ρ as V goes from zero to reverse bias V_R . Figure 10 shows a mechanism similar to one investigated by Goodman in Au Schottky barriers on CdS(11) by which C-V variation is slowed because of crossing of the quasi-Fermi level E_F over a deep level at E_{T1} .

When the density of charge compensators N_{T1} is not much smaller than the native donor density N_D in the bulk CdS, $N_D^* = N_D - N_{T1} \ll N_D$, a change of bias from 0 to V_R will cause emptying of deep levels near the junction ($x < x_{T1}(V_R)$). The resulting increase in ρ near the junction prevents the depletion width w from increasing as much as it would if ρ were constant. Since C depends (inversely) on w rather than on x_{T1} , it also changes only weakly as bias goes from zero to V_R .

Figure 11 is different in the position of the trap level. Here E_{T2} remains lower than E_F as V moves from zero to V_R , and w increases faster than in Figure 10.

Figure 10: Partial energy band diagram and charge density (both schematic) for a CdS/Cu₂S heterojunction, where quasi-Fermi level E_F crosses impurity level E_{T1} at x_{T1} , varying as DC bias is changed from zero to reverse bias V_R . Change in depletion width w is slowed by loss of electrons from impurity level.

Figure 11: The same conditions as Figure 10 except that E_F lies above impurity level E_{T2} for DC bias between zero and V_R . The change in w is faster.

Therefore, C changes strongly. Note that, at some greater value of reverse bias, E_F will cross E_{T2} , and the slow variation of w will again be experienced. A large density of interface states N_I is shown in both Figure 10 and 11, suggesting that variation of C in forward bias would be slow because of changes in charge density analogous to those in reverse bias in Figure 10.

Further measurements and analysis are needed to determine the mechanism actually responsible for the C - V behavior of the CdS/Cu_2S cell and in particular the differences produced by wet versus dry process. The model proposed is only tentative, and it is not yet certain whether dry-process cells behave uniformly. Note that cell 2.0899.122 would have $E_F - E_{T2} \sim .7\text{eV}$, comparing Figure 9 and 11.

Hole trapping at deep levels in CdS investigated by capacitance transients

The increase in current collection efficiency of CdS/Cu_2S cells with increasing illumination intensity results from trapping of holes in the CdS near the junction. In order to determine how these hole traps behave, measurements of photocapacitance decay following abrupt changes in short-wavelength illumination have been performed on a typical IEC cell.

Cell 2.1065.111 was used. It had AM1 values of $J_{SC} = 15.5 \text{ mA/cm}^2$, $V_{OC} = .512\text{v}$, $FF = 61\%$, after HT in H_2 for 16 hr. at 170°C , 197 hr. at 15°C , and 16 hr. at 130°C . Capacitance, conductance, and current were measured with the circuits described in the last report⁽²⁾ in the dark, at AM1, and under blue light, over a range of temperatures from 77.5K to 293.0K . Blue excitation consisted of intense light from a tungsten-halogen lamp passed through filters to produce a band between about 365 nm and 585 nm.

Temperature variation was described earlier⁽²⁾. In order to observe capacitance decay, an electrically operated shutter, with 3.0 msec opening time and 4.2 msec closing time, was placed in the optical path. Outputs of the lock-in amplifier proportional to C and G were fed into a strip-chart recorder. Rise time following turning on the blue light was too short to be read accurately, so that only decay time following turning off the light was analyzed. Two runs, each lasting about 25 minutes, were made at each of six temperatures. Figure 12 shows the capacitance decay for one run at each temperature.

Time decay of the capacitance of p-n junctions has been extensively treated in the literature⁽¹²⁾. Following these treatments, it was expected that C^2 would vary exponentially with time. Figure 13 shows semi-log plots of normalized C^2 versus t obtained at the four lowest temperatures in the present experiment. The non-linear nature of the plot shows that some modification of the theory is needed. A possibility that suggests itself is that CdS contains hole traps with several energy levels in the gap, so that the curves in Figure 13 represent corresponding sums of exponentials. Attempts have been made to fit the results to sums of three or four exponentials, but the results were ambiguous. Further analytical work was begun on this question, and will be described in the next report.

Regardless of the relation of capacitance to time, it is obvious from Figure 12 and 13 that decay of hole trapping is not strongly dependent on temperature. This implies that, if decay is by emission of trapped hole from an impurity level to the valence band in CdS, the spacing $E_T = E_T - E_V$ must be small. The possibility of an alternative mechanism for emission of trapped holes will be explored further in later reports.

Figure 12: Capacitance decay at temperatures indicated. Cell 21065.111 under blue excitation until $t = 0$, and in dark for $t > 0$.

IEC80304

Figure 13: Data from Figure 12 for the four lowest temperatures.
 C_0 = capacitance at $t \leq 0$, C_{00} = dark capacitance.

IEC80305

Substrate Reflectivity and Anti-Reflection Coatings

Back surface reflectivity has been examined to improve the photon economy of the devices. Both zinc plating time and alternate interlayers between the CdS and copper substrate have been pursued. The goals were the following:

- (1) Maximize substrate reflectivity without altering the back CdS contact.
- (2) Substrate reflectivity should not vary after CdS is deposited.
i.e., the back surface reflectivity should not change during subsequent heat treatments of the devices.

Samples of the copper substrate were prepared for 4, 8 and 16 sec. plating time. The samples were given a heat treatment to simulate CdS deposition, and subsequent heat treatments in flowing argon to totally brassify the material. The substrate total reflectivity was measured after each heat treatment and the average solar reflectivity, $\bar{R}$, for AM 1.5 in the 0.40 to 1.00 μm range was calculated. The results are shown in Table 13. For the 4 and 8 sec. plated sample $\bar{R}$, changes less than 2% and is essentially at optimum reflectivity after the CdS deposition. The 16 sec. plated sample requires additional heat treatment before reaching optimal reflectivity. $\bar{R}$ for the 4 sec. plating time is 4 - 5% higher than the 8 sec. and 10 - 12% higher than the 16 sec. sample. SEM of the sample were taken before and after the first heat treatment, and are shown in Figure 14. Zn platelets can be seen on all three samples before any heat treatment. After heat treatment the 16 sec. sample may have a smoother surface than the 4 sec. sample, however, no differences in CdS film characteristics are observed.

a

b

FIGURE 14. Scanning Electron Micrograph of 16 second zinc plated copper;
(a) as plated copper and (b) after brassification heat treatment.

c

d

FIGURE 14. Scanning Electron Micrograph of 8 second zinc plated copper;
(c) as plated copper and (d) after brassification heat treatment.

f

Figure 14. Scanning Electron Micrograph of 4 second zinc plated copper;
(e) as plated copper and (f) after brassification heat treatment.

To examine the influence of back surface reflectivity on the light generate current density, J_L , a set of wet processed cells fabricated on CdS substrates with both 4 and 8 sec. plating time was selected.

Table 13
Reflectance of Zinc Plated Copper Substrate - Matte Side

ZINC PLATING TIME	$\bar{R}$ AFTER H.T. #1	$\bar{R}$ AFTER H.T. # 2	$\bar{R}$ AFTER H.T. #3
4	0.75	0.74	0.74
8	0.71	0.71	0.71
16	0.62	0.66	0.66

$\bar{R}$ = average solar weight reflectance at AM 1.5 from 0.4 to 1.0 μ m

Heat Treatments

- 1 Vacuum at 210°C - equivalent to a CdS deposition
- 2 30 hours at 150°C in flowing Argon
- 3 16 hours at 200°C in flowing Argon

The fabrication of the cells was the same for all cells; 40 sec. etch in 25% HCl at 60°, 10 sec. CuCl solution barrier, 31.5 line/cm gold grid and 0.5 μ m gold tabs. A single layer Ta₂O₅ antireflection layer was applied to all cells produced on 4 sec. - plated and most 8 sec. - plated substrates. Seven of the 8 sec. plated cells were given a double-layer, TiO_x/SiO₂, antireflection coating (analyzed separately, see Table 14.) Devices were all optimized for maximum efficiency using 150°C flowing hydrogen heat treatments. Cells from 20 different substrates were considered and only cells that had an efficiency greater than 8% were used for the analysis.

TABLE 14

Influence of Zinc Thickness and Anti-reflection Coating on the Maximum Light
Generated Current J_L , and the Light Generated Current at Maximum Efficiency, J_L^* .

Values Given for 100mW/cm².

Zinc Plate A-R Cell #	4 second Ta ₂ O ₅			8 second Ta ₂ O ₅				8 second TiOx/SiO ₂			
	J_L	J_L^*	η	Cell #	J_L	J_L^*	η	Cell #	J_L	J_L^*	η
21113.112	23.8	23.1	8.0	21105.114	23.2	22.8	8.9	21102.111	24.7	23.9	8.8
21114.114	24.1	23.4	8.8	21110.112	23.8	22.7	8.1	21102.113	24.4	23.9	8.8
21122.114	24.8	24.8	8.8	21106.112	23.4	23.3	8.6	21101.113	22.8	22.6	8.4
21114.112	24.5	24.3	8.7	21106.114	23.5	22.9	8.6	21106.113	21.9	21.9	8.2
21119.111	23.7	23.7	8.7	21109.112	22.8	22.6	8.5	21103.111	22.9	22.0	8.1
21127.113	25.2	23.8	8.7	21108.112	23.9	23.1	8.5	21108.111	22.8	21.8	8.0
21128.111	25.4	24.5	8.7	21108.114	23.5	23.3	8.3	21100.111	24.1	22.5	8.0
21112.114	23.8	23.8	8.5	21110.114	22.4	22.2	8.1				
21122.112	25.5	24.7	8.5	21105.112	21.1	21.1	8.1				
21120.113	23.4	23.4	8.4								
21131.111	23.9	22.9	8.3								
21113.114	24.0	23.2	8.3								
21125.111	25.0	23.2	8.2								
21125.111	22.7	22.7	8.1								
21111.114	21.6	21.6	8.0								
21137.111	22.7	22.7	8.0								
Averages	24.0 ± 1.1	23.5 ± 0.8			23.0 ± 0.8	22.7 ± 0.8			23.4 ± 1.0	22.7 ± 0.9	
Average all 8 second plate									23.2 ± 0.9	22.7 ± 0.8	

Table 14 is a listing of the maximum J_L obtained, the J_L at maximum efficiency and the maximum efficiency for all cells considered. The 8 sec. cells are further separated according to type of AR-coating. As can be seen from the data there is essentially no difference between the cells with different AR-coatings. The average $J_L(\text{max})$ and J_L^* (at J_L max) for the 4 second plate cells is $\sim 3\%$ higher than the values for all 8 second plate cells. Thus the 4 - 5% increase in reflectivity from the 4 second plating time results in approximately 3% increase in current.

Two different interlayers, silver and ITO between the copper and CdS were also examined to improve substrate reflection characteristics. Silver was deposited on the copper substrate followed by a standard CdS deposition. The substrate had a black appearance which was probably due to formation of silver sulfide during the initial stages of the CdS deposition.⁽¹⁾ Preliminary experiments using 1000-2000 Å of ITO as the interlayer showed:

1. A reduction in reflectivity after various heat treatments for both Cu/ITO and Cu/ITO/CdS samples;
2. J_L on a limited number of cells was comparable to or lower than standard CdS cells;
3. Yield of non-shortcd cells was poor, $< 25\%$.

Further experiments are required to understand the effect of heat treatments, both temperature and atmosphere, on the ITO as well as any interaction between the CdS and ITO.

4.4 Encapsulation for Improved Stability

During the previous reporting period a first order optimization of the glass layer deposition parameters was performed. It was found that the best structural integrity is obtained with a deposition rate of 5 Å/sec and a temperature of 150°C. These parameters were used, during the present reporting period, to encapsulate micro devices which then were tested for stability.

Device Fabrication.

An array of micro device were prepared with partial support from an ILZRO research contract. There are 256 devices of 1mm x 0.25mm in size on a square substrate of 25.4mm x 25.4mm. The position of each device on the substrate is determined by a row number p and a column number q, where p and q go from 1 to 16. Three types of grid structure are used on these devices:

- . Type 1: $p = 2n + 1$ one grid line
- . Type 2: $p = 2n$ and $q = 2n + 1$ two grid lines
- . Type 3: $p = 2$ and $q = 2n$ four grid lines

In the present investigation only devices with two grid lines were used.

In preparing these devices two additional precautions were taken to optimize the encapsulation. The first was to prepare CdS films on Fe-Ni/Cu/ITO substrates. Since Fe-Ni and CdS have similar expansion coefficient the bending of the array during glass deposition and heat treatments is greatly reduced. The other precaution was to prepare devices with highly polished surfaces. This was necessary to insure that the glass coverage was uniform.

The preparation of the devices consisted in the following steps:

1. Mechanical polishing of CdS; $6\mu\text{m}$ diamond $1\mu\text{m}$ Alumina, $0.05\mu\text{m}$ Alumina
2. Chemical polishing of CdS; in a mixture of glycerol and aquaregia(13).
3. Photolithographic definition of devices.
4. Formation of Cu_2S layer by solution reaction; duration 10 seconds.
5. 16 hours heat treatment in H_2 at 150°C .
6. Deposition of gold grids.
7. 120 hours heat treatment in H_2 at 150°C .
8. Glass (IEC 9658) encapsulation of the first 8 rows of devices.
Encapsulant thickness $2\mu\text{m}$; deposition rate $5 \text{ \AA}/\text{sec}$; temperature 150°C .

Figure 15 shows one of the devices after encapsulation.

Stability Tests.

The stability tests consisted in heat treating the array in a tube furnace in dry air (air, zero gas from Matheson) and measuring the decrease in short circuit current. During these tests 24 encapsulated and 24 bare cells were monitored. Before and after encapsulation the following values for the short circuit current density were obtained.

	<u>Before Encaps.</u>	<u>After Encaps.</u>
Bare cells	12.9 mA/cm^2	13.08 mA/cm^2 $\sigma = .56 \text{ mA}/\text{cm}^2$
Encapsulated cells	12.37 mA/cm^2	15.09 mA/cm^2 $\sigma = .65 \text{ mA}/\text{cm}^2$

Figure 15: Glass Encapsulated micro-cell

The higher J_{SC} obtained for the glass covered cells is mainly due to the AR effect of the glass layer.

Results and Discussion

Stability test results averaged over 24 bare and 24 encapsulated devices are summarized in Figure 16. For the 60°C heat treatment temperature the decrease in J_{SC} is relative to its value immediately after encapsulation (given above). On the other hand, for the 80°C heat treatment the decrease is relative to the J_{SC} values after 268 hours at 60°C, which are $12.07 \pm 0.47 \text{ mA/cm}^2$ and $14.13 \pm 0.62 \text{ mA/cm}^2$ respectively bare and glass covered cells.

It is quite obvious that the relative decrease in J_{SC} is the same for bare and encapsulated cells at both test temperatures. There is, for the 60°C test, an apparent increase in the difference between the average relative decreases in J_{SC} for encapsulated and bare cells. However, this trend is not conclusive since the 2 confidence regions, which are not shown in Figure 16, were found to overlap at all cases.

At the end of the aging tests, the devices were examined by Scanning Electron Microscopy. The micrographs of Figure 17 show the typical defects observed on the encapsulating glass layers. Cracks all along the edges of the glass layer (Figure 17a) were observed without exception on all the devices. The defects of the type shown in Figure 17b were found on only few cells. Even though the cell surface is approximately $40 \mu\text{m}$ from the edge of the glass layer, the cracks are of such extent that they are the main cause of the loss of hermeticity of the encapsulant. The probably cause of these cracks is the fact that the edge of

Figure 16. Loss in Short Circuit Current for Bare and Encapsulated Cells

(a)

(b)

Figure 17: Defects observed on the glass films.
Marker = $7\mu\text{m}$

the mask used during glass deposition is in contact with the surface of the array. As a result, when the mask is removed, the glass layer is cracked at the edges. A further observation on the aging test results of Figure 16 is that, for both temperatures, an initial rapid decrease in J_{SC} is followed by a much more gradual decrease during further heat treatments. This fact seems to indicate that the rate of decrease in J_{SC} is closely related to its initial value. e.e., to the initial state of the Cu_2S layer. Consistent with this, it is observed that, during 80°C heat treatment the magnitude of the decrease in J_{SC} is lower than that observed during 60°C heat treatment.

5. References

1. IEC Quarterly Progress Report XS-9-8309-1-01.
2. IEC Quarterly Progress Report XS-9-8309-1-02.
3. D. F. Brestovansky. M.S. Thesis, University of Delaware, 1980.
4. K. H. Norian and J. W. Edington. 14th IEEE Photovoltaic Specialist Conference. pp. 700-705 1980.
5. L. C. Burton. App. Phys. Letters 35, 780, 1979.
6. IEC Final Report XR-9-3063-1-FR, December, 1979.
7. IEC Progress Report XS-9-8310-1-01, 1980.
8. IEC Technical Report NSF/RANN/AER72-03478A04/TR76/5.
9. A. Rothwarf, J. E. Phillips and N. C. Wyeth. 13th IEEE Photovoltaic Specialist Conference. pp 399-405, 1978.
10. N. C. Wyeth and A. Rothwarf. J. Vac. Sci. & Tech. 16, 1402-1405, 1979.
11. A. M. Goodman. J. App. Phys. 34, 329, 1963.
12. C. T. Sah, IEEE Trans. Electron Devices ED-24, 410, 1977.
C. T. Sah, L. Forbes L. L. Rosier and A. F. Tasch. Solid State Electronics, 13, 759, 1970.
13. A. Foundeus, et.al., Metallography 5, 307, 1972.

APPENDIX

CdS/Cu₂S and CdS/Cu-Ternary

Report Distribution List

A William W. Anderson
Lockheed Missiles & Space Co. (0/5254)
3251 Hanover Street, Bldg. 202
Palo Alto, CA 94304
/493-4411 Ext. 45014

Nagappan K. Annamalai
Clarkson College of Technology
Potsdam, NY 13676
315/268-6538

B Karl W. Boër
College of Engineering
University of Delaware
Newark, DE 19711
302/738-8048

Richard H. Bube
Stanford University
Department of Materials Science
Stanford, CA 94305

Larry C. Burton Univ.
Virginia Polytechnic Institute & State
Electrical Engineering Department
Blacksburg, VA 24061
703/961-6693

C Wen S. Chen
Boeing Aerospace Company
P. O. Box 3999 MS 88-43
Seattle, WA 98124
206/773-1074

Chevron Research Company
ATTN: Lee Donaghey
P. O. Box 1627
Richmond, CA 94802

Alton H. Clark
University of Maine
Bennett Hall
Orono, ME 04469
207/581-2717

Colorado State University
ATTN: Kenneth A. Jones
Electrical Engineering Department
Fort Collins, CO 80523

D Satyen Deb
Solar Energy Research Institute
1617 Cole Boulevard
Golden, CO 80401
303/231/1369; Fts 327-1369

E J. W. Edington
Mechanical & Aerospace Eng. Dept.
University of Delaware
Newark, DE 19711

F Erwin Fischer-Colbrie
Lawrence Livermore Lab/DOE
East Avenue L 156
Livermore, CA 94550
415/422-8704; Fts 532-8704

David L. Fleming
Sperry-Univac
Box 3525
St. Paul, MN 55165
612/456-3163

L Lawrence Livermore Laboratories
ATTN: Dr. J. H. Yee
University of California
Livermore, CA 94550

John Leong
Solar Energy Research Institute
1617 Cole Boulevard
Golden, CO 80401
303/231-1392; Fts 327-1392

Joseph J. Loferski
Brown University
182 Hope Street
Division of Engineering
Providence, RI 02912
401/863-2870, 2675

Virginia E. Lowe
Boeing Aerospace Company
P. O. Box 3999
Seattle, WA 98124

M H. Paul Maruska
Exxon Research & Engineering Co.
P. O. Box 45
Linden, NJ 07036
201/474-2054

Guy D. McDonald
Globe-Union, Inc.
5757 N. Green Bay Avenue
Milwaukee, WI 53201
414/228-2371

John D. Meakin
Institute of Energy Conversion
1 Pike Creek Center
Wilmington, DE 19808
302/994-7155

Reid A. Mickelsen
Boeing Aerospace Company
P. O. Box 3999 MS 88-43
Seattle, WA 98124
206/773-1074

John B. Mooney
SRI International
333 Ravenswood Avenue
Menlo Park, CA 94025
415/326-6200 Ext. 2906

N Naval Research Laboratory
ATTN: Dr. A. P. Defonzo
Optical Techniques Branch
Washington, D.C. 20375

P Larry Partain
Lawrence Livermore Lab L-156
Livermore, CA 94550
415/422-0545

M. Prince
Department of Energy
Division of Solar Technology
600 E Street, N.W.
Washington, D.C. 20845

S John R. Szedon
Westinghouse R&D Center
1310 Beulah Road
Pittsburg, PA 15235
412/256-3394

T John A. Thornton
Telic Corporation
1631 Colorado Avenue
Santa Monica, CA 90404
213/828-7449

V University of Vermont
ATTN: Prof. R. L. Anderson
Dept. of Electrical Engineering
Burlington, VT 05401

Patent Office*: Mr. Paul Gottlieb
Assistant Chief
Office of Patent Counsel
U.S. Department of Energy
9800 South Cass Avenue
Argonne, IL 60439