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**A MULTI-SITE MAGNETOTELLURIC MEASUREMENT
SYSTEM WITH REAL-TIME DATA ANALYSIS**

MASTER

by

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A MULTI-SITE MAGNETOTELLURIC MEASUREMENT
SYSTEM WITH REAL TIME DATA ANALYSIS

Publication No. 210

A magnetotelluric measurement system has been designed to provide a more cost effective electrical method for geothermal and mineral exploration. The theoretical requirements and sensitivities of the magnetotelluric inversion process were specifically addressed in determining system performance requirements. Significantly reduced instrument noise levels provide improved data quality, and simultaneous measurement at up to six locations provides reduced cost per site.

Remotely located, battery powered, instrumentation packages return data to a central controlling site through a 2560 baud wire-line or radio link. Each remote package contains preamplifiers, data conditioning filters, and a 12 bit gain ranging A-D converter for frequencies from 0.001 Hz to 8 Hz. Data frequencies above 8 Hz are processed sequentially by a heterodyne receiver to reduce bandwidth to within the limits of the 2560 baud data link. All variable amplifier gains, filter settings, and operational modes at the remote packages are determined by commands sent from the central controlling site over

a 600 baud telemetry link which also provides a timing reference for the remote packages to insure simultaneous sampling of data at all locations. A Motorola 6800 microprocessor at each site provides local control and data formatting.

The central data collection site provides overall control for the entire system. A Motorola 6800 receives incoming data and controls all peripheral devices at the central site. The system operator interacts with the system through a CRT terminal, and he receives hard copy from a matrix graphics printer. Data from the remote packages may be recorded in time sequence on a magnetic tape cartridge system, or an optional Hewlett-Packard 2MX minicomputer can be used to perform real-time frequency analysis. The results of this analysis provide feedback to the operator for improved evaluation of system performance and for selection of future measurement sites.

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1. INTRODUCTION

Expanding requirements for minerals and particularly petroleum in the past fifty years have prompted the development of a number of techniques for geologic exploration. As demands increased, easily located surface deposits were depleted and random searches for deeper deposits proved too costly. Interest developed in various acoustic and electrical methods which seemed to offer cost effective survey techniques. In 1953 Louis Cagniard published his work on the magnetotelluric method which combines magnetic measurements and telluric (earth current) measurements in a passive technique for the determination of electrical impedance versus depth. [4] Magnetotellurics uses natural or cultural (if sufficiently distant to satisfy the source modelling assumptions) magnetic fields as a source which induces electric fields and thus telluric currents in the earth. The ratios and relative phases of the magnetic and electric fields are related to the impedances of the earth at the measuring point. Because of the skin depth of lossy dielectrics in time varying fields, the higher frequencies produce information about the near surface properties of the geological formations. Greater penetration of lower frequencies yields information about the formations at greater depths.

The ratios of corresponding Fourier coefficients of the electric and magnetic fields form a set of impedances where each impedance value represents a composite of the impedances of all geologic layers which are penetrated by the fields at the corresponding

frequency. Thus the higher frequencies yield an impedance for the near surface geological formations while lower frequencies include this effect with increasing information from greater depths. The impedances are commonly converted to a set of apparent resistivities which have units of resistivity but retain the phase of the impedance. [21]

Much effort has been directed toward development of analytical inversion techniques to transform the apparent resistivities (versus frequency) to the actual resistivity versus depth. Earlier work assumed geologies which were horizontally uniform and distinctly layered in depth. Theoretically the apparent resistivities could be mapped into a unique layered model which corresponded to actual geological structure. However, because the skin effect decreases field strength exponentially with depth, the apparent resistivities will not have abrupt changes with frequency. Thus the depths of geologic layers were estimated from gradual changes in the apparent resistivities. Mathematical processes of this type, while theoretically unlimited in accuracy, are highly sensitive to and degrade rapidly in the presence of noise.

More recent work on single dimensional (uniform in horizontal directions) inversion has replaced the layered model with a continuous model. This approach eliminates the tendency to force resolution on the inversion when it does not exist in the data. However, good data quality is essential to provide the best resolution possible. The ultimate value of magnetotellurics in exploration will be determined largely by the quality of the electric and magnetic field measurements.

Extensive work has been done in modelling more complicated geologic structures, and solutions to numerous specific cases are available, however the resolving power of the technique remains limited by the accuracy of the initial measurements. Because of the magnitude of this problem, the data inversion process will not be treated here. Suggested references on inversion include Bostick [3], Ku [9], Patrick [16], and Wu [23]. This work will be limited to the development of a measurement system which provides the best achievable measurement accuracy in a system which could be used for a cost effective magnetotelluric exploration program.

1.1. Practical Aspects

For a number of years the lack of adequate transducers and instrumentation presented the greatest obstacle to further development of the magnetotelluric technique. In many cases the signal levels were below the inherent noise level of the instrumentation systems of that period. In this section the signal characteristics and the evolution of instrumentation will be discussed.

1.1.1. Magnetic Field Signals and Transducers

The magnetic signal energy is very low across the entire MT frequency band, and the signal characteristics vary with the source. The primary natural source of electromagnetic energy in the lower magnetotelluric (MT) frequencies (below about 1 Hz) is solar wind. The nuclear particle stream which makes up solar wind strikes

the earth's upper atmosphere and induces low frequency variations in the earth's fields. The energy at the higher MT frequencies (1 Hz to 1000 Hz) comes primarily from thunderstorms, and it consists of a series of impulses. Very near a thunderstorm the impulses may reach many volt-seconds, but with increasing distance, the high frequency energy decreases to a level below the background cultural noise at these frequencies. A plot of the derivative of spectral density versus frequency for magnetic field below 10 Hz is shown in Figure 1. (The derivative is shown because the induction coil transducer produces an output proportional to the derivative of the applied field, and therefore the plot represents the signal distribution at the amplifier input.) Figure 1 is an average of data from Sims [20] and from the 1977 Utah survey by the Geomagnetism Research Lab at The University of Texas. Energy at frequencies above 10 Hz is impulse like, and although averages could be shown, they suggest a continuity in time which does not exist. Special techniques for processing signal in this band are discussed in Section 5.9.

The random nature of the signals in the MT frequency bands makes a wide system dynamic range necessary to provide sufficient gain while preventing system saturations. The total variations in signal level over a long interval are so large that reasonable system implementations are unable to provide sufficient dynamic range. Therefore a maximum dynamic range (for short term variations) should be combined with additional gain control which remains fixed on the short term but which may be varied for day to day variations in energy.

FIGURE 1: B FIELD POWER SPECTRAL DENSITY

Although a number of magnetic field transducers are available, only those providing vector component information are useful for magnetotellurics since the inversion requires magnetic and electric field vector data. Total field magnetometers can be adapted by adding permeable material to produce directional sensitivity, but the resulting transducer provides no advantage over the inherently directional transducers. MT requires data at very low but non-zero frequencies. Because of the very large DC component in the earth's magnetic field, DC sensitive transducers must have exceptionally wide dynamic range to provide adequate sensitivity while remaining unsaturated. Induction coil magnetometers are particularly well suited to magnetotellurics because they are highly directional, and they have no sensitivity to DC. Early measurements were made with very large air core coils which achieved sensitivity by physical size. However the coils were difficult (if not impossible) to move. Construction of the vertical component sensor consisted of burying a large coil in a shallow trench in the ground. Horizontal component sensors were more challenging.

Development of a more reasonable magnetometer was necessary for any practical application of MT. The use of a highly permeable core (mu-metal in particular) enabled the design of a sensor with adequate sensitivity in an acceptable size and weight. Additional physical size can increase the transducer's signal to inherent noise ratio through increasing the number of turns of wire with constant resistance (bigger wire) or through increased core size. Added

sensitivity with a fixed coil size (by adding turns of smaller wire) produces an increased resistance and thus increased Johnson noise. Therefore, the coils are normally made as large as is practical for their applications. The best compromise of resistance and sensitivity is determined by the characteristics of the preamplifier that is used with the coil. In any case, the signal from the coil is very small compared to thermocouple potentials between dissimilar metals, chemically induced potentials due to contaminated contacts, voltages resulting from the Barkhausen effect in the coil's core, and voltages produced by flux changes as permeability of the core varies with temperature. The earth's static field can also generate voltages greater than the MT signals if either the coil or the wire leading from the coil is allowed to move. These noise sources must be controlled if useful magnetic field measurements are to be made.

1.1.2. Electric Field Measurement and Transducers

The electric field signal is related to the magnetic field by the earth's impedance. Figure 2 shows spectral density of E field for a homogeneous earth with resistivity of one ohm-meter. (Calculated from the B field spectral density shown in Figure 1.) This one ohm-meter impedance is lower than average, but it produces signal levels which are frequently encountered in actual magnetotelluric exploration.

The electric field measurement is made by determining the potential difference between physically separated points on the earth's surface. It is necessary to make electrical contact with the earth at

FIGURE 2: E FIELD POWER SPECTRAL DENSITY

these points. The ideal transducer would produce a zero impedance contact with the earth and would produce no contact potential at the interface (and none internally).

Early testing was done with aluminum rod electrodes which were readily available and offered a low impedance contact. The first tests produced very high energy levels which were independent of the electrode separation (thereby defying the expected behavior of earth currents). As a test, the electrodes were buried in a soil filled plastic pail (which insulated the test soil from earth currents), and they continued producing roughly the same output levels. The source of this energy was identified as chemical action between the aluminum rod and components of the soil. This chemical reaction between the electrodes and the surrounding soil continues to be one of the most significant problems in electric field measurements at low frequencies. If uncontrolled, the chemically produced potentials and/or thermocouple potentials can invalidate E field measurements.

Past work has indicated that the relatively inactive metals (mainly lead) work well as electrodes in some applications. Buffered electrodes utilizing a metal electrode immersed in a saturated salt solution of the same metal have proved most satisfactory in general use. The salt solution contacts the earth through a porous ceramic disk which contains the fluid but allows electrical contact. The salt solution separates the metal electrode from the soil, and thus it decreases the effects of chemical reactions between soil components and the electrode's metal contact. The buffered electrode introduces several problems associated with the solution. It is more complex and more costly; it is

more fragile; it tends to degrade with time (salt concentration decreases as diffusion occurs to soil moisture); and the salt solution may be highly toxic (as is cadmium chloride, a popular buffer).

Neither type of electrode can provide the desired low impedance because of the resistivity of the soil. Since the electrode provides a relatively small contact area, the soil resistivity produces a finite, and sometimes very large impedance. (It is commonly 50 to 5000 ohms, and sometimes 100K ohms or higher.) Soil moisture increases conductivity, and in very dry areas where soil resistivity is excessive, introduction of water or salt water can reduce the contact resistance significantly while not directly affecting the data quality (because of the relatively small area affected compared to the electrode separation). However, a secondary effect can produce noise. The water added to the electrode diffuses into the surrounding soil and dries from the surface. As this occurs, the impedance of the electrode changes with time. The impedance change creates a voltage change if the measuring amplifier has appreciable bias current.

Several types of electrodes are in general use because none has been shown to be clearly superior to the others in all applications when used with available preamplifiers. As preamp input impedances are improved, more stable (although possibly higher impedance) electrodes may be identified or developed.

1.1.3. E Field Source Characteristics and Preamplifiers

The frequency band to be measured (0.001 Hz to 1000 Hz) includes signals from three main sources. The signal below 0.1 Hz is primarily energy from solar emissions, and is roughly continuous in nature. The natural signals above about 0.1 Hz result from electrical storm activity, and are characterized by predominance of impulses with a very low background energy level. Total energy above 0.1 Hz varies widely depending on geographic separation between the measurement site and the nearest electrical storms. The third source of energy is the cultural power distribution systems. This source provides a very high energy level (relative to the other sources) at 50 and 60 Hz and higher harmonics of these frequencies. In most cases the source of this energy is too near the measurement site and too complex in geometry to allow the plane wave assumption used in magnetotelluric analysis. Thus the cultural energy is normally treated as a noise, and measurements are made away from these frequencies and their harmonics.

The amplifiers for the E field system must therefore provide very high input impedance (to make electrode impedance changes negligible), very low noise (because of the low energy levels below 0.1 Hz), and excellent dynamic range (to prevent saturation from lightning strike impulses). Additionally, the E field amplifier is normally a differential amplifier so that the layout of the electrodes is not restricted. (A pair of single ended amplifiers could measure two components of E field if the ground point were placed in the corner of a three electrode "L".) These requirements make E field

amplifier design one of the most challenging problems in magnetotelluric instrumentation.

1.2. Evolution of Instrumentation

Early amplifier systems were built with commercial operational amplifiers using vacuum tubes for the linear gain stages and magnetically driven resonant reed switches for DC stabilization or signal modulation. The noise performance of these systems was poor and the physical size and power requirements were quite large. As newer electronic amplifying devices were introduced, they were incorporated into the magnetotelluric systems. The transition from tubes to semiconductor linear devices removed the large power requirements and presented an improved noise level. As integrated circuit operational amplifiers were introduced and improved, they were incorporated into new linear electric field amplifier systems. While these systems were not equal to the chopper system in noise performance, they were only slightly higher in noise level, and they were far superior in reliability. Being linear, they offered an inherent solution to the problem of high frequency input signals aliasing about the chopper frequency. (The electric field transducer is wide band, unlike the magnetometer coils which are inherently band pass devices.) With the introduction of the linear solid state amplifiers, reliability improved to such a level that only a lightning strike near an electrode would be expected to result in any failure in the electric field system.

The very low signal levels of the magnetic field system required that modulation (chopping) be used to achieve adequate

performance of the gain stages. For many years the resonant reed switches were used to translate the input signals to about 100 Hz for improved gain stability in the linear amplifier stages. These reeds were microphonic and had short service lives. As they degraded, they would produce increasing noise levels which were frequently undetected by the operator until data quality had deteriorated severely. However no substitutes were available until the insulated gate field effect transistors (IGFETs or more commonly MOSFETs) became available in the late 1960's. Early in the 1970's, development of MOSFET chopper amplifiers was begun. These amplifiers offer a greater range of chopping frequencies because they are not limited by mechanical motion and inertia. Therefore chopping frequencies can be selected to better match the optimum frequency for the linear gain stages. MOSFET choppers eliminated sensitivities to vibration and physical positioning, and they offer very great improvements in reliability. The expected time between failures was extended to such an extent that amplifier failures and degradation have ceased to be a problem in field use of MT systems.

1.3. Recording Techniques

Early data was recorded on continuous analog strip chart recorders and analog magnetic tape recorders. The development of digital computers provided a needed tool for the processing of MT data, and manual digitizing from the strip charts provided the necessary data link. Later, automatic digitizing schemes provided better data quality and quicker conversion of data from the analog tapes. Progress in A/D conversion resulted in a transfer of the conversion process from the

manual conversion in the lab to a central computer facility; then back to the lab as dedicated converters became economically feasible. The next step placed the conversion in the central field location, and now the conversion will be moved to the transducer location. Each step moved the conversion nearer the transducer, and thereby reduced the analog processing of the signal. Since each analog process necessarily adds noise to the data, and digital storage and transmission do not, the signal quality improved with each move of the conversion process. Simultaneously the system maintenance and set-up time was reduced because digital systems typically do not have the precision components and adjustments of data quality analog systems.

As the digital conversion process moved to the field, the analog recording was initially retained both as a backup and to allow analog processing of the continuous data. However, the superiority of digital data processing soon became apparent, and the reliability of the digital recorders made the analog back-up unnecessary.

1.4. Maturing of a Technique

By the mid 1970's advances in the areas of signal measurement, data recording, and data processing had reduced the amount of instrumentation and support equipment for field exploration by a factor of about five to ten and had reduced the maintenance and repair time from near 50% of a field trip to a insignificant part. Replacement of analog tapes with the more reliable digital systems eliminated rituals of tape processing, magnetic head cleaning, and recorder set-up between

runs. Progress had resulted in a system which could feasibly be run by a technical but non-engineering staff. Feasibility of the technique had been proven, but cost effectiveness was not certain. A few commercial companies had begun using MT, but the very high cost of developing the needed instrumentation, and the relatively slow process of acquiring data with available systems delayed utilization of the technique by additional companies.

Sensing that MT might provide a useful tool in petroleum and geothermal exploration, the Energy and Resources Development Agency (ERDA), now the Department of Energy (DOE), sought proposals for development of a prototype system which would utilize state-of-the-art electronics devices and systems to produce a cost effective MT exploration system. The development would be published to enable companies, universities, and other governmental units to enter the field of MT exploration without the very large expenditures associated with an independent development of a full MT system. Hopefully the DOE expenditure would be justified by an increased production of energy as a result of expanded use of MT as a geophysical survey tool.

The Geomagnetism Research Lab at the University of Texas at Austin submitted a proposal for the DOE contract in the spring of 1977 and was awarded the contract. Work began 1 September 1977. This document is intended to explain the design goals, the necessary compromises, and the resulting hardware. Software structure and operating procedures will be explained. In some areas, alternate implementations will be discussed.

2. SYSTEM OBJECTIVES

The intent of the Department of Energy (DOE) contract and the goal of this design effort was the development of a state-of-the-art magnetotelluric (MT) measurement system which would maximize the ratio of geophysical information returned per dollar spent in MT exploration. A secondary goal was the production of a system which could be duplicated at minimum cost to provide a less expensive entry into MT exploration. Specific design goals for the system are shown in Table 1.

The primary cost of MT exploration is the labor expended and not the equipment used in field work. Thus the speed of measurements and the quantity of data gathered largely determine the cost of exploration. As an example, assume that the cost of labor for a field crew is \$1000 per day, that total equipment cost is \$100,000, the life of the equipment is five years, and the utilization is 50%. The cost of the equipment under these conditions is slightly below 10% of the total cost (ignoring the time value of money).

The magnetotelluric method is necessarily a slow technique because of the very low data frequencies involved. The period of the lowest frequency used is 16.7 minutes, and in order to obtain the desired 33% bandwidth, a minimum of six cycles is needed because the Hanning window applied to the data doubles the effective bandwidth. This approaches two hours. In practice, measurement time at each site is usually extended to at least four hours to allow for initial transients and to provide more than a single sample at the lowest frequency.

TABLE 1

OUTLINE OF SYSTEM DESIGN GOALS

1. One magnetic and six (max) electric field sites, or other configurations of up to 16 data channels
2. Minimum inherent system noise & maximum sensitivity
3. Real time processing of data (a system option)
4. Digital recording of raw data
5. Maximum reliability
6. Hardware tolerance of any software condition
7. No power supply sequencing requirements
8. Maximum commonality (minimum number of subassemblies)
9. Continuous clock synchronization
10. Non-simultaneous start-up of electric field sites
11. Audio frequency data communications
12. Minimum power consumption of remote sites (battery power)
13. Absence of any stable non-operating states (no reset needed)

With a minimum measurement time of four hours, it is necessary to collect as much simultaneous data as possible and to extract maximum information from that data. Therefore simultaneous measurement at multiple sites became a system design goal. In addition to reducing the cost per site, multiple simultaneous measurements allow cross processing of data from physically separated sites for noise reduction. [5]

An ideal data collection system would have many sets of five channel (three magnetic and two electric field) instrumentation systems, but the cost of induction coil magnetometers and the labor involved in their installation at each site makes such a configuration expensive to purchase and to use. In most locations the magnetic field is more nearly uniform over a large area than is electric field. Since the near surface geological details produce information in the electric field, processing of multiple electric field sites with a single magnetic field site can produce additional detail with a relatively small increase in equipment and labor. Although there is no particular constraint, an upper limit of six dual channel electric field systems was selected to establish the performance level necessary in the central data collection processor and the real time analysis processor. Six electric field sites can provide reasonable coverage of an area over which the magnetic field uniformity can be assumed, and they provide sufficient data to allow cross correlation of electric field data between adjacent sites if the technique is to be used. Thus the upper limit of the design was set at a single three component electric field sites running simultaneously. (Some E field sites

could be replaced with additional remote B field sites with no significant design changes.)

Accuracy of geological models produced by the inversion of MT data degrades rapidly with increasing noise in the data. Since only the best quality data produces adequate resolution in the MT inversion process, noise must be minimized. Random noise can be reduced by the square root of the amount of data averaged, but with the very long measurements times required for MT, additional averaging of data is very expensive. Normally, a single crew can measure at two sites per day for an average cost of about \$550 per site. Random noise in the data could be reduced by half if measurement time were quadrupled. While costs would probably not rise by the same factor, they could easily double. If a comparable reduction in noise could be achieved by improving the transducers and amplifiers (possible only if they are establishing the noise level), the equivalent cost savings is very substantial over the life of the equipment. Therefore optimum noise performance is the foremost design goal for the measurement system.

The very high cost associated with each MT site makes the selection of sites very important in the economic viability of the technique. Typically MT exploration crews have recorded the data and returned it to a computing facility for processing. This deprived the field crew of any feedback until the survey was completed. Location of the measurement sites (and site separation) has been determined from prior knowledge of the area, and there was no way to decrease spacing to resolve discontinuities in geological formation, nor was there any

way to repeat sites which produced bad data (except in exceptional cases where poor data quality was obvious without processing). Advances in processing techniques such as cascade decimation [22] and in computing devices appear to have made real time processing of MT data in the field a possibility. Because such processing could provide the feedback necessary to adjust site placement for maximum data value, real time processing became a design goal. In order to enable this system to be used in minimum cost configuration, the real time processor would be designed as a non-essential option. The alternative would be a recording system for raw data similar to more conventional MT systems. Raw data recording would provide a back-up for those systems which include the real time processor.

A costly loss of field crew time can occur with any failure in the instrumentation system; thus, system reliability is essential. Selection of inherently reliable devices and conservative designs can minimize random component failures, but conscious effort in designing the system is necessary to avoid catastrophic failures from abnormal system conditions. Examples of this type of failure are those caused by applying or removing power supply voltages in other than the prescribed sequence or the failure of a data communications bus if both ends are defined as transmitters (as by a software error). One goal in designing the new system was to avoid constraints on operator actions where possible, and to protect the hardware against operator error where particular actions are required. As an example of this design approach, no power supply sequencing is to be required (nor

expected), and no software action (intended or accidental) should be allowed to cause a hardware failure. In addition to providing maximum reliability, the system should be repairable in minimum time. The use of a minimum number of different subassemblies aids in repair and minimizes the spare parts inventory. Where possible, all subassemblies should be accessible and should be attached by electrical connectors to facilitate replacement. Device interfaces should be designed to avoid catastrophic failure propagation where possible. If these reliability and repairability goals are met, minimum time should be needed for system maintenance and repair.

The use of multiple simultaneous remote measurements introduces several additional design requirements. Accurate system timing at all sites is required because magnetic and electric field information which is combined for processing may be from physically separated locations and corresponding data samples must be simultaneous to within a prescribed interval (or corrected for offset) for processing. In systems for low frequency data only, very accurate clocks can be synchronized before data measurement is begun, and then run independently when separated. For example, if an error of one millisecond were acceptable, two worst case clocks (with an accuracy of 1 in 10^9) would provide that accuracy for 5.8 days after synchronization. However with a phase accuracy goal of 3 degrees at 1 KHz, the allowable error is only 8.3 microseconds. The clocks (as above) would reach this error in about 70 minutes. While this technique could be used, it would create extra work in synchronizing the clocks, and it would set severe

time constraints on site set-up and data recording operations. (Highest frequency data would have to be recorded at all sites immediately after set-up so that the clocks would have retained sufficient accuracy. Any delay could result in the need to resynchronize and restart.) In order to relax these constraints and to eliminate the requirement for the expensive clocks, a continuously synchronized clock system was chosen. An outgoing data link would be needed to control the remote sites, and it could reasonably be expected to provide a synchronization signal for the remote site clocks. The design of such a system is complicated by the phase shifts and delays expected in the variety of telemetry links which might logically be selected. The final design must include some technique to compensate for these delays.

If the system synchronization could meet these design goals, a field crew could move and set up measurement sites without returning to the central data collection site. Measurements could begin at any electric field site at any time that the magnetic field site is operating. (Each electric field site would have to be in operation through a full cycle of audio frequency magnetotelluric (AMT) and mid band data with the minimum amount of low frequency data sampled simultaneously, but a site could enter the cycle at any time.)

The second requirement introduced by the multi-site configuration is the use of battery power for the remote measurement systems because commercial power is rarely available at the measurement site, and because the use of portable generators could produce noise in the data frequency bands. Minimum power dissipation in the circuits is

different subassemblies aids in repair and minimizes the spare parts inventory. Where possible, all subassemblies should be accessible and should be attached by electrical connectors to facilitate replacement. Device interfaces should be designed to avoid catastrophic failure propagation where possible. If these reliability and repairability goals are met, minimum time should be needed for system maintenance and repair.

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that state. It would then require the operator to physically reset the system. Similarly, even if the system could be reset over the communications link, the detection of the error condition and the resetting procedure could require complicated software and hardware implementations. An automatic sense of error and reset also presents the real possibility that an error (such as lightning) could cause an unnecessary reset during an otherwise successful data run. Therefore the communication links and the remote clocks should include, as a part of normal operation, a continuous synchronization process. If disrupted, either the link or the clock should re-establish synchronization without operator (or control computer) action. If this design goal is met, no specific action would be required to correct a disruption, and the duration of such a disruption would be minimized. The only action necessary to begin a measurement would be to place the transducers, connect the instrumentation package to the communication link, and switch on the power.

If all these design goals can be met, the system should provide reduced cost per site, higher quality data, and a lower initial expense than earlier systems. Such a system should be economically justifiable for organizations interested in mineral and geothermal exploration.

3. SYSTEM CONFIGURATION

The selection of an optimum system organization must be based on the expected performance of the system and must conform to existing constraints. Various system configurations were evaluated by comparing each to the design goals explained in the previous chapter. The organization chosen achieves all design goals at a cost that should be near a minimum for the technologies available when the design was in progress. The system is shown schematically in Figure 3.

Communication of data between sites is necessary because of the single magnetic (B) field site and the multiple electric (E) field sites. Either the B field data would have to be transmitted to the E sites for distributed processing (at each E site), or all the data could be transmitted to a central location for processing. The former configuration offered the advantage of allowing a virtually unlimited maximum number of E sites without design changes. The outgoing B data would be identical for all sites, and the processing capability needed for each E site would be independent of the total number of such sites operating. Thus replication of the remote E field instrument package allows any level of system expansion. However, this configuration requires considerable processing power in the field; and if raw data is to be recorded, a data recorder would be required at each site. Thus the cost of each E field site would be quite high.

The configuration with the central site receiving all data and with central data processing and recording was chosen. A single outgoing link can provide control commands and clock synchronization

FIGURE 3: SYSTEM CONFIGURATION

for the remote sites. A separate incoming link from each site provides the data rate necessary to transfer the measured data and site status to the base site. The central processing configuration allows a single portable generator to supply power for the data processing and the recording while providing lighting and air-conditioning for the system operators. The central configuration also allows the operators to monitor any channel of data in real time. Central data processing also allows the use of cross spectra between E sites in calculation of the earth's impedance without additional data links. This new and very promising technique can be implemented in software with no changes to the hardware. (Depending on the degree of cross processing, a faster real time processor might be needed.)

The use of individual data link receivers and data processors for each E site (all centrally located) could maintain the advantage of virtually unlimited expansion capability. However the cost per operation is much lower for a single, more powerful system; and the single system eliminates complicated inter-processor communications systems. Therefore a single data recorder and a single real time processor will be used. Two channels of electric field data will be received from each of six remote sites, and this data will be recorded with three channels of magnetic field data, or each pair of E signals will be processed with the B signals for a real time data output for each E location.

Selection of a central data collection and processing system was followed by an evaluation of data communications options. Analog links appeared to offer greater data bandwidths while remaining in the low audio frequencies (for low cost communications links), but

degradation in transmission quality could directly effect the data. The requirement for phase stability in an analog link would likely eliminate the use of phone lines as well as most inexpensive radio links. Despite its lower data bandwidth, digital data transmission was tentatively chosen. It allows much greater flexibility in transmission techniques, and the analog-to-digital converters would be moved to the measurement location by this choice. Therefore the central data collection and processing site would be totally digital, and as such it would require much less stringent environmental (electrical noise, vibration, and temperature) control than a comparable system with analog links and central A/D conversion. The selection of digital links was subject to review if the data rate proved inadequate.

The system design goals include operation at any frequencies from 0.001 Hz to 1000 Hz. This six decades of frequency was divided into three bands for processing. The low frequency band covers 0.007 Hz to 0.125 Hz, and it is sampled every two seconds. The data is processed or recorded continuously when a site is in operation. If the real time processing option is used, the data will be analyzed in a minicomputer using the cascade decimation techniques described by Wight [22]. This technique uses successive digital filters and decimation to produce approximately equal percent bandwidth data at log distributed frequencies. Cascade desimation offers efficient use of processor memory, and it provides a convenient technique for removing data during intervals of poor data quality with minimum impact on total data quality and without the loss of large quantities of good data. A modification of

the Wight technique will allow the real time processor to produce valid data more quickly by reducing the effect of the start-up transients in the digital filters.

The mid band, 0.0469 Hz to 8 Hz, is processed with the same cascade decimation software that is used on the low frequency band. However, because of its sampling rate of 32 samples per second, adequate data can be obtained in about an hour. Worst case start up time for this band is only 2.6 minutes, and therefore it is not essential that the data be recorded or processed continuously. Table 2 shows the frequencies at which outputs appear and the number of independent samples obtained at a typical site.

The upper band which is known as the audio magnetotelluric (AMT) band covers 10 to 1000 Hz. Continuous wide-band sampling of data within this band would require a high speed A/D converter and a very wide dynamic range because of the impulsive energy in this band. It would also be complicated by the presence of cultural noise at 60 Hz and its harmonics. Within this band, an adequate number of independent samples can be obtained by sequentially processing individual signal frequencies. Since the required measurement time for each frequency above 10 Hz is relatively short, the overall time for sequential measurement within this band is acceptable. Therefore a special AMT processor was designed to sequentially record or process the energy at single frequencies. A tunable bandpass filter at the input provides dispersion of the impulses, and it reduces the energy at frequencies away from the signal frequency to minimize modulation products with the square wave mixers which follow. In-phase and quadrature mixers

TABLE 2
PERFORMANCE OF CASCADE DECIMATION

MID FREQUENCY BAND		(Assuming 1.9 hours of data)	
6th Harmonic (Hz)	8th Harmonic (Hz)	No. of Samples	Output Period
8	6	6839	1 sec
4	3	3419	2
2	1.5	1709	4
1	.75	854	8
.5	.375	853	8
.25	.1875	425	16
.125	.0938	211	32
.0625	.0469	104	64

LOW FREQUENCY BAND		(Assuming 4.9 hours of data)	
6th Harmonic (Hz)	8th Harmonic (Hz)	No. of Samples	Output Period
.125	.0938	274	1.07 min
.0625	.0469	136	2.13
.0313	.0234	67	4.27
.0156	.0117	33	8.53
.0078	.0059	32	8.53
.0039	.0029	15	17.07
.0020	.0015	6	34.13
.0010	.0007	3	68.27

followed by low pass filters provide the equivalent of a Fourier analysis at the signal frequency. These low pass filter signals are then digitized at a rate of 16 samples per second each. This allows a maximum bandwidth of 4 Hz on the low pass filters (while maintaining a sampling rate four times the highest data frequency), and it produces the same data rate as the mid band filter. (Note: AMT has two outputs per channel at 16 samples per second while the mid band has one output per channel at 32 samples per second.) The narrow band of the AMT procesor allows valid data to be taken between the harmonics of cultural power frequencies.

Allocation of data link capacity for the various signal bands proved that the audio frequency digital links would support operation as explained above. In all cases it was assumed that 16 bits could be sent for each A/D conversion. This would provide for more accurate converters (in the future) or for the current 12 bit converters with up to 16 levels of gain ranging. The low band data from an E field site requires a total of 16 bits per second (16 bits/sample X 2 components X .5 samples/second). The mid band data requires a total of 1024 bits per second (16 bits/sample X 2 components X 32 samples/second). The AMT band also requires 1024 bits per second (16 bits X 2 components of field X 2 for in-phase and quadrature X 16 samples per second). Since the mid frequency data and the AMT each require a small fraction of the site dwell time, they can share a data allocation in the link format. Additional bits in the link format can be used for redundancy or parity check characters. The requirement of about 1200 bits per second is within the capability of audio quality synchronous modems.

Initially the E field sites were planned as remote systems, and the B field site was to be integrated with the base data collection and processing site. As processor tasks were evaluated, it became apparent that the B field measurement required most functions of the E sites, but that it could not be conveniently partitioned to share the capabilities of the central data collection processor. Therefore the system was configured with all measurement sites (both E and B) designed as remote systems, and with the base site functioning as a system controller, data link receiver, and processor/recorder. The remote site instrument package was designed for three channels of incoming data to accommodate the magnetic field requirement. Each site was designed for two communication links to the base site, where each link can fully support two components of electric or magnetic field data. The instrument package will be fully utilized for the B site and will be partially populated for the E sites (which need only two input channels and one data link). The differences in the E and B instrument packages will be treated in more detail in the discussion of system hardware in Section 5.

A microprocessor was designed into each remote instrument package as a controller of the A/D converter and as a formatter for the data link. As the designs were developed in more detail, it became apparent that the remote microprocessor would be extremely valuable in performing other tasks. In the final design, it performs a number of tasks which enhance the reliability of the system and the quality of the data produced. The remote processor checks the redundancy character on the control link from the base site, it generates redundancy characters on the outgoing data link, and it transmits the low frequency data

redundantly to improve the probability of accurate transmission of this data. It provides a method of remotely controlling "manual gain settings", and provides active tuning and calibration of the AMT processors. Since this AMT calibration can be performed immediately before analysis of signals at each frequency, long term drift is eliminated, and data quality is assured. The use of a microprocessor controller with ROM provides the inherent flexibility of firmware to allow modification of function if necessary.

A processor is clearly needed at the central site with its data receivers, its operator interaction requirements, and its peripheral devices. The best partitioning of tasks was not apparent until the B field instrument package was separated from the base function. Because the real time processor was specified as a system option, its capability could not be used for system control (assuming that two systems would not be developed for the two configurations). When these functions were partitioned away from the base requirements, the remaining tasks appeared to be a coherent set with a reasonable performance requirement. The processor in control of the base site would be required to accept operator inputs through the CRT keyboard, provide system status information to the CRT, transfer data to the real time processor and/or the magnetic tape drives, control the remote site functions through the data link, and provide data to the line printer. With two exceptions, the above tasks are relatively low speed and may be deferred a reasonable time without loss of data. The two higher speed requirements are receiving of the data and the magnetic tape control. If data is assumed to arrive at 1200 bits per second on

each of eight incoming links (the requirement for six E sites and one B), a full byte arrives each 833 microseconds. If it were assumed that each link could be deferred for one byte time, the links would need to be read at no longer interval than 6.67 milliseconds.

Since magnetic tapes cannot complete an operation that quickly, a conflict arose. The use of a direct memory access controller for the tape units resolved the timing conflict, and made it possible to perform all base site functions with a microprocessor. In order to minimize development times and to maximize common use of parts, the same microprocessor will be used in the base and the remote sites.

An evaluation of microprocessors indicated that the system requirements could be met by any of the later, more popular microprocessors, but the Motorola 6800 offered several advantages to us. First, the University of Texas possesses an extensive system of development hardware and software for the 6800. Therefore development costs are minimized by choosing this system. The presence of the Motorola manufacturing facility in Austin and The University of Texas's excellent experience with Motorola assured good factory support in the event of problems. Also, Motorola offers a set of peripheral chips which promised to be very helpful in implementing the new system. (In particular the Serial Synchronous Data Adapter and the Direct Memory Access Controller are very useful.) Therefore the 6800 was tentatively selected for the system design. Testing of the MEK6800D2 Evaluation Kit verified

that the 6800 would perform as required. Since the D2 kit offered an inexpensive printed circuit board for the 6800 system, it was selected as the basis for both the base and the remote systems.

The early plans for the real time processing option included a special hardware device to perform digital filtering and cascade decimation with a Hewlett Packard 9825 desktop computer performing auto and cross power calculations and data accumulation in real time. A timing analysis showed that the HP 9825 is not capable of supporting six sites of data at the 32 Hz sampling rate needed for the mid band data. The auto and cross power calculations were shifted to the custom device. An analysis of the accuracy requirements for the real time processor indicated that either floating point or very long integer calculations would be required to maintain data quality through the accumulation of results. Storage of the results for auto and cross spectra of six sites with 32 frequencies each would require 4800 locations or 19.2K bytes if 4 byte precision is used. (Each frequency at each site has 25 real values accumulating as results of the real time process.) It became apparent that the speed, functions, and storage requirements for the real time processor fit a typical minicomputer with floating point arithmetic. The purchase of a commercial minicomputer avoided the very high development cost for a custom logic processor. Because of its excellent reputation for hardware reliability, and because of its lower price, the Hewlett Packard 21MX (Model 2109) with 32K words of memory was selected for the real time processor. It can be bootstrapped with the base site

microprocessor simulating a paper tape reader, and it can use all central site peripherals through the central control microprocessor. Since the real time processor function is heavily computational, a single 16 bit input/output card is the only option needed with the HP 2109, and therefore the minicomputer cost was minimized. Because the central control function is performed by the 6800, the real time processor could be sized exactly for the real-time processing function. No excess was needed for communications, operator actions, etc.

A mass storage device for the system is required to record raw data, to store the output of the real time processor, and to maintain the system software. Loading of the system software would occur before data recording begins, and thus it is not constrained by speed. Outputs from the real time processor could occur during data measurement, but the quantity of data produced is relatively small and infrequent. (A full dump of six sites for all 32 frequencies produces 4800 real data values plus any associated status information. Data at the 32nd frequency is updated every 68 minutes, and full data output would not likely be recorded more frequently.) Thus real time processor outputs do not present a significant recording load.

Recording of raw data in real time from six E sites and a single B site will require 975 bytes per second plus status information and parity during about 1.9 hours of mid frequency data recording. Low frequency data alone produces 15 bytes per second plus status and

parity for the entire 4.9 hours of site dwell time. The low band produces about 265K bytes which should be recorded continuously (with no gaps in the data). The mid band generates about 6.6 megabytes during the 1.9 hours of operation, but the data may have a few gaps without significantly reducing system efficiency. AMT band data would be recorded in the same format as the mid band data and at the same rate. However AMT data is recorded for very short periods with gaps occurring in the data itself as AMT processors are retuned for each frequency. Therefore the AMT requires the same burst rate as the mid band, but it has a much lower long term average rate, and the gaps between sampling times allow almost any physical arrangement of tracks, drives etc. to suffice.

Possible storage devices included hard and floppy disks and a number of tape systems. Hard disks were eliminated because of their relatively high cost, high power and large space requirements. Floppy disks are commonly used in systems of this size, but the packaging of the disks and the drives provides little protection from dusty environments. It seems that head and media wear could be excessive in the presence of airborne dust (which is common in the magnetotelluric survey environment).

Tape systems seem to offer the best reliability and cost for our application. Cassette systems are the least costly, but do not provide the data rate of 975 bytes per second (long term average) required for mid and low frequency data. DC-100A cartridge systems offer adequate speed, excellent convenience, and better protection

from contamination, but these systems provide too little storage for the low frequency data. Multiple DC-100A drives and clever use of multiple memory buffers could allow the use of these tapes, but the larger DC-300A tapes seem to be a better solution. A single track (of four) with ANSI standard format can record about 600K bytes, and the burst record rate is 6000 bytes per second. The speed allows relatively simple control software, and still provides time for rewrite of data in the event of a write parity error. The large capacity allows the entire low frequency band to be recorded on a single track, and thus no special timing constraints are imposed by the rewind time. A second drive can record mid frequency data (and/or AMT data) with an acceptable data loss occurring on rewind. Both 3-M and Data Electronics Incorporated (DEI) offered acceptable models. The 3-M Model DCS-3000 was selected on the basis of price. This unit contains dual DC-300 type drives with a data formatter and power supplies for 120 volt AC input power. The dual drive provides the simple control scheme explained above, and it provides redundancy for continued operation (although at lower efficiency) if either drive fails. The entire dual drive unit fits in seven inches of standard electronics rack.

Hardcopy requirements of the system include both character output (for software work, system status, numerical data output, etc.) and analog strip chart output (for raw data display). In many earlier systems an analog multi-channel strip chart recorder has been used for data display, and no character printer was used.

(Typically there was no processor in the field.) The weight and maintenance requirements for the analog recorders make them unattractive for field use. The addition of a separate character or line printer further complicates the size and maintenance problems.

Recently announced printers have offered dot matrix character printing with high resolution matrix graphics. A printer of this type can satisfy all hardcopy requirements with graphics producing a pseudo-strip-chart recording of analog data combined with high speed character output. Matrix printers use a number of techniques including thermal (Hewlett Packard Model 9876), electroresistive (Axiom Model EX810) and impact (Hewlett Packard Model 2631G, Okidata SL125 Graphics, and others). The Axiom EX810 is the lowest cost of the group and was one of the first available, but it requires aluminum coated paper which is relatively expensive. Because of the highly reflective surface, the paper is very difficult to read in less than ideal lighting. Both electroresistive and thermal printers are very quiet, and they are relatively small for the output width. The thermal printers offer much better readability (initially) than the electroresistive types, but the thermal paper tends to fade with time and exposure to light.

The impact matrix printers are noisy and large, but they offer the highest quality permanent output on the least expensive paper. The standard line printer paper is readily available, and it copies very well in Xerography copiers. A main disadvantage of the impact printer is its greater mechanical complexity, and thus

its greater probability of failure. Most low cost impact matrix printers use a single vertical row of seven to nine impact wires spaced to print one character height. This array is swept across the page to print a full line of characters on each pass. Because the array must be about one eighth inch high, there is insufficient room for the driving coils directly behind the impact points. Therefore the wires are either coupled with mechanical links, or they are bent to allow room for the coils. In either case, added wear can result. If the wires are curved for coil spacing, a compromise exists between hardening to prevent wear at the paper and preserving flexibility to prevent metal fatigue. Mechanical links allow straight wires, but add a wear point at the contact with the wire.

The Okidata SL125 offers an alternative to the dense vertical array. (Similar schemes are used by other printers such as the Printronix, but the Okidata is considered here because it is less costly.) The SL125 has twenty-two straight wires evenly spaced across the entire print width. In this configuration, the head assembly oscillates about 5/8 inch and each wire can print a horizontal row of that length before the paper is moved one vertical increment. The frequency of impacts is reduced by the ratio of wires (22 versus 7 to 9) and thus the perceived noise is reduced. All wires are straight because no crowding is necessary to accommodate the driving coils. Because no flexing is required, the wire can be hardened for maximum wear resistance. The simplicity of this configuration allows individual wire and coil subassemblies to be replaced by the

operator in the case of failure (at significantly less cost than the full head replacement necessary in many other designs).

The Okidata SL125 prints 125 lines per minute maximum (independent of line length). This is impressive for a medium priced printer for full lines. However the vertical array printers are typically much faster when printing very short lines. This reduced speed on short lines was judged to be acceptable since it results from a design which should give greater reliability, better repairability, and quieter operation.

A conventional CRT and keyboard terminal provides an efficient method of operator/system interaction. The CRT display offers much higher data rates than either a printer or a typewriter, it is silent, and it allows the simultaneous display of a large amount of data. Special options allow the system CRT to operate more effectively than a standard terminal. A full set of upper and lower case characters makes messages more legible and thus reduces the probability of operator errors. An addressable cursor allows the display to update individual status information at any point on the screen, and it can thus maintain a number of display items at current values (updating as required) while providing a stable easy-to-read display. A detached keyboard allows the display to be rack mounted with the keyboard moveable to suit operator preference. Removal of the keyboard allows much more compact packaging of the system than would be possible with a conventional terminal. For increased reliability, hermetic or noncontact key switching mechanisms were

specified. Several terminals met all system requirements, and final selection of the Teleray Model 3841 was based on price and a favorable experience with Teleray products at the University of Texas.

The decision to design special communications techniques for the new system resulted from the unique requirements and the goal of low total power consumption at the remote sites. The telemetry from the base to the remote instrument packages must provide a synchronization signal for all clocks and it must send control commands to the remote microprocessors. The synchronization function can be performed by a single link received by all remote packages. Similarly, because of the relatively low quantity of data and low rate requirements for the control commands, the same outgoing link can send tagged (addressed) data to all remote sites. This reduces the required number of transmitters and provides a global (all sites) message capability.

Fine synchronization may be achieved by phase locking the local oscillators at each remote site to a reference signal on the data link from the base site. The ambiguities existing among the data frames received may be resolved by sending a unique signal at a two second interval to correspond to the longest period necessary at the remote sites. This signal should be configured for minimum probability of false detection at the expense of higher probability of failure to detect. Since the remote clock will be assumed to have achieved synchronization, the unique two second pulse should be redundant; and therefore failure to detect is inconsequential. However, a false detection would reset the remote time reference, and cause a loss of

data until the next correct sync pulse was detected. Requiring several successive detections of two second sync signals would provide excellent reliability with almost zero probability of false detection, but this scheme is rather complex in hardware. As an alternative, a unique sequence of eight data frames (each consisting of one period of the 1200 Hz communications signal) was chosen as the sync signal. A single detection of this sequence is allowed to reset the time reference, and the probability of false detection of eight successive frames in required sequence is assumed to be acceptably low.

Time delays and phase shifts will exist to varying degrees in the telemetry links. Therefore the arrival of synchronization signals will vary at the remote sites. This must be compensated at each individual instrument package since a single reference is used. The use of a microprocessor controlled sixteen bit counter at each site will allow the delays to be offset by counting clock cycles as required from the received synchronization signal until the next actual time reference. (The delay will equal two seconds less the delay in the telemetry.) The required delay time may be determined by operating the instrument packages at the base location while monitoring the base clock and the remote package reference on an oscilloscope. Propagation time can be added for the known distance to the actual measurement location if the delay is significant. An unresolved ambiguity appears to exist in the case of phone line connections because the phase characteristics of audio quality phone lines are unspecified and are highly variable depending on the specific connection. Sending a return

signal by phone helps little because the ratio of delays between outgoing and incoming lines would remain unknown. An assumption of equal delays is probably not justifiable.

A specific phase will be chosen for the time reference, and it will be sent continuously (in all data frames) if no messages are being sent from the base site. This sequence will provide the maximum frequency of time references for phase locking the remote site clocks, and it will therefore maintain the most accurate synchronization. When messages are sent, the reference phase will occupy all odd numbered data frames (starting with the first frame of the reset sequence), and all even numbered frames (starting with the tenth which is the first even frame after the reset) are decoded as message bits. Binary "1" bits have the same phase as the reference and are thus indistinguishable except by position in time. Binary "0" bits are data frames with the phase shifted 90 degrees relative to the reference. Logic is used to enable the phase lock error signal only if two successive data frames have like phase. Since the reference phase occupies all odd numbered frames, only the reference can occur sequentially. Phase locking is enabled during two data frames as each "1" bit is received (once on the following reference frame). If a binary "0" is sent, the error signal is not correct, but since successive frames are unlike, the local oscillator remains in a hold state (the error signal is not enabled) for at least two frames. If a continuous stream of data "0" bits were sent, the local oscillators would drift since they would never sample the error signal. However, no reasonable

data contains all "0" bits, and the oscillators would not drift significantly during the length of a normal transmission even if it were all "0" bits. When the three byte queue within the Motorola MC6852 Synchronous Serial Data Adapter (SSDA) is emptied (all data for the message has been sent), the chip outputs a continuous "1" bit. This results in continuous transmission of the time reference signal.

Phase encoding of data can be used on the outgoing link because the remote oscillators are synchronized with a known phase for time synchronization. Byte framing at the receivers will be done by synchronization byte recognition in the SSDA (a feature of the chip). Byte recognition has a relatively high probability of error (with the resulting loss of subsequent data) because a single bit error in the link during synchronization will cause a mismatch. The savings in hardware is sufficient to justify the higher probability of bad framing on this link. Control commands are relatively low priority in time, and they may be repeated by the base site processor as necessary until properly received at the remote sites. Bad byte framing will not effect the synchronization of clocks since that function is achieved in dedicated hardware separate from the SSDA and microprocessor.

The telemetry from the remote sites to the base site presents a distinct contrast to the outgoing link. First, the data will be approximately 1200 bits per second from each site (1800 from a B-field site), and it will be continuous at that rate so no inquiries or repetitions will be possible for correction of unresolved errors in transmission. This data is of relatively much greater value than that

on the outgoing link because its loss can result in a restart transient in data analysis. Therefore it is essential that high data rates be combined with very high reliability.

The design of the incoming links is simplified by the synchronization of the base and remote clocks (with the outgoing link). A fully synchronous link can be used, and thus maximum data rates can be achieved. If proper byte framing is achieved initially and the clock's relative accuracy is sufficient, only the bits actually lost in a telemetry link disruption are unrecoverable. (The clock's relative accuracy should be several orders of magnitude better than necessary for short term loss of synchronization.) Synchronization and byte framing would be maintained, and data recovery would occur in minimum time. If initial byte framing is incorrect, an entire transmission period (two seconds) is lost (or a complex and time consuming correction procedure could be used). Because of the value of this data, incorrect byte framing must be minimized. Therefore the incoming link receivers will be hardware reset for byte framing at the two second reference period.

In order to fully utilize the advantage provided by a separate synchronization, the incoming links are designed with differential phase shift coding with 90 degree phase increments and two data bits transmitted per frame. This technique is very tolerant of fixed phase shifts in the link, and it requires no reference for the local oscillator. It provides a maximum rate of 2560 bits per second with a shift of phase at 1280 Hz and base frequency of

1920 Hz (shifted every third half cycle). This rate should be adequate to provide full data redundancy with parity. Blocking the data in time (such as .25 or .5 second blocks) and transmitting pairs of blocks with individual parity should make the link tolerant to multi-bit, but limited duration disruptions. This is the most likely type of link disruption because of the link's tolerance to wide band noise. Only lightning or other impulse noise sources are likely to contribute sufficient energy to cause any loss of the link.

As an example of the data blocking mentioned above, assume that each letter represents a block of data of .25 seconds duration with its parity included. Then transmission would appear as follows:

ABABCD CDEF EF GH GH

A single disruption of duration less than .25 seconds cannot result in loss of data regardless of its timing within the sequence. Assume another sequence:

ABCD ABCDEF GH EF GH

Note that this scheme provides protection from a single disruption of up to .5 seconds. It is similar to the first scheme with each data block doubled in length. The difference is in the greater probability of the second sequence to tolerate multiple disruptions because of the greater frequency of parity information. Clearly greater data security can be gained at the expense of reduced rates through greater redundancy and through the use of increased memory to spread the redundant data in time.

In summary, the system is configured with six (maximum) E field instrument packages and one B field instrument package designed as remote systems with Motorola 6800 controllers in each. The central base site includes a Motorola 6800 as the main system controller with a CRT (Telaray Mode 3841), a magnetic tape system (3-M Model DCS-3000), a graphics line printer (Okidata SL125), and optionally, a Hewlett Packard 2109 as a real time data processor. The base site provides system commands and remote site synchronization through a single out-bound data link using 1200 bits per second phase encoding with alternating data and time reference frames for a 600 bits per second maximum data transfer rate with tagged messages for the remote sites. Each remote instrument package returns status and its data through its dedicated single inbound data link (the B system using two inbound links for its three channels). These links transfer 2560 bits per second using four phase differential phase shift coding to achieve full data redundancy.

4. BASE SITE HARDWARE

4.1. Enclosure and Power Supplies

Specific designs of the base site hardware were largely fixed by the selection of the system organization. Since no analog data signals are present at the base site, the sensitivity to noise of electronic systems at that location is minimized. Noise performance of the power supplies is not critical; therefore relatively inexpensive supplies may be used. All supplies include overvoltage protection to prevent damage to base site electronic devices in the event of a power supply failure.

The Motorola 6800 in a MEK6800D2 Evaluation Kit was selected as the base site controller (Section 3). The Motorola MMS68104, a 16K byte dynamic random access memory board, was chosen as the main memory for the base site controller. Physical packaging of the base system requires about ten printed circuit boards in a card cage, and it requires power supplies, a clock display, switches for system reset and clock control, and mountings for system connectors. A standard 19 inch card rack was considered for the base site printed cards, but such a card cage would require a separate enclosure for the power supplies, and a custom mother board would be required for the Motorola 6800 bus to provide interconnections between the printed cards. Selection of the Motorola Model M68MMCC10 Micromodule Card Cage allows the use of up to ten boards 9.75 inches wide, and it includes the necessary mother board. Because the card cage is only

FIGURE 4 : BASE SITE CONFIGURATION

11.3 inches wide it is mounted inside a Bud Valu/Line enclosure Model HC-14108 which measures 15 by 17 by 12.25 inches. The card cage leaves enough room inside the enclosure to allow internal placement of the system power supplies which include a Power One HE5-18/OVP (5 volts at 18 amps) and two Power One HB12 with OVP (12 volts at 1.7 amps). The 5 volt supply is mounted to the bottom of the enclosure. The 12 volt supplies are mounted to the right side (near the front) leaving room on the upper right rear for a Boxer Model BS2107FL cooling fan which exhausts air from the enclosure. The Motorola card cage is mounted for horizontal board orientation and horizontal air flow. Cooling air enters the enclosure through a pattern of holes in the left side panel which distribute the air uniformly between the printed boards.

The front panel has two milled slots to allow viewing of two six digit LED displays (see Figure 7). The upper display shows day, month, and year; the lower, hour, minute, and second. Clock controls, system reset, and an output for clock synchronization are placed below the clock display. All interfaces are through connectors at the rear of the enclosure or through edge board connectors directly to the printed boards. Those cables entering the enclosure pass through a 4 by 4 inch cutout in the rear which is covered to maintain air flow through the hole pattern on the left side.

4.2 Base Microprocessor

The Motorola MEK6800D2 Evaluation Kit processor board is the main system controller. It fits directly into the card cage, but it requires a few minor modifications to function in the base site with the other boards at that location (see Figure 5). The primary modification is necessary for the operation of the MMS68104 memory board. This change requires an additional SN7474 and a SN7408 to provide coupling between the memory and the processor for proper timing of the refresh cycles of the memory. The modifications are detailed in the Motorola instruction manual for the MMS68104 memory board [13].

The use of the direct memory access controller on a separate printed board requires that the processor board's address and data bus buffers be modified. They must allow the processor to present a high impedance at the bus while the DMA process is executing. This buffer switching requires the addition of a SN7402 and the use of pin A on the Motorola bus for a signal from the DMA controller to the processor board. This signal indicates that a valid address is being issued by the DMA board, and it causes the processor board to issue VMA (valid memory address) to enable the memory board while maintaining high impedance of the processor's bus drivers [11].

The receiver and transmitter pins of the Asynchronous Communications Interface Adapter (ACIA, MC6850) are buffered with a SN7406 and are wired to a connector for interface with a 20 milli-ampere current loop on the CRT terminal.

FIGURE 5: BASE MICROPROCESSOR CONFIGURATION

A CMOS twelve bit binary counter (MC14040BCP) is connected to the main clock oscillator (614.4 KHz) to provide binary division of the clock rate. The ACIA clock input is then connected to outputs of the MC14040 with a dual-in-line switch which allows selection of baud rate at the CRT interface. (Normal system operation is at 9600 baud between the CRT and the control processor.)

The MEK6800D2 addressing places the system ROM (MCM6830AP-2) at hex address E000 - E3FF; and because of partial address decoding, the microprocessor interrupt vector locations at FFF8 - FFFF are mapped to E3F8 - E3FF. All interrupts therefore are vectored from the MCM6830AP-2. In order to allow firmware to control the system (and all interrupts), it is necessary to modify the addressing so that interrupts are vectored through EPROM programmed specifically for the MT system [11]. Since the MCM6830 pins are not compatible with the standard EPROM's, the EPROM socket at hex address C000 is modified to respond at E000. The MCM6830AP-2 is removed to avoid double responses from the E000 - E3FF address block. With these modifications, a new system can be written in EPROM (MCM68708) and inserted in the socket converted for E000 (Motorola designation U10). Interrupts will be vectored from this EPROM, and thus it can control system operation.

The final modification is the addition of a Serial Synchronous Data Adapter (SSDA, MC6852) to allow the base processor to test the communication links by acting as both transmitter and receiver.

While this modification is helpful in debugging communications, it is not necessary for normal system operation.

The addressing technique used on the MEK6800D2 processor board in the base controller requires that all addresses above hex 7FFF be reserved for the processor board. Modifications for the MMS68104 memory transfer the hex 0000 - 1FFF block to external addresses. Similarly, the processor board is modified to transfer the hex 6000 - 7FFF address from the PROM (U12) to an external address block. With these modifications, addresses hex 0000 to 7FFF are available for external use.

For a more complete description of the MEK6800D2 processor see the Motorola instruction manual [10].

4.3. Random Access Memory

The main memory for the base site controller is 16K bytes of dynamic random access memory (RAM) provided by a single Motorola MMS68104 memory board. This board has been designed by Motorola specifically for use with the MEK6800D2 Kit, and it plugs into the card cage with no modifications. Address selection allows separate placement of each of the two 8K byte memory segments on any address which is a multiple of hex 2000 [13]. In the base site controller the RAM occupies hex addresses 0000 to 3FFF.

4.4 Tape Controller and Real-Time Processor Interface

The magnetic tape controller uses a Motorola Direct Memory Access Controller (DMAC, MC6844) to implement all standard tape transfer functions which are possible with the 3M Company DCS-3000 dual tape drive system [24]. In order to maintain maximum system flexibility, all tape system functions may be accessed individually by the MC6800 in a software control mode. Therefore special tape operations may be implemented as necessary by disabling the direct memory access mode and using direct processor control and timing.

The tape controller also includes a two way 16 bit interface with handshake for the real-time data processor. Because separate lines are used for each direction, two bytes may be transferred each direction with a single handshake or interrupt cycle.

The tape controller board has address decoding to allow its use at any address which is a multiple of hex 20. In the Department of Energy system it occupies hex addresses 5C20 - 5C3F. Specific address allocations within this block are given in Table 3. A more detailed explanation of the tape controller and supporting software for file structured tape operation is available in Sanderlin [19].

4.5. ROM and Interface Board

The ROM and interface boards provide a variety of buffered input/output ports and read-only memory space in addition to that on the processor board. Each of these boards includes space for seven 2708 type 1024 byte EPROM chips. A pair of variable rate

TABLE 3

TAPE CONTROLLER & REAL-TIME INTERFACE 6800 ADDRESSES

Address

5C20 - 5C27 = DMAC

5C20 = Address register (High bits)

5C21 = Address register (Low bits)

5C22 = Byte Count (High bits)

5C23 = Byte Count (Low bits)

5C28 - 5C2B = PIA

5C28 = DRA; Flag inputs from tape drive

5C29 = DRB; Flag inputs from tape drive

5C2A = CRA; CA2 = Reset to tape drive

5C2B = CRB; CB2 = Read/Write control

5C2C - 5C2F = PIA

5C2C = DRA; Command lines to tape

5C2D = DRB; Read/Write auto control (not)

5C2E = CRA; CA2 = Execute to tape

5C2F = CRB; CB2 = Load command register

5C30 - 5C36 = DMAC

5C30 = Channel control register

5C34 = Priority control register

5C35 = Interrupt control register

5C36 = Data chain register

5C38 - 5C3B = PIA (Real Time Processor Interface)

5C38 = DRA; Data lines 0 - 7 (from 6800)

5C39 = DRB; Data lines 8 - 15 (from 6800)

5C3A = CRA

5C3B = CRB; CB2 = Device flag

5C3C - 5C3F = PIA (Real Time Processor Interface)

5C3C = DRA; Data lines 0 - 7 (to 6800)

5C3D = DRB; Data lines 8 - 15 (to 6800)

5C3E = CRA

5C3F = CRB; CB1 = Device command

TABLE 4
TAPE CONTROLLER & REAL-TIME INTERFACE BOARD
PIN ASSIGNMENTS

Real Time Processor Connector

Pin

1 - 16T = Data Outputs	
22T = Device Flag	(Input)
23T = Device Command	(Output)
24T = Ground	
1 - 16B = Data Inputs	
22B = Device Flag	(Input)
23B = Device Command	(Output)
24B = Ground	

3M Tape Drive Connector

Pin

2 - 16 = Command Input Bits 0 to 7	(Output)
18 = Load Command Register	(Output)
20 = Execute	(Output)
22 = Read/Write Control	(Output)
24 = Write Data	(Output)
26 = Write Shift Clock	(Input)
28 = Read Data	(Input)
30 = Read Shift Clock	(Input)
32 = Reset	(Output)
34 = Busy	(Input)
36 = Tape Unit Unavailable	(Input)
38 = Data Flag	(Input)
40 = Tape Motion	(Input)
42 = Tape Mark	(Input)
44 = Error	(Input)
46 = Early Warning	(Input)
48 = File Protected	(Input)
50 = Early Motion End	(Input)

NOTE: All odd pin numbers in the 3M connector are ground.

asynchronous ports provide fully isolated 20 milliampere current loop, RS232, or TTL levels. Dual-in-line switches provide independent selection of 2400 Hz to 307.2 KHz clock rates for the two Motorola ACIA (MC6850) chips. These chips may be set to divide the clock by sixteen for transfer rates from 300 to 19200 baud [12].

Two parallel ports are provided for peripheral device control. Each has two independent control outputs and two interrupt inputs. These are connected to Parallel Interface Adapters (pins CA2, CB2, CA1, and CB1 respectively). The parallel data for these ports is arranged as 16 dedicated outputs on one port, and eight inputs and eight outputs on the other. All outputs are buffered by open collector SN7407 chips, and all inputs are MLM339 quad comparators with the reference biased to about 1.4 volts.

Each ROM board includes an interface for the remote site CMOS bus. This interface allows the base processor to drive the CMOS bus inputs of remote site printed circuit boards for testing. Because the base site is powered by +12 and -12 volt supplies, and the remote sites are powered by +15 and -15 volts; the CMOS bus interface provides 12 volt up-levels to the bus unless a higher voltage is provided from the board being driven. In this case, the interface drivers derive their power from the driven board through the interface connector. (Component breakdown may occur on the interface board if the driven board supplies more than 18 volts through the connector.) In any case, all outputs are current limited with resistors to prevent damage to components in the event of short

circuits or voltage mismatch on the bus. For a more detailed description of the CMOS bus see Section 5.3.

Addressing jumpers allow placement of this board at any address which is a multiple of hex 2000. The board occupies hex addresses 0000 to 1C1F relative to its base address. In the Department of Energy system two ROM interface boards are used at base addresses 4000 and 6000 (hex). Specific address allocations for this board are given in Table 5.

4.6. Real Time Clock and Transmitter

4.6.1. Clock Function

The system time standard and base site communications transmitter share a single printed board in the base card cage. The clock display and controls are mounted to the front panel of the system electronics enclosure, but since they are related to the clock, they will be described in this section. Power supply inputs to the clock are split to allow separate and continuous powering of the crystal oscillator and the time counting circuits. A supply of 12 volts and about 20 miliamperes maintains time and date functions. The oscillator supply is regulated to +8 volts on the clock board to reduce the oscillator's sensitivity to power supply variations, and thus to relax the voltage accuracy requirements on the maintenance supply.

TABLE 5

ROM and Interface Board Address Allocations

Assume base address of 4000.

4000 - 43FF = EPROM (2708 type)
 4400 - 47FF = EPROM
 4800 - 4BFF = EPROM
 4C00 - 4FFF = EPROM
 5000 - 53FF = EPROM
 5400 - 57FF = EPROM
 5800 - 5BFF = EPROM
 5C00 - 5C03 = ACIA (Connector near edge of board)
 5C02 = Control/Status Register
 5C03 = Tx/Rx Register
 5C04 - 5C07 = ACIA (Connector away from edge of board)
 5C06 = Control/Status Register
 5C07 = Tx/Rx Register
 5C0B - 5C0B = PIA (Connector nearest serial outputs)
 5C08 = Output Register A (ORA); Inputs
 5C09 = Output Register B (ORB); Outputs
 5C0A = Control Register A (CRA)
 5C0B = Control Register B (CRB)
 5C0C - 5C0F = PIA (Connector nearest CMOS bus connector)
 5C0C = ORA; Outputs
 5C0D = ORB; Outputs
 5C0E = CRA
 5C0F = CRB
 5C10 - 5C13 = PIA (CMOS bus interface)
 5C10 = ORA; Address Outputs
 5C11 = ORB; Data In/Out
 5C12 = CRA; CA2 = Read/Write Line
 5C13 = CRB; CB2 = Strobe Line

The main system time reference is the 1.8432 MHz temperature compensated crystal oscillator on the clock board. This reference is divided in CMOS logic to provide all clock and calendar functions. The divider ratio can be modified to provide an increase or decrease in rate of approximately 0.1%, 1%, or 10%. This variation in rate provides a simple technique for synchronizing the clock with an external time reference such as WWV.

The outputs of the clock and calendar are connected to a static front panel LED display, and the clock outputs may be read by the base site 6800 so that current time is available for data labeling, etc. A latch function is provided to prevent carries during the 6800's sequential reading of current time. (Because it is limited to eight bits, the 6800 must make six reads to get full time and date.) The latch is timed so that any carry in progress will be completed before the data is latched.

The clock can be placed at any address which is a multiple of eight. In the Department of Energy system it occupies hex 5C48 - 5C4F. The real time data is read through a PIA (MC6821) occupying 5C48 - 5C4B. Latching of data is accomplished by setting CA2 low through control register A at 5C4A. Data register A at 5C48 is used to output a selection number from zero through five. This code selects a two digit (BCD) unit of time which may then be read through data register B at 5C49 as a pair of binary coded decimal numbers.

FIGURE 6 : BLOCK DIAGRAM OF BASE CLOCK

System timing may be established with interrupts provided by the clock. CA1 on the PIA has a one second period and CB1 has a two second period synchronized to even seconds on the real time display.

4.6.2. Real Time Clock Controls

Clock controls include six push buttons and two toggle switches on the electronics enclosure front panel (see Figure 7). A single BNC connector provides a 1 second signal from the clock with its downward transitions corresponding to real time seconds. All controls are disabled when the system power is off. With power on, each push button causes its register and thus the displayed time units (minutes, hours, days, months, or years) to advance, but carries are inhibited to allow full cycling of any level without disturbing higher levels. The push button for seconds differs in forcing the seconds, 0.1 seconds, and 0.01 seconds registers to zero when pressed. Time counting is halted until the button is released at which time it begins from zero seconds. The right toggle switch selects rates of two independent operations for the clock. When advancing the displays, this switch causes the rates to be 10, 2, or 1 step per second in the fast, mid, and slow positions respectively. When adjusting time by modifying clock rates, the retard or advance rates are approximately 10%, 1%, and 0.1% in the fast, mid, and slow positions. The advance/retard switch (left toggle switch) is a momentary switch with the center position providing

FIGURE 7: FRONT PANEL & CLOCK CONTROLS

nominal time rate. The upper position advances time rate and the lower position retards it.

4.6.3. Initial Clock Set

The procedure for initial clock synchronization requires a WWV receiver and a triggered oscilloscope. Tune the receiver to WWV. Press the Halt Seconds button on the clock, and release it when the minute tone begins on WWV. Trigger the scope on the falling edge of the sync signal from the clock (BNC connector on the front panel). Display the WWV audio on the scope and adjust to see the second tick. Set the horizontal rate to about 100 milliseconds per division. The second pulse should be off the screen to the left. (The tick for the next second may be visible on the right side of the screen.) The position will depend on your response time on hearing the minute tick and releasing the Halt Seconds button. Using the rate switch and the advance/retard switch adjust the clock so that the second tick begins just as the scope is triggered. Increase the scope horizontal rate as necessary for greater resolution as synchronization is approached. (Note: Advancing time rate moves the WWV time tick display to the right; retarding time rate moves it to the left.)

After aligning the second tick with the sync signal from the clock, check to insure that the clock displays zero seconds when the WWV minute tone is received. If not, repeat the sequence above or advance/retard as necessary to achieve proper synchronization of the seconds display.

Minutes, hours, days, months, and years may be set after seconds are synchronized with no effect on the second synchronization. The days display will cycle according to the month displayed. Therefore it may be necessary to set months and/or years before days if the day is greater than 28.

If maintenance power is provided, the clock and calendar should maintain correct information even though the display is off and the controls are disabled.

4.6.4. Clock Adjustment

If the clock has been running for an extended period, re-synchronization may be required. Connect the scope and WWV receiver as described under Initial Clock Set, and observe the second tick display relative to the clock's sync signal. Small errors are most easily corrected by advancing/retarding as necessary without using the Halt Seconds button.

4.6.5. Transmitter Function

The base communications transmitter provides a command link to remote sites and simultaneously acts as the system time reference. The transmitter is basically a sine wave synthesizer with inputs to shift the output phase by 90 or 180 degrees. The 1.8432 MHz system oscillator is divided by a binary counter which drives the 32 segment sine wave synthesizer at 1800 Hz. At a rate of 1200 Hz (every third half cycle of the 1800 Hz) the signal is inverted. The resulting

waveform is the signal utilized for system clock synchronization, and it corresponds to a continuous series of "1" bits sent over the data link (see Figure 8). The remote site clocks phase lock to this waveform, and thus it becomes the system time reference signal.

Logic allows an additional shift of 90 or 180 degrees to be applied to this reference signal. In all cases, the odd periods of 1200 Hz (starting at even seconds) will be the reference phase. Immediately after each even two seconds, the transmitter sends four 1200 Hz periods (referred to as data frames) with 180 degrees of phase shift alternated with the odd numbered frames which have no phase shift. This sequence of eight data frames (numbers 1,3,5, and 7 with no shift & numbers 2,4,6, and 8 with 180 degrees) is interpreted by the remote site clock as a reset pulse, and it is used to resolve the frame to frame ambiguity from system timing. The first data bit following the reset can occupy the tenth frame. If a "1", the relative phase is zero. If a "0", the relative phase is 90 degrees.

The data is sent to the sine synthesizer through a Motorola Serial Synchronous Data Adapter (SSDA, MC6852) which occupies hex addresses 5C4C (control/status registers) and 5C4E (all other registers). The SSDA transforms the 8 bit bytes from the micro-processor to a serial bit stream. When data from the processor is exhausted, or if no data is sent, the SSDA outputs a continuous stream of binary "1" bits [12]. Therefore when no message is sent the system synchronization signal is produced by the SSDA with no specific

FIGURE 8 : BASE TRANSMITTER WAVEFORM

TABLE 6

BASE CLOCK DISPLAY CONNECTOR

Top (Units Digits)	Bottom (Tens Digits)
Pin	Pin
1T = (No connection)	1B = Ground
2T = YEARS bit 3	2B = YEARS bit 7
3T = YEARS bit 2	3B = YEARS bit 6
4T = YEARS bit 1	4B = YEARS bit 5
5T = YEARS bit 0	5B = YEARS bit 4
6T = MONTHS bit 3	6B = MONTHS bit 7 (Gnd)
7T = MONTHS bit 2	7B = MONTHS bit 6 (Gnd)
8T = MONTHS bit 1	8B = MONTHS bit 5 (Gnd)
9T = MONTHS bit 0	9B = MONTHS bit 4
10T = DAYS bit 3	10B = DAYS bit 7 (Gnd)
11T = DAYS bit 2	11B = DAYS bit 6 (Gnd)
12T = DAYS bit 1	12B = DAYS bit 5
13T = DAYS bit 0	13B = DAYS bit 4
14T = HOURS bit 3	14B = HOURS bit 7 (Gnd)
15T = HOURS bit 2	15B = HOURS bit 6 (Gnd)
16T = HOURS bit 1	16B = HOURS bit 5
17T = HOURS bit 0	17B = HOURS bit 4
18T = MIN bit 3	18B = MIN bit 7 (Gnd)
19T = MIN bit 2	19B = MIN bit 6
20T = MIN bit 1	20B = MIN bit 5
21T = MIN bit 0	21B = MIN bit 4
22T = SEC bit 3	22B = SEC bit 7 (Gnd)
23T = SEC bit 2	23B = SEC bit 6
24T = SEC bit 1	24B = SEC bit 5
25T = SEC bit 0	25B = SEC bit 4

NOTE: The display board has a matching connector so that a 50 conductor ribbon cable may be used for interconnect. The display board fully decodes all digits, and it applies +5 volts to pin 1T.

TABLE 7

BASE CLOCK CONTROL CONNECTOR

Pin		Pin	
1T		1B	
2T		2B	
3T		3B	
4T		4B	
5T		5B	
6T		6B	
7T		7B	
8T		8B	
9T		9B	
10T		10B	
11T		11B	
12T		12B = Select Display 6 (Out)	
13T		13B = Select Display 7 (Out)	
14T = Halt Second (norm. Gnd)		14B = Halt Second (norm. +12)	
15T = Set Minute (norm. +12)		15B = Set Minute (norm. Gnd)	
16T = Set Hour (norm. +12)		16B = Set Hour (norm. Gnd)	
17T = Set Day (norm. +12)		17B = Set Day (norm. Gnd)	
18T = Set Month (norm. +12)		18B = Set Month (norm. Gnd)	
19T = Set Year (norm. +12)		19B = Set Year (norm. Gnd)	
20T = Slow Rate		20B = Fast Rate	
21T = Retard Clock Rate		21B = Advance Clock Rate	
22T = 1 Hz sync Signal to Panel		22B = Comm Link Analog Output	
23T = +12 volt System Supply Out		23B = +12 volt System Supply	
24T = +12 Maintenance Supply Input		24B	
25T = Ground		25B = Ground	

TABLE 8

BASE CLOCK & TRANSMITTER 6800 ADDRESSES

Address

5C48 = PIA - Data Register A (selects time unit to be read)
 Outputs: 0 = Years
 1 = Months
 2 = Days
 3 = Hours
 4 = Minutes
 5 = Seconds
 6 = Low level output to Control Pin 12B
 7 = Low level output to Control Pin 13B

5C49 = PIA - Data Register B (inputs two BCD digits of time/date)

5C4A = PIA - Control Register A
 CA1 = One second interval input
 CA2 = Latch Request
 0 = Hold for reading
 1 = Follow Time

5C4B = PIA - Control Register B
 CB1 = Two second interval input
 CB2 = (not used)

5C4C = SSDA - Control/Status Registers

5C4E = SSDA - All functions except control and status

action by the controlling 6800. The SSDA is software reset after each two second interval, and a message preceded by a synchronization byte may be sent immediately following the reset. Because the SSDA's internal sync byte mode is used on this link, timing of the first data output is not critical, and it may be deferred by higher priority processing. The only constraint is message completion which must occur prior to the next reset which would otherwise cause abnormal termination of the message. Figure 8 shows the reset sequence followed by two data bits.

4.7. Quad Receiver

The central site receives data over communications links from each remote site each using 2560 bits per second differential phase shift coding. Each receiver printed circuit board contains four independent receivers each consisting of a differential phase shift receiver with a local reference oscillator which adjusts to the incoming signal to compensate for phase shift in the link. The signal is coded as pairs of binary bits which are represented by phase shifts in multiples of 90 degrees. A data frame consists of three half cycles of 1920 Hz sine wave. The data frame rate is 1280 Hz with two bits per frame for the total data rate of 2560 bits per second.

The receiver consists of an in-phase and a quadrature square wave demodulator followed by a pair of integrators which are set to zero prior to each data frame. (See Figure 9 for a block diagram and

FIGURE 9: BLOCK DIAGRAM OF GUARD RECEIVER (1/4)

Figure 10 for timing and waveforms.) The integrator outputs are compared with analog comparators to determine current phase shift of the incoming data. Because the time reference is established by phase locking to the outgoing link, there is no frequency error between transmitter and receiver. Therefore only fixed phase shifts must be corrected by the receiver. Since the allowable shifts are multiples of 90 degrees, either the in-phase or the quadrature integrator should contain zero after the data frame (if the local reference oscillator is correctly phased). Therefore the most nearly zero component can be used as an error signal for local oscillator phase corrections. Logic determines the current phase (for a given data frame), and this phase determines whether the error signal or its negative should be used for local reference oscillator correction.

Since the system time references are phase locked by the outgoing link, no frequency error should exist. Only a fixed phase shift introduced by the link must be corrected. In order to increase tolerance to short duration noise, the phase correction response time of the local oscillator is made very long. The maximum slew rate is 2.6 degrees of the 1920 Hz sine wave per second. Therefore if a monotonic error could be produced (highly unlikely), it would take about 17 seconds to push the local oscillator from the correct phase to the error point at 45 degrees where the comparators can no longer determine the correct phase quadrant. In the worst case, initial lock for the link could take the same 17 seconds, but correct data interpretation occurs as soon as the phase noise is less than the

FIGURE 10: TIMING DIAGRAM FOR QUAD RECEIVER

difference between the local reference and the 45 degree ambiguity in decoding. (See Figure 11 for a representation of the receiver's phase decoding.)

In order to simplify the receiver, a correction of 0.75 degrees is applied every 285 milliseconds. This is either an advancement or a retardation depending on the phase errors which occurred during the previous period. The resulting jitter in the local reference is insignificant.

The data decoding cycle consists of 6 periods of 130.21 microseconds each within the 781.25 microsecond data frame. No data sampling occurs during the first two periods to allow passage of transients introduced by the phase shifting at the beginning of the frame. The first period is used to transfer the phase information and the phase error information from the previous data frame. The second period is used to zero the demodulation integrators. Data is sampled during the last four periods and is held (with the demodulators in the high impedance state) during the first period of the next data frame. (See Figure 10. Note that this figure shows a special case in which the demodulator drivers are at zero degrees phase relative to the short and transfer signals.)

The relative importance of the incoming data requires that a very reliable byte framing technique be utilized. For maximum reliability, a hardware reset is implemented (using the Data Carrier Detect input) for the Serial Synchronous Data Adapter (SSDA) [12]. The receiver board gets the 2 second reset pulse from the base clock

FIGURE 11

PHASE PLOT FOR QUAD RECEIVER

board through the 6800 bus. This must be delayed so that it enables the SSDA just prior to receipt of the first bit from the link. The remote clock delays one data frame after reset before clocking data to the sine wave synthesizer, and the receiving circuitry integrates for another data period. Therefore the data cannot be available before 1.56 milliseconds after reset. The hardware Data Carrier Detect (DCD) input is delayed by this period after reset, and therefore correct framing is insured. No particular data from the link is needed to correctly synchronize the two second long block of data, and thus short term disruptions of the link should not result in the loss of data beyond the disruption itself.

Inputs can be either capacitor coupled (with on-board capacitors) or they may be transformer coupled with bias supplied from the board. Contacts are available at the upper edge of the board for either application.

The quadruple receiver may be located at any 6800 address which is a multiple of 8. In the Department of Energy system, it occupies (hex) 5C50 - 5C57. Even addresses are the status/control registers of the SSDA chips (MC6852), and the odd addresses are the remaining registers of the SSDA chips.

4.8. EPROM Programmer

For prototype systems, modifications during field tests are an unfortunate reality. Since the new Department of Energy system is largely software/firmware controlled, the flexibility needed for field

changes can only be provided if firmware changes can be made without extensive support equipment. This requirement prompted the development of an EPROM programmer board which is compatible with the base site controller system.

The programmer is designed for 2708 and Intel 2716 type EPROM chips and is designed for ease of use and for protection of the chip being programmed. Chips are inserted only after the controlling program illuminates LEDs showing the chip type and indicating proper insertion time. Hardware delays and interlocks insure that chip power must precede programming pulses, and power must remain on until programming has ceased.

All power is derived from the base 6800 system except the programming voltage which must be supplied by an external 30 volt supply. A LED indicates an acceptable voltage input range for this supply, and software can check for this condition to prevent any attempt to program with the wrong voltage applied. On board regulators reduce the 30 volts to levels appropriate for the chips being programmed.

Programming functions are accomplished through two on-board PIA chips (MC6821). They apply chip addresses and data for programming. They also read data for verification, check status of voltage supplies, and control the LED indicators. The PIA chips occupy eight consecutive 6800 addresses, and may be located at any multiple of eight. When it is used, the programmer occupies hex addresses 5C40 - 5C47. Specific address allocations are given in Table 9.

TABLE 9

EPROM PROGRAMMER 6800 ADDRESS ALLOCATIONS

5C40 - 5C43 = PIA

5C40 = DRA; Output data to be programmed
5C41 = DRB; Input data from EPROM for verify
5C42 = CRA
CA2 = Apply 2716 program pulse (inverted)
5C43 = CRB
CB2 = Apply 2708 program pulse (inverted)

5C44 - 5C47 = PIA

5C44 = DRA; Status input/Indicator Output
A0 - A2 = High 3 address bits to EPROM
A3 = 30 volt supply in range (inverted)
A4 = "2716" LED control
A5 = "2708" LED control
A6 = "Insert EPROM" LED control
A7 = Programming voltage up (inverted)
5C45 = DRB; Low 8 address bits to EPROM
5C46 = CRA; Apply chip power (inverted)
5C47 = CRB; Apply programming voltages (inverted)

5. REMOTE SITE HARDWARE

5.1. Enclosure and Power Supplies

The remote site instrumentation packages for the system are battery powered, microprocessor controlled, dual channel (for E systems) or triple channel (for B systems) data acquisition systems with bidirectional communications, and they are fully controllable from a central base site. The packaging for the remote system was chosen to provide easy portability, environmental protection for the electronics, convenient access for repairability, and sufficient flexibility to allow changes in the overall system configuration.

The remote installation was partitioned into electronics, power, and communications sections plus transducers. The main section is the electronics package which includes the microprocessor, the A-D converter, the AMT processors, the data conditioning filters, the communications links, and most signal amplification. Because the Motorola MEK6800D2 processor was chosen as the controller, the 9.75 inch wide board width was adopted for the entire system. Unlike the base site electronics, the remote package must combine digital electronics with very low level analog data signals. Therefore a dual connector arrangement was chosen for the remote package printed boards. Each board (except the MEK6800D2) has two double sided 25 pin connectors located near the edges of the board. The digital commands are bus oriented on one connector, and analog signals are wired through the opposite connector for maximum separation.

A standard 19 inch (rack mountable) card cage for 9.75 inch cards was chosen to house the electronics. A custom mother board provides all interconnections between boards (except for two 50 conductor ribbon cables from the processor to the CMOS interface board and to the A-D converter board). Air flow may occur between the boards as the card guides are separated by about one inch. A modified Zero Brand (Halliburton Corp.) aluminum suitcase was chosen to enclose the remote package. Electrodes are wired directly to the enclosure in the E field systems. The B field system is similar except that each channel has external preamplifiers. (AMT preamplifiers are in the coil housings. Low-mid frequency preamps are in a separate enclosure about ten feet from the coil housing.)

The power source is external to the instrument package to allow maximum flexibility in application of the system. The instrument package includes series regulators to produce the +5, +15, and -15 volts required by the electronics. Therefore the external source may supply any DC voltage from 8 to 14 (for +5) and between 18 and 26 for the plus and minus 15 volt supplies. For remotely located applications, the source will likely be a set of four 12 volt lead-acid automotive batteries. When the package is to be used near a source of 120 volt power, the package may be powered with ordinary power supplies (which must be isolated from ground at the source). Total power consumption of the remote site package is low enough to allow powering the site for a full day from a single 12 volt automotive battery if an inverter supply were designed. However, until system

performance is established, we have chosen not to introduce the potential problems associated with the high frequency noise normally produced by power inverters.

A variety of communications schemes may be used between the remote package and the base site. The modems built into the electronics can drive wire lines over moderate distances with no additional amplification (although transformers should be used to isolate grounds between the base and the remote site). Any additional amplification hybrids, or radio link equipment must be mounted externally. The communications connector on the remote enclosure includes power and the communications signals so that a single connection should be adequate for any external equipment.

All controls for the remote package are either self-initiating, or they are controlled from the base site over the communications link. Therefore no controls are necessary for the remote package. (A power switch is included for convenience.) In addition to simplifying field operations, this feature insures that full system status is available at the base site. It may be recorded with the data on magnetic tape to fully document data recording conditions. Only the information on the physical arrangement of the transducers must be entered manually. (Normally this information will be relayed from the field crew to the base site by two-way radio, and it will then be entered by the base operator on the CRT terminal when the remote site is brought "on-line".)

Functionally the remote site instrumentation packages consist of two or three channels of transducers, preamplifiers, data conditioning filters, and AMT processors. Additionally each package contains a MEK6800D2 processor, a clock / communications board, a CMOS bus interface card, and an A-D converter. (See Figure 12 for the E system and Figure 13 for the B systems. "L", "M", and "A" on these figures represent low band, mid band, and AMT band data respectively.)

The site controller (MEK6800D2) and the clock / communications boards are explained in detail in the next sections. Section 5.3 describes the function of the CMOS bus and the addressing conventions for the remote package. Transducers and preamplifiers are treated in Sections 5.5, 5.6, and 5.7 for E-field, low/mid frequency B field, and AMT B field respectively. The final sections of the chapter include the data conditioning filters and the A-D converter board.

5.2. Remote Microprocessor

The remote site controller is a Motorola MEK6800D2 processor board. Several modifications are necessary for this application (see Figure 14). The JBUG system ROM is removed, and the addressing is modified to transfer EPROM socket (Motorola designation U10) from hex address C000 to E000 so that the restart pointer is within the EPROM address range. An additional line for the eleventh address bit (A10) provides addressing for 2K bytes and power supplies are connected for +5 volts only as required by the Intel 2716 type EPROM.

FIGURE 12: REMOTE SITE 'E' SIGNAL PATHS.

FIGURE 13: REMOTE SITE AMT SIGNAL PATHS

FIGURE 14: REMOTE MICROPROCESSOR CONFIGURATION

The EPROM at hex 6000 is similarly modified for a 2716 type chip, but its address remains at hex 6000 - 67FF. (See the Motorola manual for more detailed information on the processor board [10].)

The processor reset function occurs after a thirty second time-out which is driven from the CMOS bus interface card. The reset button is removed from the processor board, and the latch formed by the MC7400 (U22) is modified to provide non-latched buffering. The input is wired to the bus connector pin 18T.

The ACIA (U23, MC6850) is not used, and it may be removed to reduce power consumption. Two additional RAM chips (U18 & U19, MCM6810) are inserted to expand the user memory from 256 to 512 bytes.

Serial input and output which provide all communication between the remote site and the base controller occur through a SSDA (MC6852) which must be added in the wire-wrap area of the processor board. Addressing for this SSDA uses address lines A0 and A6 for addressing at hex 8040 and 8041. This partial decoding allows multiple location accesses of this chip, but the technique is consistent with the addressing of other input and output chips on the processor board, and it does not create a conflict with other chip addresses.

The remote processor for a B field system requires a second SSDA to increase data transfer capacity for the third channel. This chip must also be added to the wire-wrap area, and it should use address lines A0 and A7 for addressing at hex 8080 and 8081.

The SSDA (or both for B systems) should be wired to the Motorola bus connector of the processor board as follows:

pin	
19T	= Reset
18B	= Transmit Data (for 8040)
19B	= Transmit Data (for 8080)
23B	= Receive Clock
25B	= Transmit Clock
26B	= Receive Data (from 8040)

Since only one incoming link is used, the receive data from the second SSDA is not used.

In order to minimize power consumption, all control functions are performed by the CMOS bus. Therefore the Motorola bus is unused (except for the non-standard application of the pins listed above, and the power supply and ground pins), and the buffer chips are not needed. Elimination of the buffer chips produces a savings of 2.3 watts on the 5 volt supply (worst case). Removal of the MCM6830 JBUG ROM and the ACIA (MC6850) saves an additional 1.2 watts (worst case).

5.3. CMOS Bus Interface

The unique CMOS bus in the remote site allows the Motorola D2 kit to control the entire instrument package with minimum power requirement and maximum reliability. Speed is reduced significantly from that available on the Motorola 6800 bus, but performance is adequate, and the CMOS bus configuration provides an interface which can be easily driven by any of a number of processors. Thus if a suitable CMOS processor is available, it may be easily incorporated into the remote site system with a significant savings in power consumption.

The slow bus consists of 8 bits of address and 8 bits of data with a read/write line and a strobe line. It also includes two interrupt lines which may be used for system timing. A single PIA (MC6821) on the processor board drives the interface through a 50 conductor ribbon cable. The read/write line is available on the bus for decoding by system cards, and it also determines the direction of transfer through the bidirectional data interface buffer. The strobe line is used when writing data into the system cards. It provides a technique for delayed latching of data so that all address and data line transitions are completed prior to data sampling by the receiving card. Strobe is not needed on reading because the read process by the 6800 PIA can be delayed to allow settling of transitions. (Normally transients are shorter than the minimum time between issuing an address and reading the data lines with the PIA.)

The address lines, the read/write line, and the strobe line are unidirectional buffers (toward the CMOS bus) with MLM339 quad comparators referenced to 2.5 volts at the input and with 7.5K pullup resistors. Data lines are bidirectional with 3-state CMOS strobed hex inverters (MC14502BCP) and series 7.5K resistors used as the final driver in both directions. Outgoing data (to the CMOS bus) is sensed by an inverting MLM339 biased to 2.5 volts. It drives a MC14502BCP powered by 15 volts to provide full 15 volt up levels on the bus. Incoming data is sensed by a MC4049BCP hex buffer powered by +5 volts. The MC4049 may be overdriven on its inputs, and thus it provides a

level shift from 15 to 5 volts. The MC4049 drives a strobed hex inverter powered by 5 volts. The read/write line determines which set of strobed hex inverters is high impedance, and thus it determines the direction of data transfer.

Interrupt lines are provided by sensing two bus signals with MLM339 comparators biased to 2.5 volts. These comparators then drive the CA1 and CB1 inputs of the PIA for interrupt generation. Pull up resistors for driving the PIA are 7.5K ohms to +5 volts.

An additional function provided by the CMOS bus interface is system reset. The board contains a counter on the one Hertz signal from the CMOS bus. After a count of 32, it outputs a pulse to reset the M6800 remote site processor. Issuing an address of (binary) 0011111x on the CMOS bus resets the counter. Therefore in normal operation, this address should be issued periodically to prevent the system reset. On start up, and in the event of a system latch-up or a program loop; the time-out will cause the remote processor to restart and resume normal operation. This feature assures that the remote instrumentation package will not attain a non-responsive state. It also allows the package to be built with a single switch for power on/off. (No manual reset is needed.)

Address allocations for the CMOS bus cards are as follows:

- Bits A7,A6 = Board Type Selection
- A5,A4 = Channel Select
 - (00,01, and 10 for data channels)
 - (11 for system functions)
- A3-A0 = Device Selection (for on-board addressing)

Board and channel assignments are as follows (Bits A7-A4):

0011 = Clear processor reset time-out
 01xx = Data conditioning filter (except channel 11)
 0111 = A-D Converter board
 10xx = Pre-amp boards
 11xx = AMT processors boards (except channel 11)
 1111 = Clock board

The processor reset signal from the CMOS interface board is on pin 25T of the analog connector. Table 10 specifies the pins for the CMOS bus connector and lists the source of each signal. The input connector at the top of the interface board matches the "J1" connector of the MEK6800D2 processor board so that a 50 conductor ribbon cable may be used for the interconnection [10].

5.4. Remote Clock and Communications Board

The remote clock and communications board provides all timing and bidirectional communications for the remote site instrumentation package (see Figure 15). It provides signals to drive both the A-D conversion and the AMT processor. It contains a single incoming link decoder with phase lock for establishing the time reference, and it also contains dual differential phase shift encoded transmitters. (A single transmitter is populated with chips on the E field packages, and both are used for B field systems.)

The remote site time standard is derived from the command link being transmitted continuously from the base site. The incoming link decoder enables the phase lock error signal only if the current received phase matches the previous phase. The base transmitter sends

TABLE 10

CMOS BUS CONNECTOR PIN ASSIGNMENTS

Pin		Source
1-3T	- 5 volt Power Supply	Motherboard (MB)
4-5T	- Negative 15 volt Power Supply	MB
6-8T	- 15 volt Power Supply	MB
9-11T	- Ground	MB
14T	- Address Bit 0	Interface (IB)
15T	- Address Bit 1	IB
16T	- Address Bit 2	IB
17T	- Address Bit 3	IB
18T	- Address Bit 4	IB
19T	- Address Bit 5	IB
20T	- Address Bit 6	IB
21T	- Address Bit 7	IB
22T	- Channel Select 0 (not)	MB (by position)
23T	- Strobe (from PIA-CB2)	IB
24T	- Interrupt Input, CA1 (2 second)	Comm/Clock (CC)
1-3B	- 5 volt Power Supply	MB
4-5B	- Negative 15 volt Power Supply	MB
6-8B	- 15 volt Power Supply	MB
9-11B	- Ground	MB
12B	- Sine (In-Phase) Clock	CC
13B	- Cosine (Quadrature) Clock	CC
14B	- Data Bit 0	Bidirectional (B)
15B	- Data Bit 1	B
16B	- Data Bit 2	B
17B	- Data Bit 3	B
18B	- Data Bit 4	B
19B	- Data Bit 5	B
20B	- Data Bit 6	B
21B	- Data Bit 7	B
22B	- Channel Select 1 (not)	MB (by position)
23B	- Read/Write (1/0; from PIA-CA2)	IB
24B	- Interrupt Input, CB1 (1 second)	CC
25B	- Clock Signal for Sample & Holds (Double Pulse at 32 Hz)	CC

FIGURE 15: BLOCK DIAGRAM OF REMOTE CLOCK/COMM

the reference phase on all odd data frames, and therefore only the reference signal can occur as identical sequential phases. (See Figure 16 for receiver waveforms.) The error signal generated by the phase lock circuit is filtered and applied to a 1.8432 MHz voltage controlled crystal oscillator with plus or minus 0.003% maximum deviation. Phase locking forces the local oscillator into correct phase relative to the incoming link and therefore locks the frequency to the base clock frequency. When the reset sequence is received at two second intervals (see Real Time Clock and Transmitter, Section 4.6.), the remote site clock counters are reset, and the frame to frame ambiguity is resolved. Data may be present on even numbered data frames after the reset sequence. These frames are decoded and sent to the SSDA which is on the processor board. Incoming messages use the SSDA's synchronization character mode for data framing, and therefore the message need not begin immediately after the reset sequence. Reference phases on even numbered data frames are interpreted as binary "1" bits, and 90 degree phase shifts are interpreted as binary "0" bits. Failure to recognize the synchronization character will result in loss of the message, but the commands may be repeated and therefore such a loss is not catastrophic.

The decode technique is similar to that used on the quadruple receiver at the base site. In-phase and quadrature square wave demodulators are followed by integrators which are set to zero prior to arrival of each data frame. Like the quad receiver, the remote communications receiver uses analog comparisons of integrated values

FIGURE 16: REMOTE RECEIVER TIMING DIAGRAM

to determine the current phase of the received signal without thresholding. A primary difference is the coding scheme. The remote receiver section uses all odd numbered data frames to identify the reference phase for timing synchronization. Since the local oscillator at the remote site is locked to this reference phase, simple phase encoding may be used on the alternate data frames for transmission of binary data. (Since no transmitted phase reference is used on the link to the base site, the more complicated differential phase encoding is used.) The remote receiver also includes shift registers to maintain the most recent eight data frame phases for recognition of the 2 second reset sequence. The sequence is recognized only if all eight frames are correctly received. This produces a high probability of failure to detect, but a very small probability of false detection. This is acceptable because a single correct reset pulse is sufficient to synchronize the clock, and synchronization is then maintained by the phase lock. Later failures to detect the sequence are inconsequential because the data provided would be redundant. However, a false detection will cause the remote clock to synchronize on the wrong data frame with the resulting loss of all data sent to the base site before the next correctly detected reset sequence. Repeated loss of this quantity of data can make a restart necessary with a significant loss of field time. Therefore the complexity required for the very low probability of false detection is justified.

Time synchronization between sites must be adequate to maintain no more than about 10 microseconds difference. Delays in transmission and phase shifts in the audio frequency links could easily cause errors greater than this. Therefore, the remote clock includes a sixteen bit binary counter which counts 115.2 KHz until it matches a time delay register loaded through the CMOS bus. When match occurs, the local clock is set to zero for timing of A-D conversion, return communications, and phasing of the AMT processing. This feature allows the remote site to compensate for transmission delays on the link as well as transmission and decoding times for the reset sequence. When the correct delay is established (normally by comparing synchronization of co-located instrumentation packages), it is recorded with the system software for loading into the time delay register when the specific remote package goes on-line. Using this technique, the remote clock is actually reset on the even two second period following the receipt of the reset sequence. (The reset occurs two seconds after the reset sequence is recognized less the times of transmission, encoding of the sequence at the base, and decoding of the sequence by the remote receiver. Thus the remote site is actually reset at even seconds of real-time.)

The return link will be incorrectly framed until the time delay register is properly loaded. Therefore when a site is brought on-line, the base site must transmit a message instructing it to load the time delay register with the correct value. This message must be repeated until the return link is established. (Otherwise the return

link cannot be decoded, and the remote site status will remain unknown.)

Once the delay is loaded and the return link is established, loading of gains and other settings may proceed. Note that subsequent loss of communications will not require that this procedure be repeated, because transmission delays remain constant, and the remote memory would retain the data necessary to allow immediate resumption of data communication. If the time delay data is lost from the register at the remote site, a full restart would be required. (Note that if this data is lost, it is likely that gain settings, AMT frequencies, and data buffers may also have been lost since susceptibility of these values should be similar.)

The remote clock continuously outputs a pair of pulses at a 32 Hz rate for timing of the A-D conversion. The first pulse of each pair triggers the sample-and-hold modules for A-D conversion at the minimum gain setting. The processor determines the optimum gain for the data sample based on this ranging sample. Sampling for record occurs on the second pulse of the pair. The clock provides one second period and two second period waveforms for processor interrupts to resolve timing ambiguities in interrupts which occur at higher rates, and to identify the times at which the low frequency channels must be sampled. (AMT or mid frequency data is sampled every pair of pulses for a 32 Hz rate, but low frequency bands are sampled only at even two second intervals.) The two second waveform also signals the processor to reset the SSDA and begin a new period of data transmission to the base site.

The frequency analyzed by the AMT processor is determined by the clock board. A sixteen bit divide-by-N binary counter divides the crystal oscillator frequency and generates in-phase (sine) and quadrature (cosine) timing signals for the AMT processors. The effective rate is 230.4 KHz divided by 1 to 65, 536. The divisor is set into a sixteen bit register through the CMOS bus, and it provides a resolution of 0.0004 Hz at 10 Hz, and a resolution of 4.3 Hz at 1 KHz.

In order to verify the AMT frequencies and the phasing of the processors, an additional sixteen bit register is automatically loaded from the divide-by-N counter on even two second periods. This verification register may be read by the processor from the CMOS bus. The data is transmitted back to the base site for comparison of all sites. If the numbers are not identical, a phasing error has occurred, and the counters should be reset for a restart of the specific frequency being processed.

An AMT measurement is initiated by sending a message to all sites to load the divisor registers and to reset the AMT divide-by-N counters. The exact time of receipt of this message is unimportant so long as all sites receive the message within the same two second period. The resets are latched upon receipt at the clock board, and they are simultaneously removed when the local resets occur on the even two second intervals. At this time AMT processing begins with identical phases at all sites, and it may be checked each two seconds by comparing the contents of the verification registers.

Return data is transferred through a 2560 bits per second differential phase encoded link to the base site. The data framing is hardware controlled to insure that correct framing will occur even if the initial data in a period is lost. (In the synchronize character mode, loss of the sync character results in loss of the entire message.) After the SSDA (or both if two are used) is reset on the two second interval, it must be initialized for the proper operating mode, and data must be loaded immediately to insure that no fill characters are inserted in the data stream by the SSDA. The transmitter sections establish the phase of the outgoing signal and retain the previous phase information. Therefore the SSDA supplies binary data directly, and the transmit sections transform the data into a 32 segment synthesized sine wave with the proper phase. Dual transmitter circuits share the sine-distributed voltage divider for cost and board area savings. All other sections of the two transmitters are independent. For cost savings, the analog sections of both receiver decoders and the transmitters are biased at +7.5 volts so that lower cost single supply analog switches can be used. The loss of dynamic range is of little consequence in this application.

CMOS bus addressing for the remote clock and communications board is given in Table 11, and connector pin assignments are in Table 12.

TABLE 11

REMOTE CLOCK & COMMUNICATIONS BOARD CMOS BUS ADDRESSES

BINARY ADDRESS WORD: 1111YYYY
where YYYY = device selected

Device Code

0000 = AMT Frequency Select (8 low bits)
0001 = AMT Frequency Select (8 high bits)
0010 = Delay Time Offset (8 low bits)
0011 = Delay Time Offset (8 high bits)
0100 = Verification Register (Read only) (8 low bits)
0101 = Verification Register (Read only) (8 high bits)
0110 = Reset AMT Divide-by-N Counters (Read address)

TABLE 12

REMOTE CLOCK & COMMUNICATIONS BOARD PIN ASSIGNMENTS

Pin

1B = Transmitter No. 1 Analog Output
2B = Receiver Analog Input
3B = Transmitter No. 2 Analog Output
9B = Transmitter No. 2 Digital Input from SSDA
10B = Transmitter No. 1 Digital Input from SSDA
15B = Reset Output (2 second period)
16B = Receiver Digital Data Output to SSDA
17B = Transmitter Clock Output to SSDA
18B = Receiver Clock Output to SSDA

5.5. E Field Amplifiers

The electric field measurement is a differential voltage measurement between two earth contacts. The transducer is typically a lead plate or a metal rod conductor buffered from the soil with a saturated solution of salt of the same metal. While these are the best electrodes found to date, they are far from ideal. (See Practical Aspects, Section 1.1.)

The design of an E field preamplifier is complicated by the non-ideal transducer properties and by the characteristics of the E field signals. The amplifier must have a differential input (for flexibility of electrode placement), very high input impedance (to make electrode impedance changes negligible), very low noise (because of the low energy levels between 0.1 Hz and 2 Hz), and excellent dynamic range (to prevent saturation from the lightning strike impulses). Chopper carrier and chopper stabilized amplifiers can provide excellent noise performance by utilizing the frequencies at which the active gain devices are the quietest. However both of these types have a problem of aliasing higher frequencies at their inputs. Normally this is avoided by filtering the input data, but because of the varying source impedance from the electrodes, any input filter would need an input impedance very much higher than the maximum expected electrode impedance to assure that the frequency response of the filter would be independent of the electrode resistance. The Johnson noise from such a high resistance at the E-field preamplifier input would significantly degrade the system noise level. It would

generate additional noise as amplifier bias current varied. These noise sources or the aliasing of higher frequencies degrades chopper amplifier performance below that of linear amplifiers despite the inherently poorer noise performance of the linear electronic components at the lower signal frequencies.

The best performance currently available is achieved with a linear amplifier covering the entire MT frequency range. A dual junction FET transistor (2N5564) driving NE5534 operational amplifiers presents an extremely high input impedance, and it has excellent high frequency (above 1 Hz) noise performance. This input stage may be directly connected to the electrodes, or it may be AC coupled. Precision Monolithics Incorporated OP-10EY operational amplifiers in a differential input configuration achieve slightly better low frequency noise performance, but they have a larger bias current which may create noise when combined with varying impedances of the electrodes.

In order to allow testing of both amplifier configurations with actual electrodes in field tests, the printed circuit boards are designed for both types of input stages, and jumper wires provide selection of either input stage and either AC or direct coupling to the electrodes. Both input stages are designed for differential inputs with a gain of 40. Output of this stage is passed through a dual notch filter (60 Hz and 180 Hz) to remove the first and third harmonic of cultural power frequencies. The output is buffered and it passes to the AMT processor board (see Section 5.7). The low and mid frequency

FIGURE 17: E-FIELD PREAMP CIRCUIT

data may be taken directly from the input stage, or it may be passed through the notch filters before entering the data conditioning filters.

Table 13 lists the connector pin assignments for the analog connector of the E field preamp. The digital connector conforms to the bus convention defined in the CMOS Interface Section.

The E field preamplifier is partially populated and the input is wired directly to the 60 Hz and 180 Hz notch filters for use in the AMT B-field systems where the preamplifier is mounted inside the coil housing. Connector pin assignments remain unchanged from the E field application of this board.

5.6. B Field Low & Mid Frequency Transducers & Amplifiers

Low level magnetic field measurements in our frequency range are generally made with either induction coils or cryogenic magnetometers. While the cryogenic systems offer far better inherent noise performance, they present several practical problems. The electrical interfacing is difficult over the required dynamic range because the Josephson junction has a multivalued response to flux changes. When the magnetometer electronics slew rate limit (not an infrequent occurrence with present units), an ambiguity results which may contribute significant energy at signal frequencies. The necessity of maintaining and handling liquid helium further complicates use of cryogenics in extended field surveys. Therefore the induction coil magnetometers will be used as they have been in the

TABLE 13

E FIELD AMPLIFIER CONNECTOR PIN ASSIGNMENTS

Pin

1T- 3T = Negative Input Guard Potential
 4T- 6T = Chassis Ground
 7T- 9T = Positive Input Guard Potential
 14T- 16T = Low & Mid Frequency Ground
 18T- 20T = AMT Frequency Ground
 22T- 23T = Negative Power Supply (-18 to -26 unregulated)
 24T- 25T = Positive Power Supply (+18 to +26 unregulated)

1B = Negative Input Guard Potential
 2B = Negative Input
 3B = Negative Input Guard Potential
 4B- 6B = Chassis Ground
 7B = Positive Input Guard Potential
 8B = Positive Input
 9B = Positive Input Guard Potential
 11B = Preamplifier DC Output
 14B = Low & Mid Frequency Ground
 15B = Low & Mid Frequency Output
 16B = Low & Mid Frequency Ground
 18B = AMT Frequency Ground
 19B = AMT Frequency Output
 20B = AMT Frequency Ground

past. Since it is likely that practical cryogenic magnetometers will become available, the system has been configured to simplify conversion to alternate transducers.

The present B field system utilizes two sets of three induction coils each to measure orthogonal components of magnetic field in two frequency bands (low/mid band and the AMT band). The low and mid frequency band transducer is a coil of 30,000 turns of #22 wire on a mu-metal core six feet long with a cross section of about 1.35 square inches. The internal resistance is about 360 ohms, and the inductance is about 650 henries. At the upper frequency of 10 Hz, the coils output impedance is about 41K ohms. Therefore a preamplifier is needed to drive the cable to the instrument package and to minimize capacitive loading on the coil.

The very low signal levels from the induction coils make choppers essential to provide adequate noise performance. The 360 ohm DC source impedance and the high frequency cut off of the coil make it a good source for a solid state chopper amplifier although its inductance produces very high source impedances at the higher MT frequencies. Preamplifiers must have very high input impedances to avoid loading the coil at higher frequencies, but the low DC impedance of the coil effectively shunts the MOSFET chopper's very small charge-pumped current. Aliasing of higher frequency input signals by the choppers is reduced by the coil's upper frequency cut-off. Initially a full bridge input stage was tested, but this configuration forced the transducer coil to be electrically reversed

(the ends were alternately grounded) at the chopping frequency. Stray capacitance to the coil became a charge pump, and it resulted in a significant load on the coil at higher signal frequencies. Changes in stray capacitance could thus result in variations in system response versus frequency. As an alternative, a differential input configuration was chosen.

The linear devices of the differential input stage will theoretically produce 3 db greater noise than the devices in a single input stage, but this configuration allows the coils to be operated with one side grounded. Stray capacitance (in any reasonable quantity) will have little effect on the coils' response, and thus variations in this capacitance which may result from temperature and mechanical changes will have no significant effect on the system response.

The differential amplifier consists of a triple op-amp input configuration with a gain of 40 feeding a string of single-ended stages with a total gain of 250. The final stage is a "time-slice" demodulator (output chopper) with a 25% shunt time. This produces a total amplifier gain of 7500. The two inputs consist of Teledyne 2N6550 extremely low noise junction FETs behind series/shunt choppers of RCA 3N138 MOSFETs. The 2N6550s are run at maximum small signal gain and about 5 milliamperes quiescent current for best noise performance. Feedback from following integrated circuit operational amplifiers stabilizes the quiescent points of the 2N6550s. The gain stages are maintained at highest stable bandwidth to allow the switching spikes from the input choppers to propagate with minimum

delay. The spikes can then be "time-sliced" out of the output signal by shunting the output chopper to ground during the input switching time. The switching spikes cause saturations of the operational amplifiers after the first gain stages. Since this portion of the waveform is "time-sliced", the saturation produces no error directly. (The amplifiers recover quickly and have no latch-up characteristics.) However a saturation can cause non-linearities in feedback networks which deposit net charge on coupling capacitors at the AC breaks in the amplifier chain. The recovery of the coupling capacitor is relatively slow, and the effect persists after the "time-slice". To prevent this problem, each coupling capacitor is followed by a voltage divider driving a voltage follower. This configuration assures that the driven stage cannot be saturated, and the required slew-rate for that stage is reduced by the voltage divider ratio. This assures that no net charge can be deposited on the coupling capacitors as a result of slew rate limiting or saturations. Any needed gain is achieved in following stages which contain no frequency dependent components.

In order to produce maximum stability of chopping rate (the rate of change of chop rate affects gain), a crystal oscillator at 1519616 Hz drives CMOS logic at each amplifier. The logic produces drive signals for the four input chopping 3N138s and the three output 3N138s. The input choppers have a finite time during which both are "off" between the alternate "on" states. This assures that the choppers cannot short the input and thus load the coil. The chopping rate is 371 Hz which is a compromise between increasing noise levels

*Adjust for -1 Gain

Note: All Capacitor values in microfarads

FIGURE 18: B-FIELD PREAMP CIRCUIT

of the active gain elements with decreasing frequency and the decreasing contributions of switching transients with lower frequencies. (Jumper wires allow changing the chopper frequency by factors of .5 or 2 to optimize performance for particular frequency ranges.)

In order to minimize capacitive loading on the coil, the amplifier is located nearby. However, since the chopper needs high level drive and fast transitions, the amplifier is not placed inside the coil housing where feedback could be a problem. Instead it is placed in a separate aluminum cylinder (4.5 inches in diameter by 21 inches long) about ten feet from the coil. The cable from the coil to the amplifier is fixed on both ends to avoid chemical contamination of contact surfaces and thermocouple effects between mating connector contacts. Connectors are used after the amplifier to facilitate disassembly and moving of the system. The output of the low and mid band amplifier is fed directly into the B field data conditioning filter at the instrument package.

5.7. AMT B Field Transducer and Preamplifier

The AMT transducer is a coil of 22,304 turns of #28 wire in four sections around a 30 inch long, two inch square cross section ferrite core. The winding layers are spaced with transformer paper, and the Faraday shield on the coil is spaced 0.75 inch above the top winding to minimize capacitance and thus raise the resonant frequency. Because of the much higher minimum data frequency (10 Hz) in this band, the AMT system can use a low noise linear preamplifier.

INPUT CHOPPER
& CONDITIONING

OUTPUT CHOPPER
& CONDITIONING

FIGURE 20: B-FIELD PREAMP CHOPPER CIRCUITS

OUTPUT CHOPPER & CONDITIONING

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The amplifier uses a single ended low noise discrete JFET (Teledyne, 2N6550) followed by integrated operational amplifiers. The preamplifier includes voltage regulators (MC7815 & MC7915) to reduce power supply noise. The circuit diagram of the preamplifier is shown in Figure 21.

To minimize capacitive loading and to simplify handling, the amplifier is mounted inside an end cap of the AMT coil's PVC enclosure. The amplified signal is then connected to the instrument package through a shielded pair. Like the low/mid frequency preamp, the AMT preamp is fixed gain, and therefore it requires no control signals from the instrument package.

5.8. Data Conditioning Filters

Analog filters are used to shape the expected spectral density of data prior to A/D conversion to produce the preferred distribution of signal energy versus frequency. The preferred shape is determined by the particular application because the shape determines the ratio of A/D converter noise to signal strength at each frequency. The most frequently used filter "prewhitens" data to produce a flat expected spectral density. The flat spectrum yields a constant ratio of A-D conversion noise to signal energy at all frequencies. For most common applications which use constant bandwidth frequency analysis, and with equal emphasis on all data points; this produces the best noise performance.

FIGURE 21: AMT B-FIELD PREAMP CIRCUIT

In magnetotellurics, data analysis is based on samples derived from constant percentage bandwidth rather than constant bandwidth. Therefore a lower frequency sample represents much less energy than a higher frequency sample with the same level. By shifting the expected energy distribution slightly toward the lower frequencies, it is possible to greatly increase the levels of lower frequency samples with a relatively small decrease in the higher frequency samples. Since all points have equal value in the magnetotelluric analysis, this modified data conditioning produces a net improvement in overall data quality.

The data conditioning filters are designed to utilize this trade-off by producing a combination of flat spectral density from the highest frequencies to mid band and with spectral density increasing from mid band to the lowest frequencies. The actual implementation of the filter produces a smooth transition between the declining portion of the spectrum and the flat portion. (See Figures 22 and 23 for circuit diagrams.)

Both E field and B field data conditioning filters are designed to produce dual outputs. Each output produces the combination spectral density described above, and each output has its upper frequency cut-off designed to act as an alias filter for the appropriate sampling rate. The low frequency outputs are analyzed up to 0.125 Hz and are sampled at a two second interval. The mid frequency outputs (the highest frequencies output from these filters) are analyzed to 8 Hz and are sampled at 32 Hz. Sampling at four times the Nyquist

NOTE: All capacitor values are in microfarads.

FIGURE 22: CIRCUIT DIAGRAM OF E FIELD DATA CONDITIONING FILTER

FIGURE 23: CIRCUIT DIAGRAM OF B FIELD DATA CONDITIONING FILTER

frequency provides greater protection against aliasing than lower sampling rates, and it therefore allows less radical alias filter designs.

The E field spectral density (for a homogeneous earth with a resistivity of one ohm-meter) is reproduced in Figure 24. The response of the E field filter is shown in Figure 25, and the resulting expected spectral density is shown in Figure 26. The use of the piecewise linear approximation of E field spectral density produces the sharp changes at several points on the expected spectral density of Figure 26.

A piecewise linear approximation of average B field spectral density is shown in Figure 27. The B field filter response and the resultant spectral density are shown in Figures 28 and 29.

In order to prevent undetected saturations in the data conditioning filters, all stages have unity gain or greater at all frequencies. This design characteristic greatly decreases the probability of an earlier stage saturating while the output remains unsaturated. It also minimizes the effect of noise contributions from stages within the filter. Use of the minimum gain constraint in designing the data conditioning filters makes the use of latching saturation detectors (such as are used in the AMT processor) unnecessary.

Each output of the data conditioning filters has a variable gain stage which may be set from 2 to 4096 by factors of 2 through the CMOS bus. (See Table 14 for address assignments.) This stage

FIGURE 24: E FIELD POWER SPECTRAL DENSITY

FIGURE 25: AMPLITUDE RESPONSE OF E FIELD DATA CONDITIONING FILTER

FIGURE 26: POWER SPECTRAL DENSITY OF CONDITIONED E FIELD DATA

FIGURE 27: B FIELD POWER SPECTRAL DENSITY

FIGURE 28: AMPLITUDE RESPONSE OF B FIELD CONDITIONING FILTER

FIGURE 29: POWER SPECTRAL DENSITY OF CONDITIONED B FIELD DATA

TABLE 14

DATA CONDITIONING FILTER CMOS BUS ADDRESS

BINARY ADDRESS WORD: 01XXYYYY

where XX = Channel Selected

YYYY = Device Selected

Device

0000 = Mid Frequency Gain Select (Low 6 bits)

0001 = Mid Frequency Gain Select (High 6 bits)

0010 = Low Frequency Gain Select (Low 6 bits)

0011 = Low Frequency Gain Select (High 6 bits)

NOTE: Gains are adjustable from 2 to 4096 by factors of 2.

A single bit of the 12 gain set bits should be a "1".

A gain of 2 = 100000000000 (binary)

A gain of 4096 = 000000000001 (binary)

TABLE 15

DATA CONDITIONING FILTERS CONNECTOR PIN ASSIGNMENTS

ANALOG CONNECTOR

Pin

4T	= Mid Frequency Analog Output
13T	= Low Frequency Analog Output
22T,23T	= Negative 18 to 26 volts Unregulated
24T,25T	= Positive 18 to 26 volts Unregulated
15B	= Analog Input

will normally be set at a gain, and will remain at that setting for the duration of the complete data run. (Limiting the gain of this stage to 64 will insure that adequate feedback exists to maintain gain stability of the stage.) Short term gain changes are made by the variable gain stage on the A-D converter card in the gain ranging process. (Note however that the variable gain stage on the conditioning filter is past all frequency dependent stages, and therefore changing its gain during data sampling will not degrade the data if the change in gain is recorded.)

Analog outputs from the data conditioning filters go to the A-D converter card. If a saturation is present at the filter output, it will be detected by the A-D converter when the signal is sampled. Therefore no special saturation detectors are needed after the variable gain stages.

5.9. AMT Processor

The AMT processor determines the energy in in-phase and quadrature components of data signals at individual center frequencies between 10 and 1000 Hz. The first stage of the AMT processor is an electronically tunable bandpass filter. (See Figure 30 for a block diagram.) This filter reduces the energy at frequencies away from the measurement frequency to decrease modulation products with higher harmonics of the square wave modulators which follow. Its narrow pass band spreads the impulse energy of local lightning strikes, and this greatly reduces the dynamic range needed to prevent saturations in

FIGURE 30: AMT PROCESSOR BLOCK DIAGRAM

the presence of local thunderstorms. Therefore it allows utilizing greater system gains for improved noise performance.

The bandpass filter uses variable gain stages (designated K1 and K3 in Figure 31) to adjust effective capacitance and resistance in the tunable stages. Dual RC pairs and analog switches (not shown in Figure 31) provide two bands with each covering one decade of frequency. In order to maintain a constant Q at the desired value of 10 over the frequency range, the gains of the tuning stages must be varied reciprocally as the center frequency is changed. The remote site's Motorola 6800 calculates the nominal gains for each center frequency and sets them through the CMOS bus. Individual adjustments of gain on the two tuning stages allow fine adjustment of Q and the center frequency during calibration of the filter. The nominal Q of 10 response of the filter is shown in Figure 32 for minimum and maximum frequencies tuned by the lower band.

The response of the filter is:

$$\frac{E_o}{E_i} = \frac{\frac{K_4 R_4 S}{C_1' (R_1 R_4 + R_3 R_4 + R_1 R_3)}}{S^2 + \left[\frac{1}{R_2' C_2} + \frac{1 - K_4 \left[\frac{R_3}{R_3 + R_4} \right]}{C_1' \left[R_1 + \frac{R_3 R_4}{R_3 + R_4} \right]} \right] S + \frac{1}{R_3' C_1' C_2 \left[R_1 + \frac{R_3 R_4}{R_3 + R_4} \right]}}$$

$$C_1 = C_2 = 1 \text{ mfd}$$

$$R_1 = 10 \text{ K}$$

$$R_2 = 1.25 \text{ K}$$

$$R_3 = R_4 = 20 \text{ K}$$

$$K_1 = \text{Variable to set } C'_1$$

$$K_2 = 1$$

$$K_3 = \text{Variable to set } R'_2$$

$$K_4 = 3.8$$

$$\text{Gain} = 19$$

$$Q = 10$$

$$C'_1 = C_1(1 - K_1)$$

$$R'_2 = R_2/(1 - K_3)$$

	Freq	K_1	C'_1	K_3	R'_2
Low Range	7.95	0.0000	1.000	.9375	20 K
	127	.9375	.0625	0.0000	1.25 K
High Range	79.5	0.0000	.1	.9375	20 K
	1270	.9375	.00625	0.0000	1.25 K

FIGURE 31: TUNABLE BANDPASS FILTER CIRCUIT

NOTE: Low Band setting is shown. High Band is similar, but one decade higher.

FIGURE 32: RESPONSE OF BANDPASS FILTER

This gives a center frequency of:

$$\omega_o = \sqrt{\frac{1}{R_2' C_1' C_2 \left[R_1 + \frac{R_3 R_4}{R_3 + R_4} \right]}}$$

and:

$$Q = \frac{\omega_o}{\frac{1}{R_2' C_2} + \frac{1 - K_4 \left[\frac{R_3}{R_3 + R_4} \right]}{C_1' \left[R_1 + \frac{R_3 R_4}{R_3 + R_4} \right]}}$$

Assuming that $K_2 = 1$, $C_1' = C_1 (1 - K_1)$, and $R_2' = \frac{R_2}{(1 - K_3)}$.

As the filter is tuned to minimum frequencies, R must be made large. The divisor, $(1 - K_3)$, is reduced as K_3 approaches one. The adjustment becomes coarse as the difference between K_3 and one declines, and tuning resolution degrades. Figure 33 shows the discrete tuning points achievable with ideal components in the filter when it is tuned to the lowest frequency in the band. (The D-A converters used in the filter, Analog Devices AD7531KN, are guaranteed accurate to only 9 bits while 12 bits of resolution and ideal accuracy are shown in the figures. Therefore the real filter would not produce such a uniformly structured tuning plot.) Figure 34 shows tuning at

FIGURE 33: TUNING RESOLUTION OF BANDPASS FILTER (LOW END)

FIGURE 34: TUNING RESOLUTION OF BANDPASS FILTER (MID BAND)

FIGURE 35 : TUNING RESOLUTION OF BANDPASS FILTER (HIGH END)

mid band where resolution of C'_1 and R'_2 adjustments are about equal, and Figure 35 shows tuning at the highest frequency where capacitance changes have become coarse.

The accuracy of magnetotelluric inversions is approximately 18 times more sensitive to percentage of frequency error than to percentage of Q error. Therefore Figures 33, 34, and 35 are plotted so that errors in impedance from the inversion process are uniform for a given distance on the plot. (i.e., Plots of constant impedance error would be circular about the desired point.) Therefore the optimum achievable tuning point may be determined by selecting the point on the plot which is nearest the desired point.

In tuning the filter, the optimum point may be approached by a feedback scheme to within 9 bits of DAC accuracy. Final tuning must be done by trial of a number of points in the vicinity of the desired point because the accuracy of the D-A converters does not guarantee a monotonic or logical approach path to the best point.

Following the band pass filter is a variable gain stage which provides additional gain of the filtered signals. The gain may be set from 2 to 256 by factors of 2 under control of the CMOS bus.

The signal is then mixed with in-phase and quadrature square waves driven by a variable period generator in the remote site clock. This clock provides integer division of 230.4 KHz for a resolution of .0004 Hz at 10 Hz and 4.3 Hz at 1000 Hz. Following the mixer, the signal is passed through a variable bandwidth low-pass filter which allows selection of bandwidths from 0.4 Hz to 4 Hz and a DC gain of

10. (See Figure 36) The outputs of these filters are digitized and transmitted to the base site for processing.

Either the band pass filter or the low pass filter could mask saturations occurring earlier in the electronics. In order to assure that they are detected, comparators and latches sense saturations at the inputs of the bandpass filter and the mixers. These detectors are read and reset by the CMOS bus as each digitizing cycle occurs.

In order to maintain best possible data quality, a self calibration system is included on the AMT boards. A 2.5 volt reference circuit and analog gating provides a known level in-phase or quadrature signal or a zero at the input of the AMT processor. Using the CMOS bus, the microprocessor can tune the bandpass filter for precise phase and gain at the injected frequency. The digitizer's zero offset can be checked, and any offset can be digitally corrected as the data is transferred through the microprocessor.

The calibration procedure can be performed immediately before measurements are made at each frequency. The calibrate signal is then turned off and the signal is passed to the AMT processor. The calibrate feature not only provides maximum data quality, but it also eliminates the need for careful tuning and trimming of the precise filtering circuits. Thus it will greatly reduce the cost of producing and maintaining the AMT processor boards.

FIGURE 36: RESPONSE OF LOW PASS FILTER

TABLE 16

CMOS BUS ADDRESSES FOR THE AMT PROCESSOR

BINARY ADDRESS WORD: 11XXYYYY
 where XX = channel selected
 YYYY = device selected

Device	
0000	Band Pass Filter, Resistor Adjust (8 low bits)
0001	Band Pass Filter, Resistor Adjust (4 high bits)
0010	Band Pass Filter, Capacitor Adjust (8 low bits)
0011	Band Pass Filter, Capacitor Adjust (4 high bits)
0100	Saturation Detectors (for reading)
	Data Bit 0 = Input detector
	Data Bit 1 = Variable Gain Detector
0101	Low Pass Filter, Capacitor Adjust (8 low bits)
0110	Low Pass Filter, Capacitor Adjust (4 high bits)
0111	Variable Gain Adjust (Data word should have one "1")
1000-1100	Reset Saturation Detectors
1100-1111	Calibrator
	Data Bit 0 = Calibrate/Data Input (1/0)
	Data Bit 1 = Sine Calibrate Enable
	Data Bit 2 = Cosine Calibrate Enable
	Data Bit 3 = High/Low Band Select (1/0)

TABLE 17

AMT PROCESSOR ANALOG PIN ASSIGNMENTS

Pin	
8T	- Analog Output (In-Phase)
9T	- Analog Output (Quadrature)
10T	- Ground
11T	- Signal Input
12T	- Ground
19-21T	- Negative 15 Power Supply
10-12B	- Ground
19-21B	- Negative 15 Power Supply

5.10. A/D Converter Board

The final analog element in the data path is the A-D converter. Selection of the appropriate converter establishes the last noise added to the signal before processing. If the signal input is assumed to be random and normally distributed, an inexpensive 8 bit A-D converter can give better than 40 db signal to digitizing noise ratio if the signal variance (power) is precisely known. However, in our case the ratio of likely signal variances is almost 100 to 1 for B field (and wider for E field). In order to accommodate this range of variances with a fixed gain system, a 15 bit converter would be needed for 40 db of signal to digitizer noise ratio over the entire range. Because of the rapidly rising cost of each bit after about 12, a detailed analysis of converter noise contributions is justified.

A common alternative to a high resolution converter is a lower cost converter following a gain ranging amplifier. Several schemes are possible for predetermining the needed gain if time is available between the data sample times (as it is in our case). However the accuracy of the ranging amplifier is generally not as good as the resolution of the A-D converter, and thus it produces a significant degradation in data quality.

We shall assume normally distributed random signals and an A-D converter with neither offset nor linearity error.

Letting: E_{mx} = the hard limit level of the converter
 N = the number of converter bits
 m = the number of binary ranging steps
 $P(x)$ = the probability of event x

$$\text{erf}(x) = \text{the error function of } x = \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt$$

σ_s^2 = variance of the signal

$k_s = E_{\text{mx}} / \sigma_s$

e = resolution size of the converter = $\frac{E_{\text{mx}}}{2^{N-1}}$

e_s = signal value

For an A-D converter operating in the linear region, the noise power is:

$$P_{\text{NL}} = \frac{e^2}{12}$$

However, if the gain is reduced by a factor of 2 to prevent saturation, the noise voltage increases by 2 and the noise power by 4. Thus:

$$P_{\text{NL}} = \frac{e^2}{12} P(0 \leq |e_s| \leq E_{\text{mx}}) + \frac{2^2 e^2}{12} P(E_{\text{mx}} \leq |e_s| \leq 2E_{\text{mx}})$$

For additional levels of ranging, it follows that:

$$P_{\text{NL}} = \frac{e^2}{12} P(0 \leq |e_s| \leq E_{\text{mx}}) + \frac{2^2 e^2}{12} P(E_{\text{mx}} \leq |e_s| \leq 2E_{\text{mx}}) +$$

$$\frac{4^2 e^2}{12} P(2E_{\text{mx}} \leq |e_s| \leq 4E_{\text{mx}}) + \dots +$$

$$\frac{2^{2m} e^2}{12} P(2^{(m-1)} E_{\text{mx}} \leq |e_s| \leq 2^m E_{\text{mx}})$$

This reduces to:

$$P_{NL} = \frac{\epsilon^2}{12} \operatorname{erf}(k) + \sum_{i=1}^m \frac{2^{2i} \epsilon^2}{12} (\operatorname{erf}(2^i k) - \operatorname{erf}(2^{(i-1)} k))$$

A second noise contribution is the hard limit or saturation of the A-D converter. The error introduced is equal to the difference between the saturated level and the actual data value. This gives a noise power as follows:

$$P_{NS} = \int_{-\infty}^{\infty} (\Delta e)^2 f(\Delta e) d\Delta e$$

where Δe = the difference between actual data value and the saturated level

$$f(\Delta e) = \frac{1}{\sqrt{2\pi}\sigma_s} e^{-\frac{(|\Delta e| + 2^m E_{mx})^2}{2\sigma_s^2}}$$

Then:

$$P_{NS} = 2 \int_0^{\infty} (\Delta e)^2 \frac{1}{\sqrt{2\pi}\sigma_s} e^{-\frac{(|\Delta e| + 2^m E_{mx})^2}{2\sigma_s^2}} d(\Delta e)$$

Substituting: $x = \frac{\Delta e}{\sigma_s}$, $k = \frac{E_{mx}}{\sigma_s}$, $d\Delta e = \sigma_s dx$

$$P_{NS} = 2 \int_{2^m k}^{\infty} x^2 \sigma_s^2 \frac{1}{\sqrt{2\pi}} e^{-\frac{(x + 2^m k)^2}{2}} dx$$

$$= \sigma_s^2 \sqrt{\frac{2}{\pi}} \int_{2^m k}^{\infty} x^2 e^{-\frac{(x + 2^m k)^2}{2}} dx$$

Substituting again: $y = x + 2^{m_k}$, then $x = y - 2^{m_k}$, $dx = dy$

$$\begin{aligned}
 P_{NS} &= \sigma_s^2 \sqrt{\frac{2}{\pi}} \int_{2^{m_k}}^{\infty} (2^{2m_k} e^{-\frac{y^2}{2}} - 2^{(m+1)} k y + y^2) e^{-\frac{y^2}{2}} dy \\
 &= \sigma_s^2 \sqrt{\frac{2}{\pi}} \left\{ 2^{2m_k} \int_{2^{m_k}}^{\infty} e^{-\frac{y^2}{2}} dy - 2^{(m+1)} k \int_{2^{m_k}}^{\infty} y e^{-\frac{y^2}{2}} dy \right. \\
 &\quad \left. + \int_{2^{m_k}}^{\infty} y^2 e^{-\frac{y^2}{2}} dy \right\} \\
 &= \sigma_s^2 \sqrt{\frac{2}{\pi}} \left\{ 2^{2m_k} \int_{2^{m_k}}^{\infty} e^{-\frac{y^2}{2}} dy + 2^{(m+1)} k e^{-\frac{y^2}{2}} \right\}_{2^{m_k}}^{\infty} \\
 &\quad + \left[\int_{2^{m_k}}^{\infty} e^{-\frac{y^2}{2}} dy - y e^{-\frac{y^2}{2}} \right]_{2^{m_k}}^{\infty} \\
 &= \sigma_s^2 \sqrt{\frac{2}{\pi}} \left\{ (1 + 2^{2m_k}) \int_{2^{m_k}}^{\infty} e^{-\frac{y^2}{2}} dy - 2^{m_k} e^{-\frac{2^{2m_k}}{2}} \right\}
 \end{aligned}$$

However:

$$\operatorname{erf}(x) = \frac{2}{\sqrt{\pi}} \int_0^{\sqrt{2}x} e^{-\frac{u^2}{2}} \frac{du}{\sqrt{2}}$$

letting $x = \frac{y}{\sqrt{2}}$

$$\operatorname{erf}\left(\frac{y}{\sqrt{2}}\right) = \frac{\sqrt{2}}{\sqrt{\pi}} \int_0^y e^{-\frac{u^2}{2}} du$$

and this equals $P(-y \leq u \leq y)$

Substituting:

$$P_{NS} = \sigma_s^2 \left\{ (1 + 2^{2m} k^2) (1 - \operatorname{erf}(2^m k)) - \sqrt{\frac{2}{\pi}} 2^m k e^{-\frac{2^{2m} k^2}{2}} \right\}$$

The third noise contribution is the inaccuracy of the amplifiers used for gain ranging. It is assumed that the digitizer has no gain related noise when in the maximum gain condition, but when gain is reduced to prevent a converter saturation, a gain error is introduced. Note that this noise does not contribute below E_{mx} (because of no ranging) and it does not contribute above $2^m E_{mx}$ (because the saturation term provides this noise energy).

Within the range E_{mx} to $2^m E_{mx}$ we have:

$$P_{NG} = 2 \int_{E_{mx}}^{2^m E_{mx}} (a e_s)^2 f(e_s) de_s$$

where a = the gain error of the ranging amplifier

$$P_{NG} = 2a^2 \int_{E_{mx}}^{2^m E_{mx}} e_s^2 \frac{1}{\sqrt{2\pi}} e^{-\frac{e_s^2}{2\sigma_s^2}} ds$$

Change variables: $x^2 = \frac{e_s^2}{\sigma_s^2}$, $x = \frac{e_s}{\sigma_s}$, $dx = \frac{1}{\sigma_s} de$, $k = \frac{E_{mx}}{\sigma_s}$

$$\begin{aligned}
 P_{NG} &= \sqrt{\frac{2}{\pi}} a^2 \sigma_s^2 \int_k^{2^m k} x^2 e^{-\frac{x^2}{2}} dx \\
 &= a^2 \sigma_s^2 \sqrt{\frac{2}{\pi}} \left\{ -x e^{-\frac{x^2}{2}} \right\}_k^{2^m k} + \int_k^{2^m k} e^{-\frac{x^2}{2}} dx \\
 &= a^2 \sigma_s^2 \left\{ \sqrt{\frac{2}{\pi}} k e^{-\frac{k^2}{2}} (1 - 2^m e^{-\frac{(2^m - 1)k^2}{2}}) \right. \\
 &\quad \left. + \operatorname{erf}(2^m k) - \operatorname{erf}(k) \right\}
 \end{aligned}$$

Then the total signal to noise ratio is calculated:

$$\text{SNR} = \frac{P}{P_{NS} + P_{NG} + P_{NL}}$$

Evaluating this expression for 8, 10, 12, and 14 bits with 0, 1, 2, and 3 levels of gain ranging and with a gain ranging error of 1% produces Figure 37. This figure indicates the signal to digitizing noise ratio achieved by any of the converter configurations over a given ratio of variances. It also shows where the expected variance should be set for best performance. An example of random normally distributed data at representative levels is presented in Figure 38. For a 12 bit A-D converter with no gain ranging, this

FIGURE 37: NOISE CONTRIBUTION OF A-D CONVERSION

VARIANCE / LIMIT = .0044

VARIANCE / LIMIT = .1906

VARIANCE / LIMIT = .377

FIGURE 38

SMOOTHED GAUSSIAN RANDOM SIGNALS

figure shows the minimum signal level which produces about 46 db, and the maximum level for 30 db. It should be noted that the performance is assymetrical and that the center of the variance range must be set below the optimum point to achieve equal performance on both extremes of the variance range.

In the Department of Energy system, we chose an Analogic Model 6812SR analog-to-digital converter module. It provides 16 channels with a 12 bit conversion accuracy [1]. The converter board contains 9 channels of variable gain (2 to 64 by factors of 2) followed by 9 sample and hold circuits (see Figure 39). The added complexity of the multiple sample and hold circuits is required to permit simultaneous sampling of all data channels.

Three channels sample the low frequency band (0.125 Hz and lower) continuously at 0.5 Hz. Three channels are dedicated to the AMT data (from the AMT processors), and they are used only during AMT data sampling. The three remaining channels are used for either AMT or the mid-frequency band data with analog switches selecting the desired input signals. (Note: E field systems will use a total of 6 channels rather than 9 as indicated above for the B field system.)

The A-D converter board contains six additional channels (for -10 volt to +10 volt inputs) without variable gain or sample and hold circuits, and eight additional channels (for -5 volt to +5 volt inputs) which are multiplexed into a single Analogic 6812 input. These channels will be used to remotely monitor the battery or other power source voltages, the regulated supply levels, the DC output of the

FIGURE 39: BLOCK DIAGRAM OF A-D BOARD

first amplifiers, and the enclosure temperature (with a thermistor).

The remaining channels are not currently defined.

All gains are set by the slow bus under microprocessor control. Each channel will have the maximum (short-term) gain set by a command from the base site. Gain ranging will consist of 2 bits (3 additional levels) of reduced gain which can be changed at the sampling rate. A sample will be made at minimum (short-term) gain about three milliseconds before data sampling time. The results of this sample will provide the gain information to be used at data time. The second sample (at data time) will provide maximum possible unsaturated gain. The gain ranging bits will be appended to the converted value, and this data will be sent to the transmit queue.

TABLE 18

CMOS BUS ADDRESSES FOR THE A-D CONVERTER

BINARY ADDRESS WORD: 0111YYYY
 where YYYY = device selected

Device

0000-0100 = Gain select for channels 0 to 8 respectively
 (Data word should have one "1")

Data = 00000001; Maximum gain

Data = 00100000; Minimum gain

1100-1111 = Selector for AMT/Mid Frequency

Data = xxxxxx0; Mid Frequency Data

Data = xxxxxx1; AMT Data

Multiplexer selection for A-D converter channel 9

Data = xxxx000x; Select 5 volt supply check

Data = xxxx001x; Select -15 volt supply check

Data = xxxx010x; Select Multiplexer Input 2

Data = xxxx011x; Select +15 volt supply check

Data = xxxx100x; Select Multiplexer Input 4

Data = xxxx101x; Select Multiplexer Input 5

Data = xxxx110x; Select Multiplexer Input 6

Data = xxxx111x; Select Multiplexer Input 7

TABLE 19

A-D CONVERTER ANALOG PIN ASSIGNMENTS

Pin		A-D Channel
1T	- Ground	
2T	- Mid Frequency Input 0	0
3T	- AMT Input 0	0
4T	- AMT Input 1	1
5T	- Mid Frequency Input 1	1
6T	- Mid Frequency Input 2	2
7T	- AMT Input 2	2
8T	- AMT Input 3	3
9T	- AMT Input 4	4
10T	- AMT Input 5	5
11T	- Low Frequency Input 0	6
12T	- Low Frequency Input 1	7
13T	- Low Frequency Input 2	8
1B	- Ground	
9B	- Multiplexer Input 2	9
10B	- Multiplexer Input 4	9
11B	- Multiplexer Input 6	9
12B	- Multiplexer Input 7	9
13B	- Multiplexer Input 5	9

6. SOFTWARE

The flexibility designed into the Department of Energy system is largely dependent upon the capabilities of the multiple microprocessors. Therefore a large part of the total system development is software. Hardware partitioning of the system provides a convenient and similar partitioning for the software. The most basic software is for the remote site instrumentation package controller, a Motorola 6800. The second segment is the control software for the ~~base site controller, another M6800, and the third is the optional~~ real-time processor software for the Hewlett Packard 21MX (Model 2109). The software will be explained in this chapter in that order.

6.1. Remote Site Software

The Motorola 6800 at the remote site has several distinct tasks, all of which require careful timing. Primarily it must respond to interrupts from the remote clock board and perform A-D conversions for gain ranging. It must then set the variable gain stages for the sampling for record which occurs about three milliseconds later. On interrupt, it then samples for record and places the data values into a buffer array for transmission to the base site.

The remote controller must simultaneously maintain data in the outgoing SSDA buffer so that no gaps occur in the data stream. Normally it takes sequential bytes from the outgoing buffer array, but it must periodically provide check sums and redundant data as necessary

to support validity checks and error correction. When the two-second-interval interrupt occurs, the processor must reset the SSDA and load it with the first byte to be transmitted to the base site in the next data block.

As data is received from the base site, it must be placed into an input buffer array; and upon message completion, the processor must check for an error in transmission by comparing checksums. If an error exists, an indicator of this condition is placed in the status frame of the output buffer. If not, an acknowledgment is placed in the status frame, and the message is acted upon.

Messages will vary in complexity from simple commands to change gains, adjust AMT frequencies, etc. (all of which require only one or two bytes written to the CMOS bus) to more complex tasks such as to tune the AMT bandpass filters to the currently injected frequency under closed loop conditions. In addition, as an aid to system development and evaluation, the remote processor will be programmed to allow remote loading of software into the 512 bytes of random access memory (RAM). The code will then be executable on command from the base site.

All tasks must be programmed to avoid timing conflicts which would cause data to be lost through delayed processing. Since the outgoing communications link needs attention on the average of every 3.125 milliseconds, and it may be deferred a maximum of 6.25 milliseconds, no uninterruptable long term task may be allowed to occupy the processor. Although its rate is one fourth as high, the incoming

communications link presents a similar problem. Therefore loading and reading of the SSDA (communications link circuit) is placed under direct interrupt control with all action occurring in the interrupt routine. Timing of the SSDA reset at the two second interval interrupt must likewise be performed immediately in the interrupt routine.

The A-D conversion process will likely be too long to allow execution to completion before processing SSDA interrupts. Tasks such as filter tuning could be very lengthy. Therefore A-D conversion cannot be placed on an equal priority with the SSDA, but neither can it be assigned equal status in foreground with the filter tuning and similar tasks. Depending on the number of tasks and their lengths, several alternatives could be selected. Polling could be used if the foreground operations could be segmented to assure processor access by the more critical routines when necessary. Analog-to-digital conversions and gain ranging operations could be processed under interrupt control if these routines could be interrupted by the more time critical SSDA. This technique of nested interrupt routines can provide relief from the time constraints on the longer tasks, but it increases the complexity of program execution and therefore the calculation of maximum execution times of program segments.

Initially, the firmware for system development will be restricted to specific simple tasks such as buffer handling for communications, A-D conversions, and simple CMOS bus reads and writes. Remote loading of code and execution of code in RAM will also be provided. More complicated tasks such as closed loop filter tuning will

be tested through the use of remote loading of RAM, and it will be programmed in ROM after verification.

Figures 40 and 41 show a sample program flow diagram for a single polling loop in the foreground with interrupts for more time critical operations.

6.2. Base Site Software

The base site Motorola 6800 performs two distinct functions. First, it controls all peripheral devices, and therefore it must initialize the system operation. If present, the real-time processor must be loaded from the base M6800 through its 16 bit parallel interface. In order to bootstrap the HP2109, the M6800 simulates the response of a Hewlett Packard paper tape reader, and it loads the HP2109 through the lower 8 bits of the 16 bit interface card as the HP executes its ROM loaded paper tape bootstrap routine.

After loading the real-time processor, the base M6800 will be instructed to bring on-line the remote instrumentation packages as they are powered up. (Remote sites may be brought on-line either before valid data is taken, or during data collection by other remote sites.) This task consists of issuing a command to the new site to load its delay time register with the predetermined delay constant for the specific site and link. The constant must be loaded to establish proper time synchronization, and it must be completed before the return link can establish correct data framing.

FIGURE 40: REMOTE 6800 SOFTWARE

FIGURE 41: REMOTE 6800 INTERRUPT ROUTINES

The second task of the base M6800 is acting as the central data distributor for the entire system. As such it must receive data from up to eight 2560 bits per second incoming links, and it must place this data properly formatted into buffer arrays. It is also responsible for verifying the data and correcting errors where possible. Data from these buffers will be supplied as required either to the real time processor or to the magnetic tape units.

The base M6800 also controls all operator interaction with the system, and therefore it transfers all data to and from the CRT terminal, and all data to the graphics line printer.

In order to provide the necessary response to the links and to the real time processor, the M6800 will provide immediate processing in the interrupt routine for these devices. If delayed, the SSDA's could lose data. If the real time processor were delayed, it would simply fail to maintain its normal rate of requesting data from the M6800. The M6800 data queue would fill and eventually overflow.

If all tasks are kept short, and all input/output is buffered, other functions of the base M6800 can be executed under a polling system. Figures 42 and 43 show flow charts for this base site configuration. Note that Figure 42 shows a specific keyboard mode in which CRT output from the system is deferred while operator commands are keyed in. This is a simple technique to prevent a mixing of keyed characters and system generated message output. If keying of the command is too slow, this method can result in CRT buffer overflow because of accumulation of system messages. Alternate schemes can

FIGURE 42: BASE EMM SOFTWARE

FIGURE 43: ERASE 6800 INTERRUPT ROUTINES

provide writing of alternate characters in the proper locations as they arrive, but without a cursor position readout (which we do not have), this requires dual pointer retention and character counting. Such a scheme is not justified at this point in system development and evaluation.

If any task requires excessive time in the base M6800, the polling techniques described above may be inadequate, and multiple nested interrupt routines will be necessary. This should probably be avoided until more experience is gained with the system. Relative importance of various possible software features is difficult to judge before field testing, and therefore complexity should be avoided until priorities can be established for implementation of useful features.

The base M6800 will maintain a full utility monitor system in ROM. It supports file operations on the magnetic tapes and unbuffered drivers for the CRT and the printer. It also provides mnemonic translation for aid in program patching in the field. In development systems such as our prototype, there should be no need to include the magnetotelluric field system software in the ROM since it can easily be loaded from magnetic tape, and this process allows the use of alternate software systems and provides easy modification of code in the field as new techniques are developed. Similarly, the real-time processor software may be stored on mag tape for loading into the Hewlett Packard 2109.

Later systems which are built primarily for routine field exploration should have the full software stored in ROM, and should probably be modified so the system reset directs the processor to the MT software with the utilities available on command. The HP 2109 includes a remote start-up feature which could be used to provide automatic bootstrap of the real-time processor upon M6800 system reset.

6.3. Real Time Processor Software

The optional Hewlett Packard 21MX (Model 2109) real time processor performs one primary task in the magnetotelluric system. Its relatively high speed, floating point processor, and large memory enable it to perform real time data analysis for six magnetotelluric sites (three B channels and 12 E channels) with an 8 Hz upper frequency. The system organization will allow the 21MX to process the data from a different mix of channels, or to cross process data from multiple sites with only a software change.

Cascade decimation as described by Wight [22] was chosen for the real time processor. A modification of the Wight implementation allows the data points to be queued in the M6800 memory. This alternative to deferred processing (described by Wight) allows the total process to execute to completion after each point. It greatly reduces the software complexity, and is simultaneously increases processing efficiency. (See Figure 44 for a flowchart of the decimation subroutine.) The Hewlett Packard 2109 should use about 70%

FIGURE 44: HP2109 DECIMATION SUBROUTINE

of its capability to process 15 channels in real time. However the radical assymetry of computation within the routine depending upon the sequence number of the input point causes the HP to lag as much as about one second behind the incoming data. This corresponds to 960 bytes which can easily be queued by the M6800.

The required computational capability of the real time processor is set by the combined low frequency and mid frequency real time load. The mid frequency data is processed for only about one half the dwell time at each site. The alternate process is AMT which requires much less computation than the mid band data because the time-to-frequency transformation is performed by the heterodyne receiver on the AMT processor board. The 2109 will be used for the AMT process since it is not run concurrently with the mid frequency data, and therefore ample capacity is available in the 2109. Retaining the same input rates and formats allows the base M6800 to handle the data without distinguishing between the AMT and the mid frequency processes.

Structure of the software is defined to simplify the shift from simultaneous low and mid frequency processing to simultaneous low and AMT frequency processing. The cascade decimation (used for low and mid frequency processing) is written as a single subroutine which is called for each input point regardless of whether low or mid frequency. Loading a set of base register values before the call determines the destination of the output values. The subroutine is called 64 times for mid frequency data after each single call for low

frequency data. The ratio of calls corresponds to the ratio of sample rates. When processing low and AMT data, the decimation routine is called once for low frequency, and then the AMT process routine is called to process 64 points. (Since AMT contains in-phase and quadrature data each at half the mid frequency data rate, the routine will probably be called 32 times and will take into two points per call.) This program flow is shown in Figure 45.

The AMT processor board performs the frequency analysis of the AMT data at the remote site, and therefore AMT processing in the HP2109 is limited to accumulation of the results which arrive pre-processed.

Return communications from the HP2109 to the M6800 consist of 16 bit words which are read by the 6800 as each data value is sent to the HP2109. This technique allows bidirectional communication with a single handshake cycle for a time savings. The 2109 can transfer status in this manner, and it should also be capable of providing a "snapshot" of intermediate accumulated results of its real-time processing. In order to output this data, the HP2109 would transfer the data from the results array to a separate buffer (to prevent further partial accumulation as the transfer takes place). The data could then be transferred to the M6800 with no interruption of real time processing. This data "snapshot" could be a very helpful tool in evaluating system performance, and it could also be used to develop techniques for selecting the best data based on environmental conditions during particular time periods.

FIGURE 45: HP2103 SOFTWARE (MAIN)

The real time processor provides an interesting opportunity to develop a real time data inversion program which would refine its earth impedance estimates as more data became available. Additional tasks required for this feature include correcting the data for system response of the specific channels and inversion of the corrected data. The HP2109 contains adequate memory and speed to perform this task simultaneously with real-time processing as previously defined. However very careful study of timing would be required to implement this added feature because a slight increase in computational load at the wrong time could cause the M6800 queue requirements to grow significantly for the real-time frequency analysis. Because of the queue problem, real time inversion of data will not be included at this time.

7. CONCLUSION

Achievement of virtually all design goals is assured. The initially proposed design for the Department of Energy system has been modified only slightly; and in almost all cases, those changes were made to reduce the number of different subassemblies or to enhance the system functions or flexibility. Every significant aspect of the design has proved to work as expected.

Full software packages are not completed at this time, but representative routines have been written, tested, and timed. Final selection of desired software features should determine ultimate operating characteristics of the system, and this selection will likely be delayed until the system is field tested. In any event, the processor memory sizes and execution speeds should allow any reasonable features to be implemented.

The Department of Energy system should provide the best magnetotelluric data currently available, and it should do so in the most cost effective application of the technique. An exact copy of this system could be used for a minimum cost entry into the field of MT. Because of the modular construction and functional partitioning, many special applications could be addressed with very little additional design effort.

Logical improvements on the present system include replacement of the remote processors with CMOS processors and peripheral chips to

further reduce the power requirements of these instrument packages. A smaller, lower power, and less costly alternative to the real-time processor would be desirable. Reasonable alternatives to these choices are not available at this time, but they should be available in the future. Similarly, progress in transducers should result in the eventual replacement of the six large induction coils now used to measure three components of B-field over the frequency range. Improved preamplifier input characteristics may allow replacement of the buffered metal/metal salt electrodes with less complex and less costly types. Hopefully the new Department of Energy instrumentation system will provide the improved noise performance needed to prompt such transducer developments.

Unless problems are uncovered in field testing of the new Department of Energy system, there is no reason to recommend any change to the prototype design.

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GLOSSARY

- ACIA - Asynchronous Communications Adapter, a 24 pin integrated circuit, MC6850, which provides synchronous communications for Motorola 6800 microcomputer systems
- A/D - Analog-to-Digital; normally used as A/D converter or A/D conversion
- AD7531 - Analog Devices designation of a 12 bit monolithic integrated circuit multiplying digital-to-analog converter
- AMT - Audio Frequency Magnetotellurics; magnetotelluric processes at audio frequencies (Specifically 8 Hz to 1000 Hz in the Department of Energy system)
- ANSI - American National Standards Institute
- baud - (as used in this document) a unit of communications speed equal to one binary bit of information per second
- B field - magnetic field
- byte - a group of eight binary bits, frequently used to represent a single symbolic or alphanumeric character for text storage, processing, or communications
- CMOS - Complementary Metallic-Oxide Semiconductor, a type of integrated circuit using both N-channel and P-channel MOSFET devices to achieve extremely low quiescent power dissipation in digital logic circuits
- CRT - Cathode Ray Tube, used to refer to the cathode ray display tube or to a communications terminal using the display tube
- D/A - Digital-to-Analog, normally used as D/A converter or D/A conversion
- DAC - Digital-to-Analog Converter
- dB - decibel, a designation of relative power of two signals
- DCD - Data Carrier Detect, a signal line used by communications circuits to determine the presence of a communications signal

- DC-100A - the model designation of a small dual spool magnetic tape cartridge with .125 inch wide tape originally introduced by 3M Company (Approx. size .45 x 3.2 x 2.4 inches)
- DC-300A - the model designation of a dual spool magnetic tape cartridge with .25 inch wide tape originally introduced by 3M Company (Approx. size .65 x 6.0 x 4.0 inches)
- DMA - Direct Memory Access, an input/output technique which permits a computer's peripheral device to transfer data to/from memory with no action from the computer processor after initiation of the transfer
- DMAC - Direct Memory Access Controller, a 40 pin integrated circuit, MC6844, which provides control for DMA data transfers in Motorola 6800 microcomputer systems
- DOE - United States Department of Energy
- D2 - abbreviation of MEK6800D2 Evaluation Kit II for the Motorola 6800 microcomputer
- E field - electric field
- EPROM - Erasable Programable Read-Only-Memory
- ERDA - Energy Research and Development Administration (now U. S. Department of Energy)
- FET - Field-Effect Transistor
- hex - (1.) composed of six, (2.) hexadecimal, base 16 number system (used when referring to computer addresses)
- IGFET - Insulated Gate Field-Effect Transistor, more commonly known by the more specific term, MOSFET
- Hz - Hertz, a unit equal to cycles per second
- HP21MX - the model designation of a series of Hewlett-Packard 16 bit minicomputers
- HP2109 - a specific model of the 16 bit Hewlett-Packard minicomputer series
- HP9825 - the model designation of a Hewlett-Packard desktop computer

- JBUG - name of a Motorola monitor system provided on a 1024 byte ROM with the MEK6800D2 Evaluation Kit (provides support for a keypad and audio magnetic tape cassette recording at 300 baud)
- LED - Light Emitting Diode
- MC14040 - Motorola part number designating a CMOS digital integrated circuit containing a 12-bit binary counter
- MC14049 - Motorola part number designating a CMOS digital integrated circuit containing an inverting hex buffer
- MC14502 - Motorola part number designating a CMOS digital integrated circuit containing a strobed hex inverter/buffer
- MC6830AP-2 - Motorola part number for a 1024 byte mask programmable Read-Only-Memory, specifically programmed with the JBUG monitor program
- MEK6800D2 - model designation of the Motorola Evaluation Kit for the 6800 microprocessor (includes two printed circuit boards with a 25 key input pad and 6 hexadecimal LED displays)
- MLM339 - Motorola part number for an integrated circuit containing quadruple analog comparators with open collector saturating outputs
- MMS68104 - model designation of the Motorola 16K byte dynamic random access memory printer circuit board for the MEK6800D2 Evaluation Kit
- MOSFET - Metallic Oxide Semiconductor Field-Effect Transistor
- MT - Magnetotelluric
- M6800 - abbreviation of Motorola 6800 Microprocessor
- NE5534 - Signetics designation for a high performance, low noise, monolithic integrated circuit operational amplifier
- OP-10 - Precision Monolithics Incorporated designation of a very low noise, relatively slow speed instrumentation type monolithic integrated circuit operational amplifier

- PIA - Peripheral Interface Adapter, a 40 pin integrated circuit, MC6820 or MC6821, which provides 20 parallel input or output pins for the Motorola 6800 microcomputer systems
- Q - Quality factor for resonant electrical circuits; equal to two times π times the ratio of energy stored to the energy dissipated per cycle
- PROM - Programmable Read-Only-Memory
- RAM - Random Access Memory
- RC - Resistor-Capacitor, a common pairing of electronic components to provide passive filtering of signals
- ROM - Read-Only-Memory
- RS232 - a specification for electronic data communication determined by the Electronics Industries Association
- SN7402 - Texas Instruments part number for a digital TTL circuit containing a quadruple 2-input NOR gate
- SN7406 - Texas Instruments part number for a digital TTL circuit containing a hex inverter buffer with high voltage open-collector outputs
- SN7407 - Texas Instruments part number for a digital TTL circuit containing a hex buffer with high voltage open-collector outputs
- SN7408 - Texas Instruments part number for a digital TTL circuit containing a quadruple 2-input AND gate
- SN7474 - Texas Instruments part number for a digital TTL circuit containing a dual D-type positive-edge-triggered flip-flop with preset and clear
- SSDA - Synchronous Serial Data Adapter, a 24 pin integrated circuit, MC6825, which provides synchronous data communications interfaces for the Motorola 6800 microcomputer systems
- TTL - Transistor-Transistor Logic, a common family of digital integrated circuits using multiple emitter bipolar transistor inputs driving inverting bipolar outputs for the NAND function (Other functions are derived with additional inversions.)

VMA - Valid Memory Address, a signal on the Motorola 6800 bus used to indicate that the current value on the address lines is valid and should be decoded for system operation

WWV - designation of the National Bureau of Standards radio stations providing continuous time references

2N6550 - designation of an extremely low noise discrete junction field-effect transistor (JFET) designed for linear small signal amplifier applications

3N138 - designation of a RCA discrete MOSFET designed for analog small signal switching applications

VITA

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