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MIS SOLAR CELLS ON THIN POLYCRYSTALLINE SILICON

Progress Report No. 2, June 1—August 31, 1980

By
Wayne A. Anderson

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The State University of New York at Buffalo
Electrical Engineering Department
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U.S. Department of Energy

Solar Energy

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June 1, 1980 - August 31, 1980

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September 1980

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Prepared For The

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OBJECTIVES

Task 1 of this project involves electron-beam deposition of thin silicon films on low cost substrates. The goal is to obtain 20 μm thick films having 20 μm diameter crystallites which may be recrystallized to $> 40 \mu\text{m}$. Material characterization and device studies are to be included in efforts to reach a 6% conversion efficiency by March 1981.

The second task deals with MIS solar cell fabrication on various types of silicon including poly-Si, ribbon-Si, silicon on ceramic, and thin film silicon. Conduction mechanism studies, optimum engineering design, and modification of the fabrication process are to be used to achieve 13% efficiency on Xtal-Si and 11% efficiency on poly-Si.

Task 3 involves more detailed test procedures and includes spectral response, interface and grain boundary effects, computer analysis, materials studies, and grain boundary passivation. Stability and degradation studies will be performed as part of Task 4.

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1. SUMMARY

Efforts in the thin e-beam deposited Si area have centered on Si on Si deposition, materials analysis, and some electrical characterization. A highly crystalline Si thin film has been observed with a (111) orientation on a (111) substrate. An epitaxial type of growth is observed with the film duplicating the features of the substrate. Details concerning impurities in the film and electrical characteristics will be reported in the next quarterly report.

MIS cells have been fabricated on RTR ribbon, Hamco Si, Wacker poly-Si, Silicon and Ceramic, and IBM ribbon. Efficiency values range from 11% to 5% depending on choice of substrate. Differences in interface state density and in diffusion length appear to be the main contributors to this range in efficiency values. Spectral response, diffusion length, and interface state densities are reported. MIS cells were also fabricated using Hf, Al, and Pd as Schottky metals. All gave results far inferior to the Cr which is not surprising in such a short study. The sputtered Hf gave a low V_{oc} even though ϕ_m is very low for Hf. We feel that sputtering serves to increase interface state density to reduce V_{oc} .

Further studies using Auger and ESCA show the presence of C, Ag, F, and Al contaminants in our Cr films. The interfacial oxide composition can be controlled by using various oxide growth techniques.

Reliability studies indicate an initial degradation in V_{oc} for the Cr-MIS cells but quite stable performance thereafter.

2. INTRODUCTION

This project is undertaken to develop a low-cost, thin-film, MIS solar cell which will eventually sell for < 50¢/watt. The MIS process is being optimized for single crystal silicon and poly-Si prior to application to thin-film Si. This involves fabrication, grain boundary effects, and reliability studies. Thin Si films are e-beam deposited on Si, stainless steel, Ti, and glass substrates to evaluate the potential for future use as a low-cost semiconductor. It is our intent to combine the optimized MIS process with the thin e-beam Si film to produce a low-cost vacuum process to fabricate solar cells.

The key features of this report include MIS fabrication, reliability studies, thin Si film deposition and analysis, and surface analysis.

3. THIN FILM SILICON DEPOSITION AND ANALYSIS

Solar cells are now commercially available at a cost of about \$10/peak watt. The Department of Energy has established a goal of 30 - 50¢/peak watt to produce low-cost solar generated electrical power. One way to meet this goal is to reduce the amount of semiconductor material used in solar cells and to eliminate the necessity of cutting and polishing the semiconductor wafers. Several techniques are being explored to produce low-cost Si films for solar cell fabrication. Included in these techniques are the IBM and EFG ribbon growth methods,^[1] silicon on ceramic produced by Honeywell,^[2] RTR ribbon produced by Motorola,^[3] epitaxial growth on metallurgical grade (MG) Si by RCA,^[4] and CVD of Si on MG Si substrates^[5] by T. L. Chu of Southern Methodist University. The first three methods do not produce a truly thin Si film ($< 50 \mu\text{m}$) and the last two methods at present are not large volume techniques.

Electron beam (e-beam) deposition of Si on foreign substrates has been investigated by Fang and Eprath,^[6] Kipperman^[7] and Feldman.^[8] Recently, we have reported^[9] on e-beam deposited Si films on Al-coated Ti or stainless steel substrates. It is necessary to have substrate temperature in excess of 450°C for $0.5 - 1 \mu\text{m}$ diameter crystallites and in excess of 1100°C for $5 - 20 \mu\text{m}$ diameter crystallites. A vacuum of 5×10^{-5} to 5×10^{-8} Torr has been used by the various research teams.

A possibly more practical approach which we have recently explored involves e-beam deposition of a thin Si film on a Si substrate. Success in this area would lead to $20 - 30 \mu\text{m}$ thick high quality Si films on a low-cost MG Si substrate to produce a low-cost solar cell. Current work involves the use of (100), (111) and polycrystalline substrates heated to about 500°C prior to deposition of the Si film. A vacuum of 5×10^{-6} - 1×10^{-5} Torr is used in this work. A pre-doped Si charge, located in a water-cooled Cu crucible, is melted using a 2 KW electron beam. This gives a Si deposition rate of $1 - 2 \mu\text{m}/\text{min}$ on the substrate surface located about 12 cm from the source. We wish to report on the observed film growth and crystallite orientation which indicate the significant potential of this deposition technique.

Scanning electron micrographs are shown in Figures 1 - 4 for e-beam Si films. Figure 1 shows an e-beam Si film on an Al coated stainless steel substrate. The rounded features indicate the tops of columns which originate at nucleation centers on the Al surface and propagate towards the Si surface.^[9] The column diameters measure 3 - 5 μm . A quite different structure is formed when Si is deposited on a Si substrate. Figure 2 shows the result when using an unpolished Si substrate shown on the right. The 16 μm Si film, shown as the elevated region on the left, exhibits the same surface features as the substrate. An enlarged view of the Si film, shown in Figure 3, indicates surface features characteristic of unpolished crystalline Si. A similar SEM study was performed on a 10 μm e-beam Si film on a polished Si substrate as shown in Figure 4. Etch pits on the substrate surface (bottom) are replicated by the e-beam Si film (top) with the film edge shown as a dark line in the center of the figure. An optical micrograph of a similar film is shown in Figure 5 to clearly show how the surface features of the substrate are reproduced in the film.

Information concerning crystallinity of the e-beam Si films was obtained using a diffractometer with Cu K_α X-ray. An analysis of a film on a (100) substrate is shown in Figure 6 to exhibit a preferred (111) orientation with significant contributions from the (220), (311), (400) and (331) peaks. This film was heated to 1200° C which caused a significant increase in crystallinity as evidenced by growth of the (111) peak shown in Figure 7. Data for the (100) substrate are shown as a dashed line for comparison. The preference for a (111) orientation of an e-beam Si film on a (100) substrate suggested the use of a (111) substrate. X-ray data for this case, shown in Figure 8, indeed indicate an advantage in using a (111) substrate. The film now exhibits a very sharp (111) peak with very little indication of other peaks. This leads us to conclude that the e-beam Si film is highly crystalline and quite nicely duplicates the (111) substrate, typical of epitaxial growth.

This study has shown that e-beam deposition of Si on a Si substrate held at $\approx 500^\circ\text{C}$ leads to a crystalline film which structurally replicates the substrate. This thin (10 - 20 μm) Si film prefers to grow in a (111) orientation which suggests the use of a (111) substrate to produce a high degree of crystallinity. The use of a (100) substrate produces a strong (111) peak in the film but other peaks are significant as well. The

Figure 1 Scanning electron micrograph
of a thin Si film on Al-coated
stainless steel (5000X).

Figure 2

Scanning electron micrograph showing the edge of a thin Si film (left) on an unpolished Si substrate (right) (600X).

Figure 3

An expanded view of the Si film of Figure 2 (3000X).

Figure 4 Scanning electron micrograph showing the edge of a thin Si film (top) on a polished Si substrate (bottom) (1000X).

Figure 5 Optical micrograph showing identical surface features of film (top) and substrate (bottom) in a Si film on polished Si (400X).

Figure 6 X-ray analysis of a thin Si
film on a (100) Si substrate.

Figure 7 X-ray analysis of an annealed thin Si film on a (100) Si substrate.

Figure 8 X-ray analysis of a thin Si
film on a (111) Si substrate.

question of preferred orientation for e-beam deposited Si is of interest. Several authors^[10] have noted a preferred (110) orientation in CVD Si films which is a function of temperature, rate and dopant. Thin Si films prepared by vacuum evaporation have shown a preferred (110) orientation when deposited on foreign substrates.^[9,11] A firm understanding of the cause for these preferred orientations has not yet been presented. The data reported herein indicate that crystalline Si films may be formed in the 500 - 600° C temperature range by e-beam deposition of Si on a Si substrate with no evidence of grain boundaries. This process may be advantageous in producing low cost solar cells or other semiconductor devices.

Dr. C. V. Clemency of Geological Sciences at SUNY Buffalo was most helpful in the X-ray studies.

4. MIS SOLAR CELL FABRICATION

4.1 Effect of Different Substrates

A primary factor in preventing the large-scale use of solar cells for terrestrial application involves the high cost of Si. Solar cell cost is now about \$10/peak W. compared to the D.O.E. goal of < 50¢/peak W. Much of this cost can be eliminated by using low-cost Si production methods. We have studied several new types of Si using a MIS structure for fabricating a rectifying junction. We have measured the conversion efficiency as a function of Si source and have determined which material properties are most sensitive to the particular Si process. These results using a MIS structure are compared to similar data by other researchers for p-n junction structures.

Several different silicon sources were utilized in this study. Several unpolished 5 inch diameter Czochralski Si slices (HK) were supplied by Hamco-Kayex of Rochester, New York. Wacker cast polycrystalline Si (WP) was obtained from Wacker-Chemitronic. Si on ceramic^[12] (SOC) was supplied by J. D. Zook of Honeywell, IBM ribbon Si (IBMR) by the Jet Propulsion Laboratory and RTR ribbon Si by K. Sarma of Motorola. All samples except for SOC were degreased and then etched in a planar acid solution^[13] (8% HF, 75% HNO₃, 17% CH₃COOH by vol.) to form a polished Si surface. The planar solution gives a uniform etch rate irrespective of crystallite orientation and grain

boundaries. The need for a planar etch is illustrated in Figure 9 (top) which represents the Si surface of WP Si after a CP4 etch. Significant preferential etching at grain boundaries is revealed. A twin boundary is revealed parallel to the left-hand grain boundary. A different texture for adjacent grains is also revealed indicating different crystallite orientations and supporting the need for a planar etch. A similar sample was treated with a planar etch as shown in Figure 9 (bottom). This photomicrograph shows a much more uniform surface as evidenced by a sharp focus on adjacent grains even though one grain boundary is quite significant. The SOC sample was not etched in order to preserve the ohmic back contact which was supplied.

MIS solar cells were fabricated^[14] having a structure 700 Å SiO₂ A/R coating - 1 μm Al grid - 50 Å Cu - 30 Å Cr - 20 Å SiO_x - Si substrate. The SiO_x layer serves to reduce interface state density and to reduce majority carrier current to increase solar cell efficiency.^[15] The Cr layer serves as the Schottky contact whereas the Cu layer reduces the sheet resistance without significantly decreasing optical transmittance. All solar cells were tested for photovoltaic response, dark I-V characteristics, and spectral response. Photovoltaic data were taken using an ELH quartz - halogen lamp set at an AM1 level with a standard cell recently calibrated at NASA - Lewis Research Center. Data from these simple tests were used to compare the qualities of the four types of silicon tested in this work.

A summary of photovoltaic, and dark I-V data for several MIS solar cells on four different Si substrates is given in Table 1. V_{oc} data are observed to decrease from 0.57 V to 0.50 V when comparing HK to RTR, WP, SOC, and IBMR substrates. J_{sc} was observed to progressively decrease from 29 mA/cm² to 18 mA/cm² for HK, WP, IBMR, RTR, and SOC substrates. Fill factor was lowest for the IBMR samples compared to all of the others but was quite high on RTR ribbon. A reduced J_{sc} is caused principally by a lower diffusion length, L. The value for L may be estimated by

$$J_{sc}(\lambda) = q \phi(\lambda) T_r(\lambda) \frac{\alpha(\lambda) L}{1 + \alpha(\lambda) L} \quad (1)$$

where ϕ = photon flux density, T_r = transmittance, and α = absorption coefficient in silicon. Spectral response (SR) data are shown in Figure 10

Figure 9 Grain boundaries in Wacker
Top
poly-Si polished using CP4.
Difference in texture indicates
etching of grains having
different orientations.

Figure 9 Wacker poly-Si polished with
Bottom
a planar etch which produces
a much more uniform surface.

TABLE I
SUMMARY OF SOLAR CELL PHOTOVOLTAIC DATA

<u>Substrate</u>	<u>Sample No.</u>	<u>V_{oc} (V)</u>	<u>J_{sc}[*] (mA/cm²)</u>	<u>Fill Factor</u>	<u>Efficiency (%)</u>		<u>n-Factor</u>	
					<u>Active</u>	<u>Total</u>	<u>Dark</u>	<u>Light</u>
Hamco (5" dia. chemical polish only)	HK1	0.58	31	0.64	11.4	10.3	1.39	
	HK2	0.56	28	0.73	11.5	10.4	1.50	
	HK3	0.56	32	0.61	11.0	9.9	1.40	
	HK4	0.56	28	0.70	10.9	9.8	1.43	1.08
Hamco (Poly)	HK5	0.57	26	0.65	9.6	8.6		
Wacker (Poly)	WP1	0.52	24	0.67	8.4	7.6	1.60	
	WP2	0.54	29	0.67	10.5	9.5	1.43	
	WP3	0.53	23	0.69	8.9	8.0	1.46	1.27
	WP4	0.53	26	0.64	8.8	7.9	1.32	1.11
RTR Ribbon	RTR1	0.56	19	0.74	7.9	7.1	1.28	1.02
Silicon on ceramic	SOC1	0.51	18	0.68	6.1	5.5	1.90	1.32
	SOC2	0.52	20	0.59	5.9	5.3		
IBM Ribbon	IBMR1	0.47	20	0.54	5.1	4.6	2.2	2.15
	IBMR2	0.50	22	0.54	6.0	5.4		

* Based on NASA - Lewis calibration and using ELH lamp @ 100 mW/cm².
Active area = 2.0 cm². Grid coverage = 10%.

which compare data for HK, WP, IBMR, and SOC samples to a p-n junction solar cell. Values for L may be obtained for these samples using L for a MIS standard cell and the equation

$$\frac{J_{sc}(\lambda)_1}{J_{sc}(\lambda)_2} \approx \frac{L_1}{L_2} \quad (2)$$

which holds when $\lambda > 0.8 \mu\text{m}$, $\alpha L \ll 1$, $\phi_1 = \phi_2$, and $T_{r2} = T_{r1}$. Thus, $L_{HK} = 150 \mu\text{m}$, $L_{WP} = 72 \mu\text{m}$, and $L_{IBMR} = L_{SOC} = 39 \mu\text{m}$ which account for the reduced J_{sc} values. A shift to the left in the SR curves also suggests a reduced value for L.

The J-V equation for a majority carrier MIS cell may be expressed by [16]

$$J = A^* T^2 \exp\left(-\frac{\phi_B}{kT}\right) \exp\left(-x^{\frac{1}{2}}\delta\right) \left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (3)$$

where A^* = Richardson's constant, ϕ_B = barrier height, x = effective tunneling barrier, δ = interface oxide thickness, and n = ideality factor.

The n - value is given by

$$n = 1 + \frac{q\delta D_s}{\epsilon_i \epsilon_0} \quad (4)$$

where D_s = interface state density, and ϵ_i = dielectric constant of the insulator. Equation 4 is valid when the interface states are in equilibrium with the semiconductor. [17] Equations 3 and 4 may be solved for V_{oc} when $J = 0$, to produce [15]

$$V_{oc} = -4.95 - 0.215 n - \phi_m + 0.026 n x^{\frac{1}{2}}\delta \quad (5)$$

where ϕ_m = metal work function. Equations 3 and 4 may then be used to calculate D_s and V_{oc} from a knowledge of n and ϕ_m taking $x^{\frac{1}{2}}\delta = 2$. D_s values are calculated using both dark (n) and light (n') n - values as shown in Table 2. The n' calculation gives $D'_s < D_s$ due to light generated carriers which fill the interface states and decrease D_s . D_s is higher for SOC 1 because the sample was not etched to reduce surface imperfections as was the case for HK4 and WP3. The high value for IBMR1 is thought to be caused in part by an unknown degradation mechanism and in part by the nature of the ribbon growth technique as shown in previous work. [18] V_{oc}

TABLE 2

AN ANALYSIS OF PHOTOVOLTAIC DATA

Sample	n-Factor		D_s from eq. 4 ($\text{cm}^{-2}\text{eV}^{-1}$)		V_{oc} from eq. 5 (V)		exp.
	Dark	Light	Dark	Light	Dark	Light	
RTR	1.28	1.02	2.7×10^{12}	1.9×10^{11}	0.58	0.57	0.56
HK4	1.43	1.08	4.2×10^{12}	7.8×10^{11}	0.56	0.56	0.56
WP3	1.46	1.27	4.4×10^{12}	2.6×10^{12}	0.55	0.545	0.53
SOC1	1.90	1.32	8.7×10^{12}	3.1×10^{12}	0.48	0.52	0.52
IBMR1	2.20*	2.15*	1.2×10^{13}	1.1×10^{13}	0.43	0.38	0.38*

* These data taken 1 year after initial fabrication and show device degradation.

was calculated from equation 4 using $\phi_m = 4.16$ eV for the dark case and $\phi_m = 4.21$ eV for the light case since ϕ_m is a function of fixed oxide charge, effective interface oxide charge and effective interface oxide thickness which change under illumination conditions.^[15] Data in Table 2 indicate much more consistent results between calculated and measured values of V_{oc} using n values rather than n - values indicating the significance of using data from illuminated I-V curves in predicting V_{oc} . These data also confirm the validity of equations 3-5 for the Cr-p-type Si MIS device.

These results indicate a reduced solar conversion efficiency when using special types of silicon. This reduced efficiency may be caused by surface imperfections (chemical or structural) or reduced diffusion length due to grain boundaries, chemical impurities, or structural imperfections. A comparison of MIS cells on special Si to those on Monsanto Si (M) shows efficiency values of $\eta_{HK} = 0.91 \eta_m$, $\eta_{WP} = 0.72 \eta_m$, $\eta_{RTR} = 0.64 \eta_m$, $\eta_{SOC} = 0.48 \eta_m$, and $\eta_{IBMR} = 0.44 \eta_m$. Similar data on p-n junction cells on special Si compared to single crystal Si wafers (X)^[12,19] shows $\eta_{WP} = 0.8 \eta_x$, $\eta_{SOC} = 0.7 \eta_x$, $\eta_{EFGR} = 0.6 \eta_x$, where EFGR refers to EFG ribbon Si. The p-n junction cells have the advantage of less sensitivity to surface imperfections which gives a higher efficiency. MIS cells on SOC gave a significantly lower efficiency due to lack of surface preparation.

We wish to acknowledge the help of R. Lane of Hamco-Kayex, D. Zook of Honeywell, and T. Daud of Jet Propulsion Laboratories for supplying samples of Si.

4.2 Effect of Different Schottky Metals

A preliminary study of the use of different Schottky metals was conducted. Data for several of these samples are given in Table 3 where Pd, Al, and Hf metals were used. Pd gave a very low V_{oc} on p-Si which is to be expected since $\phi_m = 4.8$ eV for Pd which would give a low ϕ_B on p-Si. Al gave reasonable data accounting for the fact that a poor A/R coating and rather thick (100 Å) Al films were used. Hf was evaluated because of its low work function (3.2 eV) which should give a very high ϕ_B on p-type Si. Unfortunately, Pd must be sputtered which produces a M-S device rather than a MIS device. The sputtering process probably also produces a surface state density in the 10^{13} eV⁻¹-cm⁻² range which would greatly reduce V_{oc} .

From this brief effort, I would conclude that it is not wise for a small research group to try to evaluate several different MIS systems. A change in either M, I, or S in the MIS device can lead to the need for a completely new evaluation of all other variables such as:

- a) Semiconductor - doping type, resistivity, orientation, etching, thickness,
- b) insulator - type, thickness, growth temperature, growth atmosphere, pre-treatment of semiconductor,
- c) metal - thickness, rate, vacuum, atmosphere.

We will continue to concentrate on optimization of the Cr-MIS system in our device fabrication studies.

TABLE 3

MIS CELLS USING DIFFERENT SCHOTTKY METALS

Samples	Substrate	Schottky Metal	V_{oc} (V)	J_{sc} (mA/cm ²)	FF	Efficiency (%)	n-factor	
							dark	light
186	Wacker	Pd	0.02	20	-	-	-	-
188	Wacker	Al	0.44	8.0*	0.60	2.1	1.43	1.21
190	Wacker	Al	0.48	9.5*	0.69	3.2	1.44	1.40
193	<100>	Hf**	0.26	4.8	0.24	0.3	-	1.45

* Al thickness = 100 Å gives high optical absorption. Also, the A/R coating was poor.

** The hafnium was sputtered.

5. ANALYSIS OF MIS SOLAR CELLS

5.1 An Analysis of I-V-T Data Related to Grain Boundaries

Further studies were made into the current propagation mechanisms in grain boundaries. Most practical solar cell materials, that are polycrystalline, have columnar grain structures oriented perpendicular to the surface. It is known that the lattice mismatch at the grain boundaries produces dangling bonds that are traps for minority carriers. It is important to determine the number of dangling bonds and their behavior under applied electric fields. The present investigations seek to arrive at this goal by I-V measurements from 77° K to 400° K on Cr-MIS type diodes and ohmic contacts made across grain boundaries. The feasibility of this type of experimental study in clearly identifying grain boundary properties was shown in a previous report.^[20]

In the case of a Cr-MIS diode the type of conduction can be identified by a J vs $10^3/T$ plot. Figure 11 shows one such computer-generated family of curves with bias as a parameter. Above 250° K, the linearity of the curve brings out the Schottky type emission across an MIS barrier. Below 250° K, a temperature independent current flow predominates thereby indicating significant tunneling current. Figure 12 is a plot of J/T^2 vs $1/kT$ with bias as a parameter, for the same diode as in Figure 1. At low bias and low-to-medium temperature, the presence of a dip indicates that the shunt resistance of the diode is small. This is typical of all diodes made on grain boundaries. Many workers have assumed that the grain boundary acts as a current shunt and have modified their solar cell equivalent circuit to account for this fact. Our study corroborates this assumption and suggests an additional modification using a field dependent shunt resistance. Figure 13 is an activation energy plot of the same diode as in Figure 12 for temperatures above 250° K. A small bias modulation of activation energy around a constant value indicates a voltage dependent shunt resistance. More data is necessary on similar diodes, but work has been slow due to the non-availability of large grain polycrystalline silicon.

Figure 11 J-1000/T data for a Cr-MIS diode on poly-Si.

Figure 12 $J/T^2 - 1/kT$ data for a Cr-MIS diode on poly-Si.

Figure 13 Activation energy plot for a
Cr-MIS diode on poly-Si.

Cell #: 168-R2

One type of poly-Si that has been available is that made by Semiconductor Processing Co., Hingham, Massachusetts. These wafers are p type poly-Si, boron doped, 1" x 1" in area and have a single crystal core at the center whose perimeter is a grain boundary running vertically down. The other side of the grain boundary is made of poly-Si. A Cr-MIS diode made for our I-V-T studies lies partly on X-TAL and partly on poly-Si. The resistivity of the poly-Si is so high that X-TAL characteristics predominate and it is difficult to isolate grain boundary behavior. Nevertheless, the contacts made on the grain boundary show more conductivity than the grain itself, showing the action of a grain boundary as a current shunt.

A very comprehensive computer analysis of current flow in the vicinity of a grain boundary in an MIS type structure is now being made. This would incorporate a two-dimensional flow of carriers in the bulk, the grain boundary and the intermediate regions within a diffusion length distance away from the grain boundary. A theoretical study of current flow in grains and grain boundaries to conform with experimental findings is under way.

5.2 Auger, ESCA, and Ellipsometer Studies

Surface studies are continuing using a combination of Auger, ESCA, and ellipsometer measurements. We previously reported^[20] a 20 Å interfacial oxide on our standard MIS cells as measured by ellipsometry. Auger and ESCA data indicate the 20 Å oxide to not be SiO₂ but that thicker oxides do consist mainly of SiO₂. The Cr layer in our MIS cell was shown to consist of Cr + O₂ and then Cr + C₂ + Cr₂ C₃.

Further studies were made this past quarter to investigate similar properties but with altered fabrication conditions. Table 4 indicates fabrication parameters used in these samples. In Sample 180, a large amount of C, Ag, F, and Al contamination was detected on the oxide surface as shown in the AES profile of Figure 14. This ESCA profile indicated SiO₂ with Si and Al in the oxide layer. Sample 181 gave a much sharper SiO₂ peak indicating a stronger SiO₂ contribution in the oxide. A similar result was shown in Sample 182.

Figure 14 AES profile showing impurities
in MIS structure.

A more complete set of data is available for Sample 183. Figure 15 shows a greatly reduced C contamination in the Cr due to the use of a better vacuum in the deposition system. Perhaps the most significant result is that SiO_2 is detected in the oxide layer not covered by Cr (see Figure 16), but the layer covered by Cr does not show an SiO_2 contribution. Either the SiO_2 layer cannot be adequately detected when covered by Cr or the Cr interacts with SiO_2 to decompose the original SiO_2 layer.

These data indicate the care which must be taken in establishing a consistent fabrication technique. The Cr deposition rate, vacuum, and thickness are of utmost importance. Growth of the interfacial oxide must be firmly established as to time, temperature, and atmosphere. A more complete picture will be available upon analysis of samples 180-182.

TABLE 4

FABRICATION DETAILS FOR SAMPLES USED IN
AUGER, ESCA, AND ELLIPSOMETER STUDY

<u>Sample</u>	<u>Oxide Growth</u>	<u>Cr Deposition</u>		
		<u>Time (s)</u>	<u>Vacuum (Torr)</u>	<u>Thickness ($\text{\AA}$)</u>
180	Ramp to 580°C in O_2	59	2×10^{-5}	28
181	Hold at 580°C in O_2 for 5 minutes	35	2×10^{-5}	31
182	Hold at 625°C in O_2 for 1 minute	29	1×10^{-5}	30
183	Ramp to 600°C in Air	10	8×10^{-6}	100

Φ AES SURVEY
MOD= 6
5.00KV, 24.000UA
FILE: 183

SF= 5.860
DAT= 1.68
MOC 45 BUR

Figure 15 AES profile showing reduced C
contamination when using a better
vacuum.

⊕ ESCA MULTIPLEX
PE= 50
MG. 8.0KV. 40.0MA
FILE: 918304

SF= .498
OAT= 1.96
ESC MUL 5147 50 150

Figure 16 ESCA profile showing SiO_2 in
oxide uncovered by Cr.

6. RELIABILITY STUDIES

In this part of the project, we continued the study of MIS degradation and investigated cell encapsulation. Cells were tested using an ELH lamp to simulate AM1 illumination. Solar cells used in the degradation study were subjected to either shelf-life or light-bias conditions (Table 5). Shelf-life studies were conducted by placing cells in darkness and each month performing photovoltaic tests. Table 5 indicates that the efficiency (Eff.), open circuit voltage (V_{oc}), and short circuit current (I_{sc}) of these single crystal silicon solar cells remained relatively constant.

Under the light-bias condition, cells operating at their maximum power points were continuously illuminated by a 300 W tungsten lamp. As shown by Figure 16 the efficiency of the cells decreased a maximum of 15% to a relatively constant value. The open circuit voltage (V_{oc}) exhibits the same trend. (Table 5).

Silver-bond conductive epoxy was used to bond copper leads to cells prior to encapsulation. Front contact resistance ranged from 0.18 to 0.52 ohms. Back contact resistance was reduced from this level. Data from Table 6 indicates that the use of Sylgard 184 encapsulant decreases the cells efficiency (Eff.) and short circuit current (I_{sc}) by approximately 13 and 7-1/2 percent, respectively. The thickness of the encapsulant was varied for each cell. Sample ACI was dipped in encapsulant and samples AAA and ACD were encapsulated in molds. Mild detergent was found to be a good releasing agent. As the thickness of the encapsulant increases, the change in the short circuit current (ΔI_{sc}) due to encapsulation decreases (Table 6). For example, as the encapsulant thickness increases (samples ACI and ACD), the change in short circuit current (ΔI_{sc}) decreases from 5 mA to 3 mA. p-n solar cells were encapsulated with the MIS cells. However, the efficiency (Eff.) and the short circuit current (I_{sc}) of the p-n cells increased upon encapsulation. It was also found that the change in short circuit current (ΔI_{sc}) increased with increasing encapsulant thickness. This indicates that for both MIS and p-n cells, as the encapsulant thickness, the short circuit current increases. These cells have been place in a solar panel that is exposed to weather conditions. Further study will reveal whether the Sylgard 184 encapsulant has adverse effects on the performance of the cells.

TABLE 5

SOLAR CELL RELIABILITY DATA

A. SHELF LIFE STUDY

<u>Cell</u>	<u>Date</u>	<u>V_{oc} (V)</u>	<u>J_{sc} ($\frac{\text{mA}}{\text{cm}^2}$)</u>	<u>FF</u>	<u>P_o ($\frac{\text{mW}}{\text{cm}^2}$)</u>	<u>Comments</u>
EC	9/21/79	0.51	24.0	0.72	8.8	XTAL Now Illuminated
	3/6/80	0.51	24.5	0.65	8.1	
	4/29/80	0.48	23.5	0.70	7.9	
FE	8/22/79	0.53	28.5	0.71	10.7	XTAL
	1/24/80	0.54	26.6	0.72	10.3	
	5/8/80	0.53	25.5	0.69	9.4	
	5/27/80	0.52	23.5	0.70	8.6	
	7/30/80	0.52	27.0	0.73	10.3	
	8/25/80	0.53	26.0	0.75	10.3	
AJF	10/12/79	0.53	28.6	0.63	9.6	XTAL
	4/8/80	0.51	30.0	0.68	10.4	
	4/29/80	0.51	30.5	0.61	9.4	
	5/27/80	0.50	28.0	0.68	9.5	
	6/27/80	0.50	29.0	0.66	9.6	
	7/30/80	0.50	31.5	0.69	10.7	
	8/25/80	0.51	30.0	0.72	10.9	

B. LIGHT BIAS STUDY

ABF	3/18/80	0.53	26.0	0.68	9.4	Hamco, Pressure Contract
	5/8/80	0.51	25.5	0.67	8.7	
	5/27/80	0.51	22.5	0.70	8.0	
	6/27/80	0.51	23.5	0.68	8.2	
	7/30/80	0.51	24.5	0.66	8.3	
	8/25/80	0.51	24.0	0.68	8.4	
AFB	4/1/80	0.50	23.5	0.63	7.4	Wacker, Silver Epoxy
	5/8/80	0.49	22.0	0.58	6.3	
	5/27/80	0.48	19.5	0.54	5.0	
	6/27/80	0.49	21.5	0.51	5.4	
	7/30/80	0.49	20.0	0.55	5.4	
	8/25/80	0.49	22.0	0.50	6.1	
EC	5/27/80	0.48	21.5	0.72	7.4	XTAL
	6/27/80	0.48	23.5	0.72	8.2	
	7/30/80	0.48	24.0	0.72	8.3	
	8/25/80	0.48	23.5	0.72	8.1	

TABLE 6
SOLAR CELL ENCAPSULATION DATA

Before Encapsulation*					After Encapsulation**			
Sample	Comments	V_{oc} (V)	I_{sc} (mA)	Eff. (%)	V_{oc} (V)	I_{sc} (mA)	Eff. (%)	ΔI_{sc} (mA)
ACI	Wacker poly	.506	51	8.76	.496	46	6.85	5
AAA	XTAL	.488	58	9.36	.497	54	8.82	4
ACD	Hamco	.511	51	8.05	.503	48	7.04	3

* Using Sylgard 184

** Encapsulant increases in thickness from ACI to AAA to ACD.

Figure 17 Reliability data on Cr-MIS solar cells.

7. CONCLUSIONS

1. E-beam Si film on Si substrates are crystalline at 500-600° C substrate temperatures during deposition. An epitaxial type of growth is observed.
2. ESCA and Auger studies reveal significant carbon in the metal films for our MIS cells. Composition of the insulator layer may be controlled by growth conditions.
3. MIS cells on different Si substrates perform in a manner consistent with p-n junction cells on the same substrate.
4. Reliability studies indicate some initial degradation but then quite stable performance.

8. PLANS FOR THE NEXT QUARTER

1. Improve the purity of e-beam deposited Si films.
2. Further evaluate electrical properties of e-beam Si films.
3. Further evaluate MIS cells on various types of Si.
4. Improve the maximum MIS efficiency on single-crystal Si.
5. Evaluate grain boundary effects using I-V-T and lock-in-amplifier studies.
6. Continue reliability studies.

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APPENDIX A

GRAIN BOUNDARY EFFECTS AND CONDUCTION MECHANISM
STUDIES IN CHROMIUM METAL-INSULATOR-SILICON
SOLAR CELLS ON POLYCRYSTALLINE SILICON

GRAIN BOUNDARY EFFECTS AND CONDUCTION MECHANISM STUDIES IN CHROMIUM METAL-INSULATOR-SILICON SOLAR CELLS ON POLYCRYSTALLINE SILICON*

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Summary

Chromium metal-insulator-silicon (MIS) solar cells fabricated on Wacker polycrystalline silicon and electron-beam-deposited thin film silicon were studied to determine current flow mechanisms. Wacker polycrystalline p-type silicon was shown to produce MIS solar cells which exhibit surface-state-controlled current for $T > 150$ K and tunneling-controlled current at lower temperatures. MIS cells on unpolished Wacker silicon are clearly space charge limited. Electron-beam-deposited polycrystalline silicon 20 - 30 μm thick has a conductivity which may be limited by the grain boundary trap density or the availability of free carriers. Surface state analysis, laser scan data and diffusion length studies also show the limitations which exist at grain boundaries of polycrystalline silicon.

1. Introduction

A study was conducted to evaluate the influence of grain boundaries on the performance of metal-insulator-silicon (MIS) solar cells using Wacker p-type polycrystalline silicon. The purpose of this work was to determine conduction mechanisms associated with grain boundaries, to evaluate the potential efficiency of MIS cells on polycrystalline silicon and to determine whether processing variations can reduce unwanted grain boundary effects. Large-area (2 cm^2) solar cells were made on the Wacker (Silso) polycrystal-

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line silicon substrates whereas smaller solar cells were made on the electron-beam-evaporated thin film silicon [1]. The typical structure of these solar cells was 700 Å SiO_x, 50 Å Cu, 30 Å Cr, 20 Å SiO_x, silicon substrate [2].

Previous data [2] for MIS cells on single-crystal silicon gave an open-circuit voltage V_{oc} of 0.62 V, a short-circuit current density J_{sc} of 28 mA cm⁻² and 12.5% efficiency η , which may be compared with 0.52 V, 24 mA cm⁻² and 8.8% efficiency using Wacker polycrystalline silicon. Current mechanism studies were designed to investigate the differences seen in the performance with different substrates.

2. Current mechanism study

Cr-MIS diodes were tested to determine current-voltage (I - V) behavior from 77 to 400 K. These data were then plotted to determine the model which fitted the temperature behavior best. Figure 1 shows a log I versus V plot for a chemically polished Wacker polycrystalline silicon MIS diode at several temperatures. An activation energy plot for this case is shown in Fig. 2 to satisfy the equation

Fig. 1. Variation of log I vs. V data with temperature for an MIS cell on polished Wacker polycrystalline silicon.

Fig. 2. Activation energy plot for an MIS cell on polished Wacker polycrystalline silicon.

$$J \propto T^2 \exp\left(\frac{\phi_B}{nkT}\right) \exp\left(\frac{qV}{nkT} - 1\right) \quad (1)$$

and gives $\phi_B/n = 0.48$ and $n = 2.1$, corresponding to $\phi_B = 1.01$ eV. This value of ϕ_B is comparable with the value of 1.055 eV obtained using the high frequency C^{-2} versus V plot. The graph of Fig. 3 indicates the presence of different conduction mechanisms in different temperature intervals. The high temperature region satisfies the equation [3, 4]

$$J_t^s = J_{03} \left(\psi_{bp} - \frac{\phi_A}{n} \right) \frac{\exp(\phi_A/nkT) - 1}{1 + (J_{03}/J_{04}) \exp(\phi_A/nkT)} \quad (2)$$

where

$$J_{03} = \sqrt{6\pi} A_{11}^* T^2 N_{ss} \sigma_{ss} \exp\left(-\frac{\phi_{bp}}{kT}\right)$$

$$J_{04} = qN_{ss}/\tau$$

$$\phi_A = qV + JA_T R_s + qV_{ox}$$

N_{ss} is the surface state density in equilibrium with the semiconductor surface, ϕ_{ss} is the capture cross section of surface states and other symbols are as commonly defined. This mechanism is indicative of a domination of surface state current for Cr-MIS cells on polycrystalline silicon. As long as the surface state current is limited by carrier capture rate and not by carrier emission rate eqn. (2) assumes a form similar to that of eqn. (1). Therefore it appears that these devices are operating by a mechanism in which surface states capture the carriers from the semiconductor bands and then the carriers are allowed to tunnel across the oxide barrier. The tunnel transmission coefficient is assumed to be unity since the tunneling time constant is less than the surface state recombination time constant.

At lower temperatures a different tunneling mechanism applies in which the carriers directly tunnel across the space charge region and the oxide barrier. The current density for this mechanism is given by [5]

Fig. 3. Plot of $kT \ln(A^* T^2/J_0)$ vs. temperature for an MIS cell on polished Wacker polycrystalline silicon.

$$J_t^h = A_h^* T^2 \left(1 + \frac{kT}{E_{00}}\right)^{-1} P_{ih} \frac{N_A}{N_V} \left\{ \exp\left(\frac{\phi_A}{nkT}\right) - 1 \right\} \quad (3)$$

where

$$E_{00} = \frac{\hbar q}{2\pi} \left(\frac{N_A}{\epsilon_s m_h^*} \right)^{1/2}$$

$$P_{ih} = \exp \left\{ - \frac{2(2m_i^*)^{1/2}}{\hbar} (X_h + \phi_{bp} - qV - \phi_d)^{1/2} t_{ox} \right\}$$

and ϕ_d is the doping potential. Our experimental data in Fig. 3 can be fitted for this mechanism using an oxide thickness t_{ox} of 15 Å when $N_A = 5.5 \times 10^{14} \text{ cm}^{-2}$ as obtained from $C-V$ analysis. Similar studies were also performed on unpolished Wacker polycrystalline silicon. These studies indicated a space-charge-limited conduction as defined by the equation $I \propto V^B$ with $B \approx 2.0$ at room temperature. Analysis of the experimental data indicates a gaussian-type shallow trap distribution. These traps are apparently associated with the rough surface. Since our polished samples did not show this kind of behavior it is obvious that the traps are easily removed by etching several microns of silicon.

A similar study was conducted using electron-beam-deposited silicon on an aluminum-coated titanium or stainless steel substrate [1]. The silicon films were 20 - 30 μm in thickness, were boron doped and had 500 - 1000 Å crystallites with a (110) preferred orientation. The grain size is presently limited by a combination of low substrate temperature, low vacuum and high deposition rate. Data for the variation of conductivity with temperature are shown in Fig. 4 and may be explained using the equation [6]

Fig. 4. Conductivity variation with temperature for electron-beam-deposited polycrystalline silicon films 20 - 30 μm thick : ○, NS68, silicon deposited with the titanium sublimation pump in operation; ▽, NS34, silicon deposited without the titanium pump.

$$J = \frac{1}{4} \bar{p} \bar{v} q \exp \left(- \frac{q \phi_B}{kT} \right) \left\{ \exp \left(\frac{q V_g}{kT} \right) - 1 \right\} \quad (4)$$

where $\bar{p}$ is the average hole concentration, $\bar{v} = (8kT/\pi m^*)^{1/2}$, ϕ_B is the grain boundary potential barrier and V_g is the voltage drop across the grain boundary. We assume the applied voltage to be distributed across many grain boundaries such that $V_g \ll kT/q$ which gives

$$\sigma = Lq^2 \bar{p} (2\pi m^* kT)^{1/2} \exp(-q\phi_B/kT) \quad (5)$$

where L is the crystallite size. This equation reduces to

$$\sigma \propto \exp(-\phi_d/kT) \quad \text{for } LN_A < Q_T \quad (6)$$

or

$$\sigma \propto T^{-1/2} \exp(-q\phi_B/kT) \quad \text{for } LN_A > Q_T \quad (7)$$

where Q_T is the grain boundary trap density. Thus sample NS34 deposited without using a titanium pump fits eqn. (6), which corresponds to a high trap density, giving $\phi_d = 0.38$ eV. Also, sample NS68 deposited while using a titanium sublimation pump may be analyzed using eqn. (7) for a lower trap density, giving $\phi_B = 0.091$ eV. Photovoltaic data are also much improved for MIS solar cells on electron-beam-deposited silicon if the titanium sublimation pump, which reduces the oxygen partial pressure, is used during the deposition. Oxygen has recently [7] been shown to inhibit grain growth in polycrystalline silicon and is thus detrimental to obtaining a large crystallite size.

3. Discussion

$I-V$ data taken from 77 to 400 K have revealed certain details concerning conduction mechanisms in polycrystalline silicon. Unpolished Wacker Silso substrates give MIS cells with space-charge-limited conduction. Similar studies on chemically polished Wacker Silso show that the surface state current dominates at higher temperatures and the tunneling of majority carriers dominates for $T < 150$ K. The grain boundary trap density is important in determining conduction processes in electron-beam-deposited silicon films 20 - 30 μm thick.

Surface state measurements have shown MIS cells on Wacker Silso to exhibit a midgap density N_{ss} of $7 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ compared with $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ for a single-crystal substrate. A comparison of $\log J$ versus V curves from dark current data and from a plot of $\log J_{sc}$ versus V_{oc} was also conducted using MIS cells on Wacker polycrystalline silicon. The illuminated curve gave an increase in ϕ_B from 0.78 to 0.81 eV and a decrease in n from 1.99 to 1.58 which indicates a filling of interface states during illumination. A laser scan study showed current loss to take place within one diffusion length of a grain boundary which is typically 40 μm for these Wacker polycrystalline silicon substrates.

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