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Silicon Film™ Photovoltaic Manufacturing Technology

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Introduction

Project Overview

The goal of AstroPower's PVMaT-2A project is to develop an advanced, low cost manufacturing process for a new utility scale flat plate module based on thin active layers of polycrystalline silicon on a low cost substrate. This is called the Silicon-Film™ process. This new power module is based on a new large solar cell that is 675 cm² in area. Eighteen of these solar cells form a 170 watt module. Twelve of these modules form a 2 kW array. The module, array and solar cells have the features shown in Table 1.

Table 1. Utility Scale Silicon-Film Product Features

Solar Cell Size	675	cm ²
Solar Cell Power	9.45	watts
Module Size	1.23	m ²
Module Power	170	watts
Array Power	2041	watts

The program has three components:

1. Development of a Silicon-Film™ wafer machine that is capable of manufacturing wafers that are 675 cm² in size with a total product cost reduction of 70%.
2. Development of an advanced solar cell manufacturing process that is capable of turning the Silicon-Film™ wafer into a 14% efficient solar cell.
3. Development of an advanced module design based on these large area, efficient silicon solar cells with an average power of 170 watts.

The completion of these three tasks will lead to a new power module which will be designed for utility and other power applications with a substantially lower cost. The module assembly labor cost is significantly reduced because only 18 solar cells are required for a 170 watt module in contrast to 36 solar cells for a 53 watt module.

Silicon Film Technology

The Silicon-Film™ Process is a method for fabricating solar cells by direct growth of a solar cell quality polycrystalline silicon layer on a low-cost, electrically conductive, supporting substrate. The Silicon-Film™ Process is designed to significantly reduce the silicon cost while retaining the physical and power output characteristics of single crystal silicon.

A drawing of a Silicon-Film™ solar cell is shown in Figure 1.

Figure 1. Silicon-Film™ solar cell.

Silicon cost is determined by silicon quality, wafer thickness, kerf loss during sawing and wafer breakage. With the Silicon-Film™ process, a dramatic reduction in silicon consumption and processing cost is achieved while maintaining solar energy conversion efficiencies as high as standard crystalline silicon wafers.

In the Silicon-Film™ process, cost reduction begins with designed-in limits on the consumption of costly high quality silicon. Additional reductions come from the elimination of most sawing steps, the use of thinner silicon layers, a lower cost supporting substrate, and the utilization of high yield continuous manufacturing technology. The continuous manufacturing process produces the volume to reduce the per wafer cost of capital equipment and labor while improving process control.

The photovoltaic effect in Silicon-Film™ grown on a low cost, coated steel substrate was first observed at AstroPower in August 1984 [1]. The energy conversion efficiencies of these micro-sized devices (less than one square millimeter) increased to 9.6%, without an antireflection coating, by October 1985 [2]. Larger area devices were plagued by shunts which were eventually attributed to stress caused by the thermal expansion differences between the steel and the silicon. The impact of this stress was reduced by adding a fairly thick ceramic coating to the steel which led to a 12 square millimeter, 9.6% solar cell as measured by SERI in November 1986 [3]. This thick ceramic coating led to the abandonment of steel in favor of a thermal expansion matched ceramic in January 1987. One square centimeter, 10.2% efficient solar cells were measured by Sandia in June 1987 [4]. Continued development of this approach led to the achievement of a 15.7% Silicon-Film™ solar cell measured by Sandia in December 1988 [5]. All of the above results were achieved with active silicon layers approximately 100 microns thick. Light trapping was not employed for these initial solar cells.

A series of commercial-size, 100 cm² solar cells was measured by Sandia in September 1989 with a median efficiency of 10% [6]. These results led to a focus on the development of the Pilot Scale manufacturing machine. This Pilot Scale machine was operated for eight months in a batch mode, while the data was collected and the design rules were developed for the first manufacturing machine. Present material has demonstrated efficiencies in excess of 10%.

Expected efficiency improvements are based on the product development and optimization approach utilized at AstroPower. Following are the key steps:

1. Develop a process that yields an acceptable and reproducible morphology. The key material quality test is minority carrier diffusion length.
2. Demonstrate 25 mA/cm² in a 0.1 cm² structure with a diffusion length greater than 20 microns.
3. Improve voltage and fill factor through emitter and base doping and contact optimization.
4. Improve current through diffusion length improvement using phosphorus gettering and hydrogen passivation[7].
5. Maximize performance with the addition of surface passivation and grid optimization.

PVMaT Project Goals

AstroPower is upgrading its facility to produce 1.22 m² Silicon-Film photovoltaic modules with an output of 170 Wp. At a production rate of 19 MW/year a 70% cost benefit would be realized from the current level. Areas of focus that will enable meeting these goals include process improvements in wafer formation, solar cell fabrication and module assembly. Specifically, AstroPower will accelerate improvement in production rate and material quality of Silicon-Film fabrication machines; accelerate improvements in solar cell efficiency from 11% to 14%; and utilize large area solar cells and modules to improve parts handling efficiency. These efforts will significantly reduce materials and labor costs. In addition, AstroPower will establish the capability for increased production capacity by increasing wafer machine production rates; automating solar cell processing to accommodate larger wafers; and automating circuit formation to reduce labor costs. AstroPower will also assure that the processes developed for scale-up will minimize the generation of waste streams and minimize environmental impact.

During the first yearly phase of the project, AstroPower is addressing improvements to a significant portion of its module manufacturing process. Areas of focus has included improving the productivity of the Silicon-Film machine. This effort began by establishing a baseline capability for the growth of Silicon-Film by optimizing present equipment. AstroPower also improved the solar cell performance of devices made from the Silicon-Film machine while decreasing the materials consumption of the cell processing portion of the manufacturing line. In addition, AstroPower plans to decrease module costs through the integration and mechanization of the fabrication process for cells and modules while scaling-up cell and module manufacturing equipment to handle larger sizes. Parts of the line to be automated include surface preparation, diffusion, PSG removal etch and contact printing. AstroPower will minimize the waste stream loads of the processes by initially evaluating the processes to assess the potential for waste reduction.

Key Results

Wafer Machine Performance Benchmarks

AstroPower has made substantial progress towards the first year goals of the project. The basic goal for the first phase of the project is to establish the baseline capability of producing Silicon-Film™ wafers at a rate of 400 kw/year on a single machine which are capable of being manufactured into 7.0 watt solar cells on a substrate area of 675 cm².

We have established much of the basis for achieving the first year's goals. The linear processing rate has been accomplished. The fabrication of wide wafers at the required linear processing rate shows the basis for meeting the large solar cell goal of the project. Table 1 shows the demonstrated benchmark process values for the wafer machine. These values have been simultaneously achieved in a single solar cell.

Table 1. Demonstrated Benchmarks Simultaneously Achieved

Milestone/Benchmark	Required	Demonstrated	Units
Baseline Process - Machine Rate	0.40	0.43	MW/year
Baseline Process - Solar Cell Output	1.10	0.97	watts
Baseline Process - Material Use Efficiency	75	71	%
Baseline Process - Solar Cell Size	15 x 45	10 x 10	cm x cm

From this table it is clear that the baseline process has substantially met the requirements for 10 cm x 10 cm wafers. Table 2 shows the key collateral benchmarks that have been achieved. These collateral values show the potential for the process to achieve the Phase 1 goals in the near term.

Table 2. Collateral Benchmarks Indicating Process Potential

Collateral Benchmarks	Demonstrated	Units
Upgraded Process - Machine Rate Capability	1.09	MW/year
Large Area Wafer Capability	275 cm x 16 cm	planks
Large Area Wafer Capability	2@ 275 cm x 11 cm	planks
Large Area Wafer Capability	15 cm x 45 cm	wafers
Large Area Solar Cell Capability	15 cm x 45 cm	cells

The present SF-2 machine rate for the baseline process is equivalent to 0.43 MW/yr, which meets the target for the first year of the project. An important machine efficiency was gained by employing two 11.5 cm wide sheets on one setter. The effective growth width is 23 cm.

Material usage efficiency has also been improved by increases in sheet growth length and width. The sustainable benchmark for material usage efficiency is 71%, which is 4 points less than the goal of 75%. The best single material usage efficiency for a single run was 74%.

A set of 15 cm x 45 cm Silicon-Film™ wafers were fabricated from 16 cm x 275 cm planks. These wafers

were fabricated into solar cells using a modified baseline process. Figure 2 is a photograph of 15 cm by 45 cm Silicon-Film™ wafers.

Figure 2. 10 cm x 45 cm Silicon-Film™ wafers

Solar Cell Results

Some encouraging progress has been made, but we are still short of our 1.1 watt solar cell goal. We have delivered to NREL a 0.97 watt solar cell on a nominal 100 cm² area. Figure 4 shows the voltage-current characteristic for this solar cell. Recent device characterization has indicated that, with the exception of one parameter, minority carrier diffusion length, the solar cell characteristics of current Silicon-Film material are excellent. As part of this project, the limiting factors of minority carrier diffusion length for the process have been identified.

Figure 3. 0.97 watt 10 cm x 10 cm Silicon-Film™ solar cell

Figure 4. 15 cm x 45 cm Silicon-Film™ solar cells

Wafer Manufacturing Process Research

Process Capability

The goals of this task are to optimize the wafer fabrication process at high rates, determine and fix input material specifications, develop an in-line substrate and film application method and fabricate large wafers.

Wafer Machine Development and Performance

Construction was completed on the next generation Silicon-Film™ machine (SF-3). This machine incorporates significant improvements in the active layer growth furnace design, and in gas handling. These improvements enabled the achievement of linear process speeds up to two times greater than the previous generation Silicon-Film™ machine (SF-2).

At initial start-up of SF-3, the process yield was less than 50%. Two sources for the low yield were identified: dislocation density and active species in the gas ambient. Compared to SF-2 generated wafers, SF-3 wafers initially had a higher dislocation density in the active silicon layer. The technical reason for the difference was identified and related to differences in the thermal profiles of the process. The dislocation density in SF-3 is now the same as in SF-2.

In collaboration with The Dow Chemical Company, an in-situ quadrupole mass spectrometer was used to analyze the chemical composition of the argon atmospheres in SF-2 and SF-3. In general, the argon was found to be quite clean. Only expected gases were seen: H_2O , O_2 , N_2 , CO_2 , H_2 (CO could not be resolved from N_2). O_2 and N_2 were about at the detection limits. Trace amounts of CO_2 and CO are expected. Thermo-gravimetric analysis with mass spectrometry, TGA-MS, of some of the wafer and setter materials showed that desorption of CO_2 from these materials could account for most of the observed CO_2 . H_2 is an expected by-product from H_2O oxidation of Si. It was seen in SF-3, but not in SF-2. There is some evidence that gases can concentrate in the argon recycle stream (e.g. CO_2 , H_2). We are planning to add an on-line gas chromatograph. This would be able to monitor all of the gas species detected.

Process Length and Width

An important step in improving process continuity and yield was made when the Silicon-Film sheet length was increased by a factor of six. Improvements in setter preparation and transport were critical to this success. An additional machine efficiency was gained by employing two 11.5 cm wide sheets on one setter. The effective growth width is 23 cm, which produces two 10 cm wide wafers.

These two improvements increased the machine usage efficiency, machine process rate and material usage efficiency. Further gains can be made by employing wider sheets. For example, sheets 31 cm wide for fabrication into two 15.0 cm wafers would provide significant gains in material usage efficiency by limiting wafer cutting losses.

Large Area Wafers

The first 15 cm x 45 cm Silicon-Film™ wafers were fabricated in April. Fabrication of the wafers went smoothly, and the quality of the wafers generated was much higher than expected. Since our existing sawing equipment for wafer sizing was not adequate for these large area wafers, the wafers were sized by

hand scribing. The wafers were processed into solar cells by the solar cell processing team as described in the later section on solar cell fabrication.

Silicon Feedstock and Material Preparation

An investigation of an alternative source of solar-grade silicon led to the discovery of a process which consistently produces large, columnar grain wafers at high process speeds. Initial device results have been very encouraging. The new process material shows higher lot averages for Voc and Isc when compared to the other source of solar grade silicon. Maximum Voc and Isc have not yet been shown to be higher than the standard source.

Silicon material processing yields have been significantly increased by improvements in the material preparation process. Sources for contamination of incoming material have been identified and are being addressed.

Defects

An area of major focus has been characterization and reduction of dislocation density in the active layer. We are developing techniques for etch delineation of crystal dislocations and etch pit counting. A chemical polish procedure has been developed which allows us to defect etch the as-grown wafer surface. We have also developed a procedure to defect etch in cross-section, and to defect etch small area mesa devices. Figure 5 shows the defects developed on mesa and off mesa on a Silicon-Film™ device.

Figure 5. On mesa/off mesa defect density, Area = 0.1 cm²

Minority carrier diffusion length on the mesa devices, measured by spectral response, has been roughly

EPD measured in cross-section, on-mesa, and off-mesa. Our goal is develop an EPD measurement technique which can reliably predict the minority carrier diffusion length of as-growth Silicon-Film wafers. We are also developing an image processing system which will be used to automate EPD counting.

Despite the progress in using EPD as a tool, we are still having difficulty correlating etch pit density (EPD) of intentionally defected control samples to minority carrier diffusion length, as measured by a spectral response technique on mesa devices. We have resolved discrepancies between EPD measured in cross-section, on-mesa, and off-mesa. A thorough examination of our spectral response hardware and technique for determining minority carrier diffusion length (L_n) has led to several significant improvements and modifications. However, the correlation between EPD and L_n is still very weak and noisy. We are currently investigating possible mechanisms for non-uniform defect delineation by the defect etch (Secco etch), as well as other possible cofactors for reduction of L_n , such as contamination by impurities. We are also investigating improved EPD counting and averaging procedures.

A new short-loop mesa process has been correlated to 100 cm² device results. The mesa process has been effective for rapid comparison of solar cell device results to defect density. We have also established a procedure to track relatively large engineering split lots of 100 cm² wafers through solar cell processing, to allow for more statistically significant evaluations of process improvements.

Impurities

One important cause for limiting the diffusion length, L_n , of the active layer may be the presence of impurities. Impurities may be brought in with the silicon feedstock, or incorporated during material preparation, or added during the growth process in the wafer machine. We have begun a comprehensive program to ascertain concentration levels of impurities at various stages in the process. In collaboration with The Dow Chemical Company, we performed a detailed chemical impurity analysis of the Silicon-Film process. Evidence for impurities was found at several points in the process sequence. Some impurities appear to be coming in with the current supply of silicon, although additional lot sampling is needed to confirm this conclusion. Some impurities are added in the material preparation process. These impurities correlate well with expected contaminants. However, they are expected to cause minimal photovoltaic degradation. Additional analytical testing is planned to further investigate the size of the potential problem arising from impurities for our material. The analytical test data will be correlated with detailed measurements of spectral response.

Process Characterization and Measurement Techniques

Thermal Profiles

The focus of our defect density reduction effort is on profiling the Silicon-Film growth and anneal process. Our data and much of the literature shows that the thermal history of the active material plays a major role in controlling defect formation. Considerable progress was made in characterizing the thermal profiles in the Silicon-Film growth path. Several performance enhancing modifications have already been implemented. We expect that characterizing and optimizing the thermal profile will be an area of focus for the next several months.

By adjusting process parameters, we have been able to change the temperature profiles somewhat predictably, but we have not yet been able to optimize the profiles. Interpretation of the data collected is also non-trivial. We are currently working on a first-order thermal model to estimate the actual wafer surface temperature based on the thermal profile data for the setter.

A major heater modification for the anneal chamber of the SF-3 machine was designed, built, and installed in June and tested in July. Although not yet optimal, the heater has had a significant positive impact on the measured thermal profile. The heater has proven to be very reliable in operation. Some fine tuning and minor modifications of the heater are planned to attempt to further improve its performance.

Based on the success of the high temperature post-heater, a custom high temperature pre-heater based on similar technology was designed, built, and installed on the SF-3 machine in July. We plan to start-up and test this pre-heater in August.

Wafer Quality Characterization

We are investigating alternative methods for characterization and routine monitoring of minority carrier lifetime in Silicon-Film™ wafers. Possible methods include: SPV, laser scanning, and microwave reflection decay. Minority carrier diffusion length is currently extracted from spectral response measurements. We have begun development of a circular polariscope to monitor residual stress in Silicon-Film wafers. A simple LBIC system is also under development in order to gain another measurement of wafer quality.

Statistical Process Control

The goal of this task is to provide process control information to the wafer process improvement task to direct wafer process development work. The process control information is being collected and analyzed using the statistical process control methodology, SPC.

Methods for measuring key active layer parameters were developed and daily data collection instituted. Three key variables were chosen. Two variables were related to incoming wafer material parameters. These variables depend on proprietary aspects of the wafer fabrication process. The third variable chosen was wafer mass. Two parameters: input power and inert gas flow rate have been brought under complete closed loop computer control.

Data was collected for the first incoming material parameter for 22 lots, and Xbar and R control charts were generated. Although variation from the mean value was small ($\pm 2\%$), the control charts were slightly out-of-control, indicating there is some non-random variation in material preparation or in incoming raw material. This non-random variation is being investigated.

Control charts for the second key parameter of starting material have also been found to be out of control. Causes for the non-random process variation have been identified and have been addressed.

A sampling procedure was developed for wafer weight. Xbar and R control charts were generated. Although wafer weight is in statistical process control, indicating that the process variation is random, the process is not yet capable of meeting the process specification at 100% yield, i.e. $C_p < 1$. Figure 6 shows a typical Xbar control chart for wafer weight. The control charts for wafer weight are being implemented as SPC monitors.

Figure 6. Xbar chart for wafer weight showing in-control process parameter

We plan to review other remaining process variables for inclusion in data base development and incorporation into the on-line SPC methods during the next three months.

Solar Cell Efficiency Improvement and Process Development

The goal of this task is to identify and implement processes to improve solar cell efficiency. Area of focus include diffusion, fine line metallization, in-line hydrogenation and AR coating and gettering. The efficiency goal for this task is an 11% Silicon-Film™ solar cell process.

Baseline Solar Cell Process Sequence

Work focused on refining the baseline process sequence. We conducted a series of experiments to optimize the firing time and temperature for the emitter junction. These experiments were combined with diffusion experiments targeted at increased blue response for the final diffusion step. A low cost all aluminum back contact process was prototyped and evaluated.

Four process sequence variations which compared the standard process diffusion to a 'gettering' diffusion were conducted. The objective was to determine the influence of surface treatment and sequence of processes on obtaining optimal electrical properties and electrical contact integrity. Comparison of the measured parameters of electrical performance and mechanical yield for the four process sequences showed one of the sequences to be superior, shown below in Table 4.

Table 4. Baseline Solar Cell Process Sequence

	Process Step
1)	Surface Preparation
2)	Gettering Diffusion
3)	Etch Gettered Junction
4)	Standard Shallow Junction Diffusion
5)	PSG Removal
6)	Print/Dry Back Contact
7)	Print/Fire Front Contact
8)	H+ Passivation
9)	AR Coating
10)	Contact Burnishing
11)	Test

Initial results indicate an increase in J_{sc} of approximately 1 mA/cm² compared to the standard production diffusion schedule. Optimization of the diffusion and the surface etch process that the deep diffusion gettering step requires was carried out. Further evaluation of the back contact process is being carried out.

Process Development Research

Gettering

Improvements described in the baseline process including the gettering process were achieved in diffusion and etch. The original process in January required an HF etch of the top cell surface after the front contact was fired on. Poor front contact adhesion was a result of etch process variability. The process was modified to gain improvements in contact adhesion as well as in blue response. Instead of etching the

gettering diffusion back to the resistivity for the final n+/p junction, the layer is almost entirely removed. A second diffusion is added to provide a new junction with proper resistivity. As a result of this change the final etch step was eliminated which improved contact integrity.

Hydrogen Passivation

A hot wall PECVD tube reactor for hydrogenation and Si_3N_4 deposition was brought on-line for production as well as for process improvement studies. The goal of the process studies was to characterize the hydrogenation and AR coating processes to be able to specify an in-line process which combines these two steps in a sequence. RF power, wafer temperature, gas flows and process time were varied to determine the minimum time necessary for acceptable solar cell performance.,

A full-factorial experimental design exploring hydrogenation times and RF power levels was developed using the ECHIP™ software. The purpose of this experiment was to find optimum system conditions (to maximize percentage gain, and minimize process time) for Product I wafers, and to begin defining the conditions for in-line processing.

The first experiments were conducted to determine the range of hydrogenation time and RF power levels. Twenty-five Product I wafers from the standard process sequence were included for each trial in the experimental design. The percentage gains in open-circuit voltage and maximum power were used as response variables.

The data were analyzed using a factorial model by the ECHIP software. Figures 8a and 7b show the performance output contour maps as a function of process variables. The parameters determined for the model indicate that process time has the most significant effect on both Voc and Pmax, with RF power having a slight effect. For process development purposes, the contour plots confirm that the "standard" process yields acceptable electrical performance improvement.

Figure 7. Contour Plots of Percentage Changes in Voc and Pmax, For Hydrogenation Times (minutes) and RF Power, (percentage of Maximum).

Si₃N₄ AR Coating Process

Screening experiments using mechanical substrates were conducted exploring RF power and deposition time effects on process uniformity. The deposition rate was observed to be linear with respect to RF power; i.e., for a 2x increase in RF power, the time needed to deposit an AR coating was cut by half. No significant change in uniformity either on-boat or on-wafer was evident.

Combined PECVD Processes: Hydrogenation and AR Coating

An important saving in process cost will be obtained as the result of combining the H⁺ passivation step and the Si₃N₄ AR coating step into one operation sequence rather than in two separate steps requiring separate vacuum entry/exit pump/purge cycles..

A "tracking lot" system was implemented to characterize statistically the results from hydrogenation and AR coating depositions. The first tracking lot consisted of seventy work-in-progress wafers fabricated using the previous solar cell process. The results from the tracking lot indicated that the average performance gains through the H⁺/AR sequence were nearly 100%. The overall mechanical/electrical yield of solar cells to module fabrication from the CVD processes was established as greater than 95% (67/70 passing).

Two other tracking lots were established with solar cells fabricated from the streamlined process sequence. The performance gain from hydrogenation for these other lots was significantly reduced as compared to Tracking Lot 1. Verification of the integrity of the production line CVD system was performed by reprocessing through the laboratory CVD system, with no significant change in device performance evident. Work is currently underway to establish the electrical characteristics of Product I solar cells fabricated using the streamlined process sequence, and determine the nature of the loss mechanisms.

A full-factorial experimental design exploring hydrogenation time and RF power for the combination H+/AR process was conducted. The experimental space was determined by the results of initial screening experiments, which indicated that hydrogenation times below 30 minutes were sufficient to demonstrate acceptable performance. Although the design has not been completed, there has been some indication that significantly shorter hydrogenation times may be possible with the combined process.

The initial trials for the combined H+/AR process exhibited an anomalous deposition pattern, consisting of a discoloration around the bus bars. This pattern is not encountered in the normal sequence where the process vacuum is broken between the hydrogenation and AR deposition steps. This anomalous deposition (termed the "butterfly" pattern) is also seen when an AR coating run is terminated and subsequently restarted *in vacuo*.

An experiment was conducted to determine whether the "butterfly" pattern seen after H+/AR runs is related to unpassivated silver metallization. Wafers which received a 150 Angstrom PECVD SiO_x layer (applied in a separate laboratory process) were H+/AR processed along with representatives of the current process sequence, and bare silicon witness samples. The SiO_x coated wafers and the bare silicon samples exhibited no anomalous deposition, while the wafers from the current Silicon-Film process sequence showed the "butterfly" deposition pattern. This result is consistent with the hypothesis that ammonia gas is reacting with unpassivated Ag metallization to generate some deposition-inhibiting compound, although it is not conclusive evidence of the hypothesis. It is anticipated that the implementation of the CVD SiO_x process before AR will eliminate the anomalous deposition by chemically passivating the Ag surface with the thin oxide layer.

Solar Cell Characterization

Quantum efficiency measurements of Silicon-Film™ solar cells have been performed, demonstrating blue response typical of standard production solar cells. Improvement of blue quantum efficiency to a level seen in high-performance solar cells is considered to be an area for improvement needed to achieve project performance goals.

The solar cell modeling program, PC-1D, has been employed to model and characterize both the optical properties of the Si₃N₄/SiO_x over Si coatings, and the electrical properties of the high-performance junction. PC-1D results suggest that with a high-quality junction and a thin (less than 200 Angstroms) oxide layer, the internal quantum efficiency at 400 nm will be near 95%, with a minimal change in global reflection as compared to a Si₃N₄ AR directly over Si.

Improvements in junction quality (as measured by quantum efficiency and solar cell current-voltage measurements), and modifications to the production line CVD system to deposit SiO_x will continue in July. PC-1D modeling along with reflectance measurement techniques will be used to optimize the deposition characteristics of the SiO_x and Si₃N₄ layers to maximize short-circuit current. Inclusion of the H+/SiO_x/Si₃N₄ CVD process into the fabrication sequence is planned.

Device Equipment/Process Improvements

The goal of this task is to increase the level of automation in the solar cell fabrication process to handle 15 cm x 45 cm substrates. The approach has been to run prototype lots of large solar cells through the current line on a pilot basis to determine the specific automation process issues. The experience gained is being

used to specify the automation design rules for surface preparation, diffusion, PSG removal, contact printing and solar cell testing.

Fabrication of 15 cm x 45 cm Solar Cells

The development of larger solar cell processing capability is being carried out in two steps. The first step is the fabrication of the largest possible solar cells using the present equipment set. The second step is the addition of prototype or bench scale equipment at certain steps to accommodate solar cells at least as large as 15 cm x 45 cm.

Smooth, mechanically strong wafers, 15 x 45 cm, were fabricated in a Silicon-Film™ production machine. Little modification from present tooling was required. The wafers met the flatness specification of the 10 cm x 10 cm wafers normally produced. Large solar cells were successfully fabricated from these wafers using a modified process sequence. The solar cell fabrication process tools were identical to standard 10 cm x 10 cm production tools for all processes except for printing and AR coating. A hand operated screen print station for printing the front pattern was employed to print the contacts. The contact pattern screen was identical to the one which will be employed in the automatic printer to be developed later in the program. Print resolution and quality met the requirements for present product. A metal oxide AR coating was applied at a hand operated coating station employing a process used on the single crystal silicon solar cell production line.

The solar cells produced were mechanically strong and readily able to survive four high temperature processes: standard diffusion, back contact firing, front contact firing and spray pyrolysis AR coating.

The gettering and H⁺ passivation steps were not employed in this initial effort. The present polysilicon active layer material requires both the use of gettering and the use of the H⁺ and Si₃N₄ AR coating process steps to obtain acceptable currents and fill factor. These steps, in the proper combined sequence, produce significant passivation of defects in the bulk and at surfaces as well as efficient optical coupling of the incident radiation as described previously. The simpler metal oxide CVD process was employed because the process tooling could readily accommodate the large solar cell.

The results of this task to this point have established the ability to process large wafers into completed solar cells with a minimum of difficulty. The issues for automation of the processes for large solar cells appear to be reduced to mechanization of current, known processes.

Waste Impact/Cost Minimization

The goal of this task is to reduce the amount of hazardous materials used and waste materials generated by the solar cell fabrication processes. The approach is first to measure the materials used and generated by the processes and second to assess the opportunities for reduction or elimination.

The present process for neutralization of the waste stream from the front end surface preparation step was evaluated for improvement in operation efficiency. A process audit was carried out for the baseline Product I process to determine its waste load. There are two primary streams of interest: the water effluent stream from the various wafer etch and cleaning processes and the silver paste clean-up stream from cleaning printing screens. A third stream is the air exhausts from the furnace and CVD processes, which are relatively minor.

A number of changes have been made in the baseline process for solar cell fabrication since the beginning of the project. One of the important changes has been the elimination of an aluminum back etch step which generated a hydrochloric acid/aluminum oxide waste stream.

The solar cell fabrication process has been subject to some significant changes. As a result, a detailed analysis of the waste impact and cost minimization has been delayed. The plan is to pursue a detailed analysis in August and September when most of the base-line processes will be fixed for the balance of the first year's effort.

Advanced Module and Panel Design

The goal of this task is to evaluate alternatives for solar cell, module and panel designs and then to prototype the solar cell and module designs. The result of successful completion of this task will be specifications and designs which will minimize cost of manufacture and optimize product performance. The focus of this task is to implement designs which employ large solar cells in large modules. The target baseline module design is to employ 18 solar cells of dimension 15 cm x 45 cm in a 2 x 9 series arrangement. Another important objective is to match solar cell and module manufacturing process techniques to assure a high performance, high reliability product.

Module Assembly and Process Development

Work started on establishing a module fabrication process development and test capability. The baseline process sequence was determined. Materials required for fabricating modules from Product I solar cells were ordered. A module assembly process development line was established. The primary goals are to evaluate alternative assembly processes, establish process yields for module manufacture using Product I solar cells and fabricate prototype modules.

Front and Back Contact Interconnection Process Development

During the course of the project several variations in the solar cell process sequence have been assessed. These variations have had significant impact on process development for module assembly.

A new base-line process was established in February for solar cell fabrication which incorporated an etch step after the gettering diffusion process. Solar cells produced by the base-line process were used in assembling modules to evaluate issues in module manufacture, particularly at the front contact process. As expected, contact pull strengths for the front contact were found to increase by the use of a gettering etch after the gettering diffusion step. The solar cell performance and contact pull strength were optimized by varying the contact firing conditions. High pull strength bonds to the front contact have been consistently achieved.

A new all aluminum, screen printed back contact process was developed which offers significant potential for cost reduction, while improving the solar cell electrical output. It has been our intent for some time to replace the all silver back contact with a modified back contact which would reduce or eliminate the use of silver. The back contact under development eliminates the use of silver which is expensive and which generates a minor waste stream of silver particles. Work in the advanced module development focused on developing a technique for bonding the solder coated ribbon interconnect to the solar cell back contact. Three basic techniques are being investigated for the interconnect bonding process: use of conductive adhesives, direct solder attachment, and welding.

So far, conductive adhesives have not proven capable of meeting the performance requirements. An interim process for direct solder attachment has been found and implemented. It requires an additional process step and appears to cause a 2-5% reduction in solar cell output. A cost/performance comparison is being conducted with an alternative process. This process employs the printing of two silver stripes for the solderable contact and the overprinting of an aluminum back plane. A review of welding process options has been made and a process development welding station is being specified.

Solar Cell and Module Design

The contact pattern employed for the 15 cm x 45 cm solar cell was based on the same pattern employed in the standard 10 cm x 10 cm Silicon-Film™ solar cell: 0.15 cm spacing between grid lines and 5 cm spacing between bus-bars. These parameters result in a 9 bus-bar pattern with 46 grid lines, yielding a shading loss of 10.5%. A detailed analysis of the front contact design was conducted to determine an optimal pattern. A better design was produced using present values for printing parameters and electrical characteristics. This design employs 7 bus-bars and 36 grid lines, yielding a shading loss of 8.9%. This result is important because it helps determine the complexity of the tabbing and stringing operation. Clearly, the fewer the bus-bars the fewer front to back interconnect ribbons. Later designs for large solar cells will incorporate these results as well as results based on improving the grid line printing process.

Design and Prototyping of Large Modules

The baseline process was reviewed to determine the steps requiring modification to accommodate 15 cm x 45 cm solar cells. A preliminary solar cell and module design for 15 cm x 45 cm solar cells in 18 cell modules was completed.

Several of the large solar cells produced during April were tabbed and laminated to assess the mechanical robustness of the solar cells. Plastic sub-module laminates were fabricated with no problems.

Specifications were developed for the procurement of a laminator capable of laminating large area modules, employing large area solar cells. The proposed design will accommodate a module size of up to 1.05 m by 1.35 m, or 1.42 m². This will meet the requirements for the module delivery at the end of the first phase of the project. The laminator will be fabricated by AstroPower Canada, using separate funding.

Conclusions

AstroPower has made significant progress in carrying out the first phase of the project. Key demonstrations to this point are:

- demonstration of 0.48 MW/year operating rate for Silicon-Film machine in fabrication of 100 cm² wafers,
- fabrication of a 0.97 watt Silicon-Film solar cell on a 100 cm² substrate,
- fabrication of 675 cm² wafers,
- fabrication of solar cells from 675 cm² wafers.

A number of technical issues have been identified which are important for improvement of Silicon-Film solar cell efficiency. Short circuit current density is limited by the diffusion length. Diffusion lengths for present wafer material is in the range of 10-20 micron. Improvements of the diffusion length appear to be controlled by three factors: density of dislocation defects in the material, impurities, and residual stress. Work up to this point has prepared us for evaluating the relative importance of these factors during the next period of the project.

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Abstract

This semi-annual report describes Astropower's progress in the improvement of its Silicon-Film manufacturing technology by increasing the rate and material use efficiency of its wafer machine, fabricating large area wafers, and converting them into large area solar cells. The increase in operating rate and fabrication of large area solar cells, while preserving solar cell efficiency will significantly reduce cost. The meeting of three key goals for manufacturing improvement are described. A machine operating rate of 0.43 MW/year has been demonstrated; a 0.97 watt 100 cm² solar cell was fabricated; and large area solar cells of 675 cm² were fabricated.

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