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SILICON SHEET WITH MOLECULAR BEAM EPITAXY FOR HIGH
EFFICIENCY SOLAR CELLS

Final Technical Report for the Period March 22, 1982—April 30, 1984

By
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SILICON SHEET WITH MOLECULAR BEAM EPITAXY
FOR HIGH EFFICIENCY SOLAR CELLS

Final Technical Report for period 3/22/82 - 4/30/84

by

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Pasadena, California
Contract No. 956233

MASTER

The JPL Flat Plate Solar Array Project is sponsored by the U. S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort towards the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology by agreement between NASA and DOE.

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Fig. 32. Efficiency as a Function of width of front p-layer. Cells had $\rho(\text{front}) = 0.1 \Omega\text{-cm}$, $\rho(\text{back}) = 1 \Omega\text{-cm}$, $SN1 = SP2 = 5 \times 10^6 \text{cm}^2/\text{s}$ and $SP1 = SN2 = 0$.

Fig. 33 Short Circuit Current and Open Circuit Voltage as a Function of Width of Front p-layer for Cells in Figure 32.

ABSTRACT

A two-year program has been carried out for the Jet Propulsion Laboratory in which the UCLA silicon MBE facility has been used to attempt to grow silicon solar cells of high efficiency. MBE offers the potential of growing complex and arbitrary doping profiles with 10 Å depth resolution. It is the only technique that can readily grow built-in front and back surface fields of any desired depth and value in silicon solar cells, or the more complicated profiles needed for a double junction cascade cell, all in silicon, connected in series by a tunnel junction. Although the dopant control required for such structures has been demonstrated in silicon by UCLA, crystal quality at the p-n junctions is still too poor to allow the other advantages to be exploited. Results from other laboratories indicate that this problem will soon be overcome. A computer analysis of the double cascade all in silicon shows that efficiencies can be raised over that of any single silicon cell by 1 or 2%, and that open circuit voltage of almost twice that of a single cell should be possible.

FINAL TECHNICAL REPORT

"Silicon Sheet with MBE for High Efficiency Solar Cells"

I. Introduction - Objectives and Performance of Two-Year Program

The goal of this program was to apply the capabilities of the new technique of Molecular Beam Epitaxy (MBE) to the growth of high efficiency silicon solar cells. Because MBE can provide well-controlled doping profiles of any desired arbitrary design, including doping profiles of such complexity as built-in surface fields or cascade junction cells, it appears to be an ideal method for development of high efficiency solar cells..

For the first year it was proposed that UCLA grow and characterize silicon films and p-n junctions by MBE to find whether the high crystal quality needed for solar cells could be achieved. It was found that the initial cleaning step of heating the silicon substrate to 1200°C for one to two minutes, in high vacuum, did not degrade the good quality of substrates used. Diffusion lengths, as measured by JPL, remained at their initial values near 100 microns. However, p-n junctions then grown by MBE at UCLA had very poor reverse leakage characteristics. When one of these was made into a solar cell at JPL, its performance was very poor with an efficiency of 2.8%, compared to diffused cells made at JPL using the same substrate material, which had efficiencies of 6.7%. (These cells suffered degradation during processing at JPL.)

The grant was then extended for a second year with three objectives - to find the source of degradation in the MBE grown junctions and to grow good single silicon cells; to grow a tunnel junction and a double cascade silicon cell to demonstrate very large open circuit voltage; and to run calculations on double cascade silicon cells to predict optimum profiles and predict the resulting performance.

Of these objectives, only the last has been achieved. As for the first, many junctions were grown by MBE and tested, and several were fabricated into solar cells by JPL. All junctions grown had poor reverse leakage characteristics, though their quality improved over the year. Two solar cells were fabricated by JPL from MBE-grown junctions with efficiencies of 4.70 and 4.79% efficiencies still very poor, but much better than the first MBE cells grown the previous year.

The reasons for these problems at UCLA are still not known. It is known that MBE-grown junctions of silicon in two other laboratories - one at Bell Laboratories, and one at AEG Telefunken in Germany, have demonstrated nearly ideal reverse characteristics and lifetimes as high as 100 microseconds.

During the two years, much has been learned about the quality of the MBE-grown material from mobility, SIMS and spreading resistance measurements. A new technique for growing and doping the films by solid phase epitaxial regrowth has proven very successful. The extraordinary doping control potential of MBE in various arbitrary profiles has been confirmed, and certain majority carrier devices using the triangular barrier diode configuration have been grown successfully for the first time in silicon.

As for the second objective, one tunnel junction was grown by MBE of p^+ on n^+ material. The expected doping density in the film was $1 \times 10^{19} \text{ Ga cm}^{-3}$, and the substrate was n-type with $N_D = 2 \times 10^{18} \text{ cm}^{-3}$.

As for the last objective the calculations on the cascade cells show promise of achieving efficiencies of 1 or 2% higher than the best single silicon cells and with an open circuit voltage of almost twice that of good single cells.

The following report describes our technical activities, results and problems in detail, and concludes with recommendations for future effort.

II. Silicon Molecular Beam Epitaxy

A. Background

Molecular beam epitaxy of silicon, despite an earlier beginning, (1966 vs. 1969)^(1,2) has lagged far behind that of GaAs. The first serious attempts to demonstrate it as a new device growth technique start with Russian papers in 1971⁽³⁾ and 1975⁽⁴⁾ and a Japanese paper in 1976⁽⁵⁾. The first use of MBE to grow a silicon device was reported by Ota at Bell labs in 1976⁽⁶⁾, and the first well-controlled experiments on doping and crystal quality began with Becker and Bean, at Bell Labs in 1977⁽⁷⁾.

Since 1977 the number of workers in the field has grown gradually, with the principal results coming from the groups at Bell Laboratories and UCLA, several Japanese groups^(8,9,10) and Kasper's group at AEG Telefunken in Germany. The UCLA group since 1981 has been studying the incorporation of the two principal evaporative dopants - Ga (p-type) and Sb (n-type),^(11,12,13) and has recently pioneered the solid phase low temperature epitaxial regrowth method⁽¹⁴⁾ as a simple and effective means of fine dopant control. The two Bell Laboratories groups have adopted the ion imbedding method of doping during normal (high temperature) MBE growth^(15,16). The Japanese groups have used both evaporative doping and a kind of ion imbedding with a plasma but without a focussed ion beam.⁽¹⁷⁾

Recently, results presented by Bean⁽¹⁸⁾ and by Kasper⁽¹⁹⁾ document crystal quality sufficiently high for the most demanding devices, including solar cells. Thus Bean reports lifetimes in his MBE grown films of up to 100 μ secs, and trapping levels, by DLTS, below the noise level. Kasper is successfully growing, by MBE, high frequency Impatt diodes and epitaxial portions of a silicon integrated circuit that is now in production at Telefunken with an 80% yield.

Both Bean and Kasper have shown that extreme control of all background impurities in the high vacuum chamber during growth is essential for this high quality, and that achieving it comes only after many repeated runs in any station.

The very superior control of sharp dopant profiles of arbitrary shape afforded by MBE in silicon is now well documented. The UCLA group has shown how, by a build-up and flash-off technique, one can produce extremely sharp doping transitions using evaporative doping of Ga and Sb during normal MBE growth at $\sim 700^{\circ}\text{C}$ (See Fig. 1). This technique is being used by Kasper to grow Impatt diodes. We have also demonstrated 50 $\text{\AA}$ doping layers in the new solid phase epitaxial regrowth method in the first silicon triangular barrier silicon diodes⁽²⁰⁾.

Fig. 1 TUNNET STRUCTURE GROWN BY M.B.E. IN SILICON
AT UCLA

II. B. Silicon MBE Growth and Doping

We discuss here the parameters of the two MBE growth procedures now being used at UCLA: normal MBE growth at $\sim 700^\circ\text{C}$, and solid phase epitaxial regrowth at $\sim 575^\circ\text{C}$. In each case we dope only by evaporation of Ga(p) and Sb(n) from boron nitride crucibles during growth. Silicon growth rates are at 1 to 3 Å per second.

1. Normal MBE Growth at $\sim 700^\circ\text{C}$.

This is the conventional approach in which the substrate is hot enough to permit each arriving silicon atom to diffuse into an epitaxial site of the lattice before the next arrives. While this process can occur at temperatures as low as 450°C , crystal quality and evaporative dopant transients can be better controlled at 700°C and above. The higher the temperatures and the faster the silicon growth rate, the lower the contamination due to adsorption of CO_2 , H_2O and O_2 molecules from the high vacuum. At growth pressures of 10^{-9} Torr, the maximum contamination of the grown silicon film, if all incident atoms stick to the surface, is $\sim 10^{19} \text{ cm}^{-3}$, for a growth rate of $\sim 3 \text{ Å/sec}$. Actually sticking coefficients are much less than unity on clean silicon at elevated temperatures so that O_2 and C levels in grown MBE films should be $< 10^{18} \text{ cm}^{-3}$. At such levels they should be electrically inactive, though O_2 may precipitate into clusters if the crystal is held at $\sim 700^\circ\text{C}$ for many hours. These give rise to localized stress and dislocations, as shown by etching studies of denuded zone crystals. (21)

Evaporative doping by Ga and Sb during normal MBE growth suffers from three disadvantages: 1) the sticking coefficient is extremely low and temperature sensitive; 2) the maximum dopant concentration seems to be limited to $< 10^{19} \text{ cm}^{-3}$; and 3) both Ga and Sb have long residence times, τ , on the silicon surface. Sudden changes in profile cannot be made more abruptly than τ , causing severe smearing of profiles. This limitation can be eased by going to temperatures above 750°C to shorten τ , or by using the "build-up" and "flash-off" technique developed at UCLA⁽¹¹⁾.

Mobilities measured at UCLA for both Ga and Sb doping of normally grown MBE silicon have matched bulk values except at the highest doping levels reached of $> 10^{18} \text{ cm}^{-3}$. (Figs. 2 and 3). TEM views of these normally grown MBE films show considerable areas with no dislocations, but other areas with moderate stacking fault densities (Fig. 4)

Lifetimes derived from reverse current measurements on p-n junctions made from our normal MBE films, have all been low. The reverse current is dominated by the generation term

$$J_{\text{rev}} = \frac{qn_i W}{2\tau_e}$$

where $n_i = 1.45 \times 10^{10} \text{ cm}^{-3}$, q the electronic charge, W the depletion width and τ_e the effective minority lifetime in the depletion region. Our diodes typically have had reverse current densities, J_{rev} , of $\sim 10^{-4} \text{ amps/cm}^2$ giving a τ_e for $W \approx 1 \text{ micron}$, of $\sim 10^{-9} \text{ secs}$, whereas good quality Si should have τ_e values of over 10^{-4} secs . (100 microseconds).

Fig. 2 Mobility of Ga doped Si MBE films grown at UCLA by normal (700°C) growth.

Fig. 3 Mobility of Sb doped Si MBE films grown at UCLA by normal (700°C) growth.

a. Classic Stacking Fault Pattern

b. Line of Dislocations

Figure 4

2. Solid Phase Epitaxial Regrowth

To overcome the three above disadvantages in doping during normal MBE growth, the UCLA group has explored a new technique, first reported by others,^(21,23) of evaporating silicon in an amorphous film at room temperature, co-evaporating the dopants as desired and then crystallizing the film in a solid phase epitaxial regrowth at only $\sim 575^\circ\text{C}$. This appears to work extremely well. It completely solves the doping problems since it is found that 1) sticking coefficients of Ga and Sb are unity; 2) Maximum dopant levels can be pushed far above the solid solubility limits at the melting point, and we have achieved n^+ values of $> 10^{20} \text{ cm}^{-3}$ and p^+ values in the high 10^{19} cm^{-3} range. To our accuracy, all evaporated dopant atoms become electrically active; 3) there is apparently absolutely no smearing of dopant profiles, since the regrowth at 575°C allows dopant atoms to diffuse less than one atomic step.

Using this technique, we have grown for the first time silicon triangular barrier diodes that have the predicted I-V characteristics.⁽²⁰⁾ This structure requires a narrow plane of p-type doping about $50 \text{ \AA}$ wide at a level of $\sim 10^{19} \text{ cm}^{-3}$, superposed on an intrinsic background, as shown in Fig. 5.

RBS results on our solid phase regrown films give an $X_{\min}$ value of $\sim 4\%$, very close to that of 3% for a perfect crystal.

Mobility measurements thus far indicate bulk values over the intermediate range of doping, but reduced values at very low and very high doping level. (Fig. 6).

Fig. 5. **Triangular Barrier Diodes in Silicon
by MBE using Epitaxial Regrowth**

p^+ dopant plane

35-50 Å thick

$N_a = 3-5 \times 10^{18} \text{ cm}^{-3}$

Energy bands at zero bias

Fig. 6. Mobility of Sb doped Si MBE films grown at UCLA by solid phase regrowth.

**Fig. 7. UCLA SILICON MBE SYSTEM
AS OF
12/13/62**

Despite the desirable features of the solid phase regrowth, initial TEM views suggest these films have poorer crystal quality than normally grown MBE films. Diodes we have grown by this technique, and the two solar cells grown in the second year for JPL, however, have been as good as or better than diodes and solar cells grown by normal MBE.

We believe the crystal quality during solid phase growth can be optimized, by evaporating at somewhat elevated temperatures (about 250°C*), and keeping vacuum background pressure close to 10^{-10} Torr during evaporation. (At the lower substrate temperature, gas atoms will have a higher sticking coefficient so contamination is more likely).

For solid phase regrowth, the (100) silicon surface is definitely superior to the (111) surface, as was found earlier in the regrowth of self-implanted amorphized silicon.

* A recent run seems to bear this out.

C. Experimental Details of MBE Station

1. Vacuum System (See Fig. 7.)

The basic station is an all stainless steel 12" diameter Varian ultra-high vacuum system with a total pumping speed of 225 l/sec (consisting of 5 separate 45 l/sec pump elements) controlled by a Varian pump power supply (921-0066). Additional pumping is available with a Titanium Sublimation pump (Varian 922-0032) and a set of vacsorb pumps (Varian 941-6501) for use during initial pumpdown. The base pressure for this system is less than 10^{-10} T.

A Load Lock (Thermionics - custom design) permits sample loading without breaking the vacuum which would necessitate a bakeout. The sample is loaded onto the sample holder on the bench and then attached to the sample carrier in the loading port. The loading port is roughed down to 10^{-4} Torr with vacsorb pumping at which point the first gate valve is opened resulting in the ion pump lowering the loading chamber pressure to 10^{-7} to 10^{-8} Torr. When this pressure is obtained the second gate valve is opened and the sample carrier is inserted into the main station where the sample holder is then transferred to the sample manipulator. The sample carrier is removed and the second gate valve is closed. During transfer the main chamber pressure rises to the mid 10^{-9} Torr range and recovers to the 10^{-10} Torr range within minutes of closing the gate valve. This allows a sample turn-around time of only several hours.

2. Effusion Ovens

The heart of the MBE station consists of the liquid nitrogen shroud, ovens and E-gun assembly. Two effusion ovens are present for either Sb or Ga doping. These ovens were designed and fabricated at UCLA, (see Fig. 8). The ovens consist of 48 turns of 10 mil tantalum wire spring wound against four ceramic posts held on a tantalum can. This can is wrapped by five layers of tantalum foil and encased in an outer Ta can to which a ceramic base plate is attached. The base plate has feed-throughs for both the power and thermocouples. The crucibles within the ovens are made of pyrolytic boron nitride. These ovens can range from room temperature to 1000°C and are controlled by a Eurotherm digital temperature controller (Model 990). Both these ovens are inserted into shuttered stainless steel cans which are attached to the underside of the liquid nitrogen shroud.

3. E-Gun

Beneath the oven-shroud assembly is a modified ultra-high vacuum Airco Temescal E-Gun (FIH-270) with a water cooled crucible (Molybdenum insert in copper block) which can hold 7 cc of silicon. This gun is powered by an Airco Temescal supply (ES-6) capable of 6 KW of power. Actually, during Si growth, only 500 watts has been used.

4. Thickness Monitor

The Si, Ga and Sb flux is monitored by a Sloan Digital Thickness Monitor (Model 200), with a vibrating quartz plate, calibrated to read the film thickness at the substrate.

Fig. 8. SCHEMATIC OF UCLA EFFUSION CELLS

5. Sample Holders and Heaters

The sample holder is mounted directly to a Varian high precision sample manipulator (981-2523) which permits movement in the X, Y, and Z directions coupled with full 360° rotation and 90° flip. (See Fig. 9). There were two sample holders used in this work. In the first the sample is heated resistively, and in the other it is heated radiatively.

The resistance heater is shown in Figure 10. The silicon sample is rectangular, 1.3 cm x 2.3 cm x .05 cm, and is held at both of its ends by molybdenum spring clamps. The sample is heated for initial cleaning to 1000°C or held at growth temperatures of $650 - 750^\circ\text{C}$ by passing heating current from the clamps directly through the silicon sample. This is advantageous in requiring minimum heated surfaces and a rapid thermal time constant. But it is disadvantageous in that 1) some mechanical stress is always present in the sample, causing dislocations and plastic yielding when the sample is hot, 2) hot spots develop at the end contacts so that temperature sometimes varies across the sample by as much as 100°C .

To avoid these problems, and to take advantage of a larger, more standard sample size, the radiant sample heater (Figure 11) was built. Tantalum filaments supported on a boron nitride disk lie in a plane parallel to and just behind the silicon sample. Radiation shields of Ta foil keep the boron nitride disk cool. The 2" diameter sample is supported loosely at three points in the 10 mil thick Ta can in a 2.01" diameter hole in its

FIG. 9. SAMPLE MOUNTING, HEATING, POSITIONING, AND CHANGING. UCLA SILICON MBE SYSTEM

Fig. 10. **SILICON SAMPLE HOLDER FOR
RESISTIVE HEATING**

Fig. 11 SILICON WAFER RADIATION HEATER

front surface. This can carries the sample from the loading station outside the vacuum system, through the load lock and then is twisted into a locked position on the boron nitride disk. The entire sample and heater can be flipped 90° by the Varian flip stem so that the sample is vertical, for inspection or LEED-Auger analysis, or horizontal during growth (see Fig. 9).

The sample can be heated up to 900°C readily using about 280 watts. For additional heating, to $1000\text{--}1200^\circ\text{C}$ electron emission from the Ta filaments is accelerated to the silicon sample with 1000 volts to provide an extra 100 to 150 watts.

The heater assembly has been designed for rapid outgassing, with a low thermal mass. Special attention was paid to ensuring that no metal surface protrudes beyond the silicon surface to act as a contamination source during cleaning or growth.

6. Analytical Tools

The station has several analytical surface tools. For use before and after growth to check surface cleanliness and crystalline quality a LEED/Auger system is present consisting of Varian 4-grid LEED/Auger Optics (981-0127) coupled with a Varian electron gun (981-2145). There is also a UTI quadropole mass spectrometer (Model 100C) with specially modified pole pieces to obtain mass detection in the range of 2 to 500 atomic mass units. The mass spectrometer can be utilized in two modes: as a residual gas analyzer to monitor background gases and as a detector for thermal desorption spectroscopy.

The sensitivity of the Auger electron spectrometer depends on the element detected. For example, Taylor⁽²⁴⁾ reports that for a system comparable to the UCLA one, 2.5% of a monolayer of

oxygen could be detected. Metzger⁽²⁵⁾ reports the detection of $< 10\%$ of a monolayer of antimony using the UCLA system. Auger spectroscopy is three times more sensitive to carbon and 1.5 times more sensitive to oxygen than to antimony.⁽²⁶⁾

The LEED is able to distinguish between amorphous (no LEED pattern), polycrystalline (diffraction rings) and single crystal (diffraction spots) material. The sensitivity of the LEED to surface contaminants is comparable to the Auger. The LEED pattern on (100)Si is significantly changed by the presence of 0.25 monolayers of Sb⁽²⁵⁾ (see Figure 12). At 0.5 monolayers, the pattern changes from the clean surface (2 x 1) structure to the (1 x 1) pattern.

D. Sample Cleaning

The chemical cleaning procedure consisted of a thorough degreasing followed by repeated growth and stripping of an oxide. The final step was the growth of a clean oxide approximately 50 Å thick to protect the surface during transportation to the MBE laboratory. In the UHV chamber, the sample was heated at 700°C to remove any adsorbed gases. Then it was heated to 900°C or 1000°C to remove the clean oxide.

1. Chemical Cleaning

The degreasing procedure consisted of a five minute soak in a warm solvent followed by five minutes in an ultrasonic cleaner for the sequence of three solvents: trichloroethane, acetone and isopropanol. This was followed by a thorough rinse in deionized water.

The oxidizing solution was 5 : 3 : 3 H₂O : HCl : H₂O₂. It was

Figure 12.

LEED Sb on Si(100)

prepared by heating the water and hydrochloric acid to about 80°C then adding the hydrogen peroxide immediately prior to use. The first oxidation step lasted five minutes and was followed by another water rinse.

A new oxidizing solution was made. The repeated stripping and oxidizing followed the pattern:

- a) Soak in 10 : 1 H_2O : HF for twenty seconds.
- b) Brief water rinse, in fresh deionized water.
- c) Two minute soak in oxidizing solution.
- d) Brief water rinse, in fresh deionized water.

On the fifth cycle through that procedure, the oxide was allowed to grow for five minutes. Then the samples were rinsed with deionized water and blown dry with nitrogen gas. The samples were transported in clean teflon containers.

A more detailed description of this chemical cleaning can be found in Reference 27.

D. 2. Thermal Cleaning - LEED and Auger Examination

The chemical cleaning procedure was tested at UCLA by examining the LEED and Auger spectra during and after the thermal cleaning in the vacuum station. The thermal cleaning consisted of a degassing step followed by a high temperature stage to remove the oxide.

The sample as inserted in the UHV station is covered with an oxide and adsorbed gases. There is no LEED pattern visible because of the gases. The Auger spectrum for sample 1B (see Appendix I) is shown in the top trace in Figure 13.

The degassing step involves heating to $\sim 700^\circ\text{C}$ for two

Fig. 13. Auger spectra during thermal cleaning
a) as inserted, b) after degassing and
c) after oxide removal.

minutes. As seen in the second trace in Figure 13, the adsorbed carbon has disappeared. The slight carbon signal grew with time as more gas adsorbed.

After heating to 900°C for two minutes, the oxide has been removed as seen in the bottom trace. Heating at higher temperatures for longer times can induce a carbon signal, presumably by diffusion of carbon to the surface. The LEED pattern after this step showed a very sharp, reconstructed surface.

The Auger and LEED results provide confirmation that the combination of chemical and thermal cleaning was effective for obtaining an atomically clean silicon surface.

E. MBE Film Growth Procedure

A typical procedure for cleaning the substrate and growing an MBE film is given below:

- 1) Chemically clean substrate.
- 2) Load sample through load lock into UHV chamber.
- 3) Take initial Auger spectrum.
- 4) Use an infrared pyrometer to calibrate heater voltage vs. temperature while degassing sample at 700-750°C for 5 minutes.
- 5) Establish voltage setting for 750°C⁽²⁴⁾ for high temperature growth of $\sim 575^\circ\text{C}$ for solid phase crystallization.
- 6) Cool sample.
- 7) Remove oxide:
 - i) Ramp temperature to $\sim 800^\circ\text{C}$ in 5 minutes.
 - ii) Ramp to 1000°C in 2 minutes. Measure temperature with pyrometer.
 - iii) Hold temperature for 2 minutes.
 - iv) Ramp to 800°C in 2 minutes.
 - v) Ramp to room temperature in 5 minutes.
- 8) Check that there is a (2×1) LEED pattern for (100) substrates or (7×7) for (111) substrates.
- 9) Check the Auger spectrum to make sure no carbon or oxygen is present.
- 10) Heat sample to $\sim 200^\circ\text{C}$ facing the load lock and horizontal.
- 11) Start heating the dopant oven.

- 12) Turn on the e-beam evaporator and set the evaporation rate to $1-2 \text{ \AA}/\text{minute}$.
- 13) Reclean the substrate using step 7) except that for high temperature deposition the final temperature should be set to the growth temperature.
- 14) During the cooling step of the recleaning, bring up the e-beam evaporation rate to $100 \text{ \AA}/\text{minute}$.
- 15) When the desired substrate deposition temperature is established, swing the sample into the Si beam and reset the computer program that monitors film thickness.
- 16) Deposit a $50-200 \text{ \AA}$ buffer layer of undoped Si.
- 17) Open the shutter on the dopant oven.
- 18) Deposit the Si and dopant.
- 19) When the final thickness is reached, swing the sample out of the beams and stop the computer.
- 20) Close the oven shutter.
- 21) Turn down the e-beam gradually, then turn it off.
- 22) If the deposition was at high temperature, ramp the temperature to zero.
- 23) If the deposition was amorphous, raise the temperature to the crystallization temperature. The regrowth rate is $230 \text{ \AA}/\text{minute}$ at $575^\circ\text{C}^{(14)}$. During regrowth, sometimes an interface between amorphous and crystalline material can be seen at the surface of the film if there is a temperature gradient. The phases have different reflectivities with the crystalline being shinier. Cool the sample after regrowth.
- 24) Check the LEED pattern to make sure the film is epitaxial.

- 25) Remove sample and place in a clean teflon container before further processing.
- 26) Check the film by eye: it should be uniformly reflecting with no haziness or discoloration.

F. Characterization of Films

The films have been characterized by their resistivity, mobility and doping density as determined by Hall and resistivity measurements using the Van der Pauw technique⁽²⁸⁾ and by fabricating mesa diodes and measuring their I-V curves. With this contract we have been able to improve our data acquisition for these measurements to be fully computer controlled. Additional resistivity measurements have been made at Rockwell by spreading resistance, and crystal quality has been assessed by TEM analysis at UCLA and by Rutherford Back-Scattering done at CalTech.

1. Hall/Van der Pauw

The samples for the Hall/Van der Pauw measurements were epitaxial films isolated from the substrate by a p-n junction. The sample size was approximately 1 cm x 1 cm. Contacts to the film were made by pressing 20 mil diameter In balls onto the corners then sintering at 400°C for 5 minutes under flowing nitrogen gas. Indium wires were attached by pressing them to the balls. For some p-type films, better contacts were formed by using successive layers of In, Al discs then In. This technique worked well for film thicknesses $\geq 0.5 \mu\text{m}$, but the contacts often shorted through thinner films. The contacts were tested by measuring the resistivity with an ohmmeter and requiring that $R(A \rightarrow B) = R(B \rightarrow A)$ for all the contacts.

The apparatus for the measurements is shown in Figure 14.

Fig. 14. Schematic of Hall/Van der Pauw Equipment.

Initial measurements were made using a Keithley 220 current source and a Keithley 177 digital multimeter. At present the HP-85 computer controls the Keithley programmable current source. The switching network is set for either resistivity or Hall measurements. The voltage developed is output by the Keithley 195 digital multimeter to the computer. The resistivity is calculated using

$$\rho = \frac{\pi z}{\ln 2} \left(\frac{R_{AB,CD} + R_{BC,DA}}{2} \right) f \left(\frac{R_{AB,CD}}{R_{BC,DA}} \right)$$

where z is the sample thickness, A,B,C, and D are the four contacts, $R_{AB,CD}$ is the resistance calculated by dividing the voltage drop from C to D by the current flowing from A to B and f is an analytic function plotted in reference 28. For square samples $f = 1$.

The doping density and Hall mobility are found using

$$R_H = \frac{z}{B_0} \frac{\Delta V_{AC}}{I_{BD}} = - \frac{1}{qN_D}$$

and

$$\mu = - \frac{R_H}{\rho} ,$$

where ΔV_{AC} is the change in the potential drop from A to C in the presence of the magnetic field B_0 and current I flowing from B to D. The mobility is independent of the film thickness.

The sample can be cooled to liquid nitrogen or helium temperatures for low temperature measurements.

2. I-V Measurements

The mesa diodes were fabricated in the UCLA MBE laboratory using a diffusion pumped system equipped with a filament evaporator. Aluminum was evaporated to form the back contact and was sintered at 450°C for five minutes. The front contacts were evaporated through a mask with 20 mil diameter holes on a 30 mil grid. These contacts were not sintered if the film were heavily doped. The mesas were etched using a 1:4 $\text{HF} : \text{HNO}_3$ solution for 20 seconds to give a 3 μm high structure.

The measurement apparatus assembled with this contract is shown in Figure 15. The HP-85 computer controls the voltage source. The current is measured by the digital multimeter for high currents. For low currents, the analog output from the picoammeter is fed into the digital multimeter. A curve tracer (Tektronix 5110 oscilloscope with 5CT1N and 5A15N plug-ins) is available for preliminary measurements.

The computer program will plot the forward and reverse I-V curves. In addition it will plot the $\ln I$ vs. V curve and provide values of n at various values of V .

Fig. 15. Schematic of I-V Measurement Equipment

F. 3. Spreading Resistance Measurements

Measurements were carried out on both normally grown and solid phase regrowth Si MBE films at Rockwell International at Anaheim, California using a Spreading Resistance Measurements device, in connection with another UCLA program. Two fine metal points are pressed against the bevel-lapped silicon surface and the voltage drop across the points is recorded for a known current passed through them. The points are ~ 25 microns in radius, osmium tipped, and the two are spaced about 100 microns apart. Sampled spots on the surface are about 1 micron apart, so that with a bevel of 1/100, one can approach a depth resolution of 100 Å. The resistance so measured is the local spreading resistance around the tips, averaged over some volume comparable to the tip contact area which depends on the load applied - usually ~ 20 grams (29).

While absolute calibration is difficult and Debye smearing must be taken into account, good variation of resistivity with depth can be found.

In the present measurements the results on UCLA MBE films

- 1) confirmed the approximate absolute doping levels in Sb and Ga doped films as measured in our Hall probe.
- 2) showed that background impurity levels as low as 10^{13} cm^{-3} were achieved in UCLA high resistance films, grown by normal (700°C) MBE growth; (see Figure 16).
- 3) showed that solid phase regrowth films had impurity levels as low as $\sim 3 \times 10^{13} \text{ cm}^{-3}$.

F. 4. Transmission Electron Microscope (TEM) Results

Several samples of normally grown Si MBE films and one sample of solid regrowth film have been examined in the UCLA TEM facility. A hole was jet-etched in the 12 mil thick silicon substrate and the tapered edges of the MBE grown film, about 0.6 microns thick, were examined. The results showed many areas in the normally grown MBE film that were entirely free of dislocations. Fig. 4 shows an area of a normally grown MBE silicon film doped with Ga to $8 \times 10^{17} \text{ cm}^{-3}$ where there were about 10^5 stacking faults cm^{-2} , and a line of dislocations.

TEM views of the one solid phase regrowth film examined thus far showed almost no regions free of dislocations with higher densities than the normally grown films.

F. 5. R.B.S. Results

Rutherford Backscattering Analysis was carried out at CalTech on several of the solid phase regrown films. A relatively good film is shown in Fig. 17, which gives a $X_{\min}$ value of $\sim 4\%$ compared to a value of $\sim 3\%$ for perfect silicon. This is the ratio of the minimum reflection value just below the surface peak for the aligned epitaxial crystal to that at a random direction. This is a good indication that the regrown film is of quite high crystal quality though it is not perfect. It does not allow inferences of minority lifetime, for example.

Fig. 17. Rutherford Back Scattering Results for a Solid Phase Regrown Film.

III. Experimental Results

A. Summary of first year's efforts

The major accomplishments and findings ⁽³⁰⁾ during the period 3/22/82 to 3/21/83 were:

- i. The diffusion length of good quality substrates (100 to 200 microns) was not degraded by the high temperature cleaning used before MBE growth.
- ii. Two testable solar cells were made by MBE growth of n-on-p junctions at UCLA. They were fabricated and tested at JPL. Even the better cell had poor properties ($\eta = 2.8\%$, $J_{sc} = 27 \text{ mA}$, $V_{oc} = 0.38 \text{ V}$ and Fill Factor = 0.55) due either to dislocations or deep level impurities.
- iii. It was demonstrated that the JPL SIMS analysis could give profiles both of dopants and of troublesome impurities in MBE grown films.
- iv. It was shown that UCLA can grow Si MBE films with good bulk mobility values for both n and p-type dopants except at the extremely pure and extremely heavily doped limits. There the mobility falls below bulk values.
- v. Doping with Sb was understood, making sharp n-type profiles without transient effects possible.
- vi. Films with net doping density down to 10^{13} cm^{-3} with few or no detectable dislocations were grown by MBE.

vii. Initial calculations indicated that a cascade Si cell should be investigated.

B. Second Year's Efforts

1. Films Grown

There were thirty-two runs made during the second year of this contract. (see Appendix I). Of these, seven were sent to JPL or Applied Solar Energy Corporation for solar cell fabrication, and eight were made into mesa diodes at UCLA. The rest were used for testing of the MBE growth technique or were not single crystal films. All substrates for solar cells were float zone (100) p-type wafers with resistivity of $1 - 2 \Omega\text{-cm}$.

2. Solar Cell Results

Table I contains a summary of the results on the solar cells tested at JPL during the second year.

The first cell, SPE #8, was grown using solid phase epitaxy before that technique was well-established. Rutherford backscattering measurements at CalTech on a similar sample showed incomplete recrystallization. We believe that is the reason for the poor characteristics.

Samples JPL 102 and JPL 103 were fabricated at Applied Solar Energy Corporation. They were not a standard size for the metalization apparatus. One sample was shorted around the busbar. The other may also have shorted during metalization. After removing the busbar on JPL 103, it was possible to measure the reverse leakage current to be $\sim 0.2 \text{ A/cm}^2$ at -0.5V , but there were large uncertainties in the actual area. Sample JPL 102 showed some rectification after removing the busbar but mesa diodes made on it were shorted after sintering the contacts.

TABLE I. Solar Cell Results

Sample	J_{sc} (mA)	V_{oc} (mV)	n (%)	FF
SPE#8	poor characteristics			
JPL102	short circuited in processing			
JPL103	short circuited in processing			
JPL109	21.9	454.9	4.70	0.707
JPL110	23.5	486.7	4.79	0.713
JPL112	lost during processing			
JPL113	lost during processing			

The solar cells from JPL109 and JPL110 were fabricated at JPL. The samples were cut to 1 x 2 cm by making a groove in the back then cleaving. The contacts were made by e-beam evaporation. They were 600 Å of Ti, 400 Å of Pd, 4 μm (2.5 μm) of Ag for the front (back) contacts. The back contacts were sintered, but the front were not, due to concern about metal shorting the junction through the film. The contact area was ~ 7%. Sample JPL110 was annealed in H₂ at 750°C for 1 hour before metalization.

The dark forward, dark reverse and light I-V curves and the spectral response for JPL110 are shown in Figures 18 - 21. The reverse leakage current is ~ 0.1 A/cm² at -0.5V, which is very high. There is a large increase in the open circuit voltage and fill factor over the previous MBE cell. The short circuit current is comparable, so the efficiency is much higher.

Samples JPL112 and JPL113 were ruined in processing at JPL.

3. Diode Results

The overall quality of the mesa diodes was not good. There was a large variation of the reverse leakage current over the sample, but had no obvious correlation with position in the holder, crystallographic orientation or characteristic of the etched film. The reverse current was very sensitive to the environmental conditions. It would decrease by breathing on the sample and increase by blowing dry N₂ through a nalgon tube. This is consistent with the current being dominated by conduction by ions on the surface.⁽³¹⁾ Because this is a large effect, we do not believe we know the true reverse current of the p-n junction over small sample areas.

Fig. 18. Dark Forward Characteristic for JPL110.

Fig. 19. DARK REVERSE I-V

Fig. 20. **LIGHT I-V CURVE**

Fig. 21. Spectral Response of JPL110.

The results for one of the diodes made from sample JPL105 are shown in Figure 22. The reverse leakage current at 0.5V was 2×10^{-4} A/cm². The breakdown voltage was 35V, lower than the expected 45V for the 1 Ω -cm substrate. The n-values for the dark forward characteristics were high.

Fig. 22. Diode Dark I-V Characteristics of JPL105

III. B. 4. SIMS Results

Secondary Ion Mass Spectrometry (SIMS) measurements were performed at JPL on MBE films to determine contamination at the interface, impurities in the films and the doping profile.

During the first year, the SIMS results showed smeared Sb profiles. This is consistent with the understanding of Sb incorporation developed in this lab. That problem was eliminated.

Some SIMS results for JPL105 are shown in Figure 23.

The important features are the peaks in the C and O at the interface, the elevated C level in the film, the sharpness of the Sb profile and the relatively uniform Sb doping. For that sample, the Auger showed no C or O after the cleaning. It is therefore possible that the source of the carbon is the filaments of the e-beam evaporator or the dopant oven. The most recent SIMS data showed much less C contamination, so the problem has been alleviated.

In Figure 24 are the results of looking for Ni, Cu and Au contamination in JPL101. The Ni was greater in both the film and the substrate than in a high purity silicon sample from Union Carbide Corporation but no peak at the interface could be detected. There is an elevated amount of Cu and Au in the epi film. Also, there is a pronounced Cu peak at the interface. After these data were taken, a Si washer was placed over the Si source to shield the Cu hearth from the e-beam. Recent results still show Cu contamination. However, the washer had been melted by the e-beam. A heavy ring of Si is now in place, and this may eliminate the Cu in the film.

Fig. 23. SIMS Results for C, O and Sb on JPL105.

Fig. 24. SIMS Results for Ni, Cu and Au on JPL105.

Not shown are the SIMS results for Mo in JPL 105 and PP1. An initially very high estimate of the Mo content lead to the removal of the Mo crucible around the Si source. The recent data revise that estimate to say there is a negligible Mo contamination.

IV. Computer Modeling

A. Introduction

During the first year, calculations carried out by Dr. T. Daud of J.P.L. had already indicated that a double junction, cascade cell made entirely of silicon might achieve higher efficiency than any single silicon cell, and in addition, almost double the open circuit voltage. Therefore, a computer program was developed and put into use in the second year which was relatively simple but accurate enough to allow more definite conclusions on the performance of the cascade cell and to guide its design. One important aspect of the program is the ease with which calculations can be performed for a variety of input parameters. Another is that the program is self-calibrating; comparisons can be made with the results for single cells computed using the same model. The sensitivity of the computed properties to the uncertainties in the input parameters is easily calculated. Before presenting some results of our calculations we will outline the derivation of the equations used, and the assumptions that enter the derivation. A listing of the cascade cell program is given in Appendix II.

B. Outline of model

The geometry and input parameters for the cascade cell are shown in Figures 25 and 26. The cascade cell is modeled as the series combination of two back surface field (BSF) cells; that is, two n^+pp^+ layers. We will treat the effects of the tunnel junction by specifying a surface recombination velocity at the p^+n^+ junction. In fact, any minority carrier that reaches the tunnel junction will be swept across and will not contribute to the

Fig. 25. TWO-LAYER TANDEM SILICON SOLAR CELL

Figure 26. Geometry and Input Parameters for Cascade Solar Cell Calculation

photocurrent. This corresponds to a surface recombination velocity of 5×10^6 cm/s. In the front cell, the pp^+ transition will reduce the effect on the minority carriers of the surface recombination at the tunnel junction by building in an electric field that will partially reflect the carriers. This can be incorporated by specifying an effective surface recombination velocity at the pp^+ interface, S_{eff} . The concept of S_{eff} is extended to model the possibility of reflecting more of the minority carriers before they reach the tunnel junction. As we shall see, for the cascade cell to be more efficient than a single cell, S_{eff} must be lower than it would be for a simple pp^+ transition.

The input parameters are shown in Figure 26. They are:

- i) the doping density, assumed to be uniform
- ii) the minority carrier diffusion lengths, diffusion constants and lifetimes in the n^+ and p regions.
- iii) the depletion widths in the p regions.
(the depletion width in the n^+ region is neglected).
- iv) the surface recombination velocities at the front and rear surfaces and at the front p^+n^+ junction.
- v) the solar spectrum for AM0 specified at 101 wavelengths.
- vi) the absorption coefficients in silicon at those wavelengths.
- vii) the thicknesses of: the n^+ regions, the p^+ regions, and the total cell thickness.

The following derivation for a single BSF cell is a synthesis of previous work.^(32,33,34) The photocurrents can be evaluated by assuming low injection levels and abrupt junctions.

The minority carrier continuity equations are:

$$\frac{1}{q} \frac{dJ_p}{dx} - G_p + \frac{(p_n - p_{no})}{\tau_p} = 0 \quad \text{in the } n\text{-type material}$$

$$\frac{1}{q} \frac{dJ_n}{dx} + G_n - \frac{(n_p - n_{po})}{\tau_n} = 0 \quad \text{in the } p\text{-type material}$$

where all symbols have their usual meanings. The hole and electron currents are assumed to be

$$J_p = -q D_p \frac{dp_n}{dx}$$

$$J_n = q D_n \frac{dn_p}{dx}$$

where the electric field has been set to zero in the uniform material. Note that these expressions for the current assume that the current is determined by the diffusion term in the quasineutral region.

The rate of generation of electron-hole pairs by photons of wavelength λ at a distance x from the surface of the semiconductor is

$$G(\lambda, x) = \alpha(\lambda) F(\lambda) (1 - R(\lambda)) e^{-\alpha(\lambda)x}$$

where

$\alpha(\lambda)$ is the absorption coefficient

$F(\lambda)$ is the photon flux per unit bandwidth at the surface
and

$R(\lambda)$ is the reflection coefficient for the surface.

We will define the boundary conditions at the coordinates of the front cell in Figure 26. The rear cell in the cascade will be handled analogously.

The boundary conditions for the continuity equations at the p-n junction are that there be negligible excess minority carriers:

$$n_p(x_1) = n_{p0}$$

$$p_n(x_1) = p_{n0}$$

At the $p - p^+$ junction, the boundary condition is

$$n_p(x_2) = n_{p^+}(x_2) \frac{N_A^+}{N_A}$$

At the surfaces of the BSF cell, the boundary conditions are determined by the surface recombination velocities, S_n or S_p :

$$D_p \nabla (p_n - p_{no}) = S_p (p_n - p_{no}) \quad \text{at } x = 0$$

$$-D_n \nabla (n_{p^+} - n_{p^+o}) = S_n (n_{p^+} - n_{p^+o}) \quad \text{at } x = x_3.$$

For each incident wavelength, the solution for the photocurrent is divided into three parts: the hole and electron photocurrents evaluated at the depletion edge, and the photocurrent generated in the depletion region. We neglect the photocurrent generated in the p^+ region. The hole photocurrent at the depletion edge of the n^+ region is:

$$J_p = \left[\frac{qF(1-R)\alpha L_p}{\alpha^2 L_p^2 - 1} \right] \quad (1)$$

$$* \left[\frac{\frac{S_p L_p}{D_p} + \alpha L_p - e^{-\alpha x_1} \left(\frac{S_p L_p}{D_p} \cosh \frac{x_1}{L_p} + \sinh \frac{x_1}{L_p} \right)}{\frac{S_p L_p}{D_p} \sinh \frac{x_1}{L_p} + \cosh \frac{x_1}{L_p}} - \alpha L_p e^{-\alpha x} \right]$$

where D_p is the diffusion constant and $L_p = \sqrt{D_p \tau_p}$ is the diffusion length.

The photocurrent from electrons which are collected at the depletion edge of the base p-region is:

$$J_n = \left[\frac{qF(1-R)\alpha L_n e^{-\alpha(x_1+W_1)}}{(\alpha^2 L_n^2 - 1)} \right] \quad (2)$$

$$* \left[\alpha L_n - \frac{\frac{S_n L_n}{D_n} (\cosh \frac{H'}{L_n} - e^{-\alpha H'}) + \sinh \frac{H'}{L_n} + \alpha L_n e^{-\alpha H'}}{\frac{S_n L_n}{D_n} \sinh \frac{H'}{L_n} + \cosh \frac{H'}{L_n}} \right]$$

where W_1 is the depletion width in the p-region, selected as a parameter for each calculation and $H' = x_2 - x_1 - W_1$ is the width of the neutral p-region.

All the carriers generated in the depletion region are assumed to be collected before they can recombine. Therefore the depletion region contributes a current

$$J_{dr} = qF(1 - R)e^{-\alpha x_1}(1 - e^{-\alpha W_1}). \quad (3)$$

The total photocurrent is the sum of Eqs. (1), (2) and (3), integrated over the solar spectrum. That is, the short circuit current is given by

$$J_{sc} = \int_{\lambda} (J_p(\lambda) + J_n(\lambda) + J_{dr}(\lambda)) d\lambda. \quad (4)$$

The dark current for the cell is made up of the injection current, J_{inj} , the recombination-generation current, J_{rg} , and the tunneling current. In this calculation, the tunneling current is neglected. The injection current is $J_{inj} = J_0(e^{eV_o/kT} - 1)$ where J_0 will be defined in Eq. (5). Note that by analogy with normal p-n junction terminology, J_{inj} is simply the diffusion dominated dark current of the junction. The effect of the BSF is to reduce the loss of electrons from flow across the pp^+ boundary and recombination at the back of the p^+ region. This effect can be incorporated in an expression for J_0 by defining an effective surface recombination velocity, S_{eff} at the pp^+ boundary. The value of S_{eff} is lower than the surface recombination velocity at the back of the p^+ region. Using this effect, the expression for J_0 is:

$$J_0 = J_0(n^+-\text{region}) + J_0(p\text{-region})$$

$$= q \frac{D_p}{L_p} \frac{n_i^2}{N_D} \frac{\frac{S_p L_p}{D_p} \cosh \frac{x_1}{L_p} + \sinh \frac{x_1}{L_p}}{\frac{S_p L_p}{D_p} \sinh \frac{x_1}{L_p} + \cosh \frac{x_1}{L_p}} + q \frac{D_n}{L_n} \frac{n_i^2}{N_A} \frac{\frac{S_{eff} L_n}{D_n} \cosh \frac{W_p}{L_n} + \sinh \frac{W_p}{L_n}}{\cosh \frac{W_p}{L_n} + \frac{S_{eff} L_n}{D_n} \sinh \frac{W_p}{L_n}} \quad (5)$$

where $W_p = x_2 - x_1$, is the width of the p-region and $S_{eff} = S_n \frac{N_A}{N_A + N_D}$ is the effective surface recombination velocity assuming the p^+ layer is much thinner than the electron diffusion length in it

The derivation of the recombination-generation current assumed the same doping on both sides of the junction and a single recombination center near the center of the gap. The resulting expression is:

$$J_{rg} = \frac{q n_i W_1}{\sqrt{\tau_n \tau_p}} \frac{2 \sinh(qV_0/2kT)}{(V_d - V_0)/kT} f(b) \quad (6)$$

where τ_n, τ_p are the lifetimes in the p- and n-regions and

$$V_d = \frac{kT}{q} \ln \left(\frac{N_A N_D}{n_i^2} \right)$$

is the built-in voltage and $f(b)$ involves the trap energy, the intrinsic Fermi energy and the lifetimes. The quantity $f(b)$ was assumed to be equal to its maximum of $\pi/2$.

The total output current is found from Eqs. (4), (5) and (6):

$$J_{out} = J_{sc} - J_0 (e^{eV_o/kT} - 1) - J_{rg}. \quad (7)$$

From this expression, the I-V curve for a BSF cell can be calculated. From that, the maximum power, efficiency and fill factor can be evaluated.

The calculation for the cascade cell is depicted schematically in Figure 27. The cell dimensions are determined by the condition that the short circuit currents in the two cells be equal. The I-V curve for the cascade is derived from the I-V curves for the individual cells by requiring $I_{out}(1) = I_{out}(2)$ and finding the appropriate voltages. In the output from the calculation are the maximum power, and hence the efficiency, the short circuit current and open circuit voltage, from which the fill factor can be calculated.

Figure 27. Schematic of Cascade Cell Calculations

C. Results of Calculations

We will first present some results⁽³⁵⁾ of these calculations assuming a perfect reflection of minority carriers before the tunnel junction, then determine the condition on S_{eff} for the cascade cell to be more efficient than a single cell, and will finish by proposing parameters for a reasonable cell.

1. Perfect reflection before tunnel junction

Some of the results of these calculations assuming a perfect reflection of minority carriers before the tunnel junction are shown in Figure 28. The data are parameterized by the base resistivities in the single cell and in the rear cell of the cascade structure. The base resistivity in the front cell was assumed to be $0.1 \Omega\text{-cm}$.

The input parameters used in this calculation were taken from Hovel (31). They are specified in terms of the base resistivity and are shown in Table II. All symbols have their usual meanings.

The important trends to note are:

- 1) The cascade cells show an enhanced efficiency for practical thicknesses.
- 2) The increase in efficiency is greater for higher resistivity substrates.
- 3) At typical cell thicknesses (150-300 μm), the cascade cells with high resistivity substrates are more efficient than the

Figure 28. Calculated AMO efficiency as a function of total cell thickness for cascade and single Si cells. Input parameters from Table II (except both p^+ and n^+ layers were $0.2 \mu\text{m}$ wide) and $S_n = S_p = 10^4 \text{ cm/s}$ on the outer surfaces.

TABLE II.

Parameters for Calculation

ρ (base) (Ω -cm)	N_A (cm^{-3})	D_N (cm^2/s)	L_n (μm)	τ_n (μs)	w_n (μm)
0.1	5×10^{17}	10.9	52.2	2.5	0.05
1	1.5×10^{16}	27	164	10	0.29
10	1.25×10^{15}	36	232	15	0.93

N_D^+ (cm^{-3})	D_p (cm^2/s)	L_p (μm)	τ (μs)
10^{19}	1.295	7.2	0.4

$$N_A^+ = 10^{20} \text{ cm}^{-3}$$

Width of front	n^+ layer	=	0.2 μm
Width of front	p^+ layer	=	0.1 μm
Width of rear	n^+ layer	=	0.1 μm
Width of rear	p^+ layer	=	0.2 μm

single cells with the lowest resistivity substrates. This would be an advantage for crystal growth.

- 4) For a cascade cell, there is a maximum in the efficiency as a function of the rear base resistivity near $0.3 \Omega\text{-cm}$ (not shown on graph).
- 5) The increase in efficiency possible for cascade cells is approximately one percentage point. Note again that the efficiencies were computed using AMO.

In Figure 29 are shown the computed data for the width of the front p-layer, short circuit current, and the open circuit voltage as a function of total thickness for cells with front base resistivity of $0.1 \Omega\text{-cm}$ and substrate resistivity of $1 \Omega\text{-cm}$. As expected, the front cell must initially increase with x_{TOT} in order to match the short circuit currents. The short circuit current and open circuit voltage have the same qualitative thickness dependence that they do for single cells⁽³²⁾.

A plot of the efficiency of $150 \mu\text{m}$ thick cells as a function of the three remaining surface recombination velocities (SP1, SP2 and SN2) is shown in Figure 30. The efficiency is insensitive to losses of the electrons at the back contact (high SN2) and losses of the holes at the tunnel junction (high SP2). However, there is a large decrease in efficiency if there is a high surface recombination velocity at the front surface (high SP1).

Fig. 29. Total thickness (μm).

Fig. 30. Efficiency as a function of surface recombination velocity.

2. Condition on S_{eff}

The effect of non-ideal reflection of electrons before the tunnel junction is shown in Figure 31 for a cell with $x_{\text{TOT}} = 100 \text{ } \mu\text{m}$. For the standard BSF formed by an abrupt pp^+ junction, $S_{\text{eff}} \sim 10^4 \text{ cm/s}$. For that value of S_{eff} , the efficiency of the cascade cell is less than that for a single cell. To make the cascade more efficient it is necessary, for this case, to reduce S_{eff} below $2 \times 10^3 \text{ cm/s}$. This might be possible by building in a doping gradient through the front base to enhance the reflection of electrons away from the tunnel junction.

The open circuit voltage is also a function of S_{eff} . For the cells shown in Figure 31, V_{oc} drops from 1.33V for $S_{\text{eff}} = 0$ to 1.18V for $S_{\text{eff}} = 5 \times 10^6 \text{ cm/s}$. For the single cell, the calculated V_{oc} is 0.68V.

3. Proposed Parameters

The choice of parameters for a proposed cascade cell is influenced by both theoretical and experimental considerations. For example, the optimum thickness is less than usual substrate thicknesses. However, calculation shows that the decrease in efficiency from an optimal $x_{\text{TOT}} = 125 \text{ } \mu\text{m}$ to $x_{\text{TOT}} = 250 \text{ } \mu\text{m}$ is only 0.2%, which is not significant at this stage.

A more stringent experimental constraint is that the present UCLA Si-MBE station can conveniently grow only $\sim 2 \text{ } \mu\text{m}$

Fig 37. **AMO EFFICIENCY OF Si SOLAR CELLS**
(THICKNESS = $100\ \mu\text{m}$)

of material. Of this, $0.6 \mu\text{m}$ would be used in the n^+ , p^+ and n^+ layers leaving $1.4 \mu\text{m}$ for the front base. In Figures 32 and 33 we show some of the characteristics of mismatched cells by plotting η , J_{sc} and V_{oc} as a function of the width of the front p-layer, X_{p1} . For these calculations, $S_{eff} = 2.5 \times 10^4 \text{ cm/s}$ and $SP2 = 5 \times 10^6 \text{ cm/s}$; i.e. we assume that there are severe losses at the tunnel junction. As expected, the efficiency decreases rapidly with X_{p1} because the current generated in the front cell decreases. By decreasing X_{p1} from the optimum of $1.9 \mu\text{m}$ to $1.4 \mu\text{m}$ one would decrease the efficiency by 0.8%. This is not sufficient to rule out the possible growth of a cascade cell in the UCLA system.

Interestingly, the changes in the open circuit voltage of the two cells cancel causing the open circuit voltage of the cascade to vary by only $\sim 1\%$. This means that one could use V_{oc} as the first test of a cascade cell and grow thin, mismatched cells to test the concept.

Fig. 32. Efficiency as a function of front p-layer thickness.

Fig. 33. J_{sc} and V_{oc} as a function of front p-layer thickness.

D. Extensions of Computation

There are two extensions of the program we would like to make. The first is to include the option of using the AM1.5 solar spectrum. This will be useful because most other calculations for terrestrial solar cells cite results for AM1.5. The second is to investigate cascade cells where the front cell is made of GaP or BP. To make this change we need the absorption coefficients for those materials and good estimates of the minority carrier properties. The adaptations to the program are relatively straightforward. At present it is not technologically feasible to grow these structures, but recent advances (36, 37) are encouraging.

V. Summary of Two-Year Effort

A. Principal Accomplishments and Findings

1. The diffusion length of good quality substrates (100 to 200 microns) is not degraded by the high temperature cleaning (1100°C for 2 mins) used before MBE growth begins.

2. Five solar cells have been made by MBE growth of n-on-p junctions at UCLA and fabricated and tested at JPL. With no surface passivation nor AR coatings, the efficiency of the two cells made the first year (by normal MBE growth at 700°C) measured $\sim 2.7\%$, while that of the two better cells made the second year (by solid phase epitaxial regrowth) was $\sim 4.8\%$. All four cells had poor properties because of high reverse leakage currents at the p-n junction, as evidenced by the low V_{oc} .

3. SIMS (Secondary Ion Mass Spectroscopy) runs at JPL on UCLA-grown MBE films confirmed Auger probe analysis results at UCLA in showing that carbon at the substrate epi interface is reduced to an insignificant level (< 0.1 monolayer) by an etching-cleaning treatment that uses a peroxide to leave a thin oxide ($\sim 30 \text{ \AA}$) on the silicon surface which is then evaporated during initial heat cleaning.

4. SIMS measurements at JPL and Hall measurements at UCLA confirm that Sb n-type doping levels achieved during MBE are close to those intended.

5. A computer program was applied to calculating efficiencies of both single and double cascade silicon solar cells of various

geometries and profiles. It was found that the cascade cell can improve efficiency of the best single cell by 1 or 2% (at the 19-20% level) and can provide almost twice the open-circuit output voltage. Required for this is a good tunnel junction connecting the cells in series, with a reflecting built-in field to avoid minority carrier loss. (35)

B. Related MBE Progress at UCLA During the Period.

1. The Hall probe was put into regular use and automated for mobility measurements.

2. A probe station for measuring and recording diode characteristics was acquired and put into regular use.

3. The new technique of amorphous deposition at room temperature followed by solid phase epitaxial regrowth at $\sim 550^\circ\text{C}$ was pioneered at UCLA and shown to provide great advantages over normal high temperature (700°C) MBE growth. It demonstrated unity sticking coefficients of Sb and Ga dopants, absolutely no smearing of profile, much higher maximum doping levels up to $> 10^{20} \text{ cm}^{-3}$ for both Ga and Sb, and good crystal quality judged by Rutherford Back Scattering and mobility measurements. The first silicon triangular barrier diode was grown by this technique and a report published.

4. Intrinsic films of high resistivity (net impurity content $< 10^{13} \text{ cm}^{-3}$) were grown by MBE, demonstrating the

C. Problem Areas

P-n junction diodes made by the UCLA MBE station continue to have much larger reverse leakage current than required for high efficiency solar cells. The cause is thought to be generation-recombination centers at the junction, due to metal impurities or dislocations. SIMS results from JPL indicate that copper could be a problem and we cannot yet rule out dislocations as a cause. Since at least two other silicon MBE stations (Bean at Bell Labs and Kasper in Germany) are making high quality junctions, it is only a matter of time until we find the problem at UCLA and correct it.

VI. Future Effort

It is clear that silicon MBE is rapidly maturing as a powerful new technique for making well-controlled, arbitrary and complex device profiles. Recent progress in major American, Japanese and German laboratories has prompted commitments at Bell, General Electric and now IBM to mount major efforts in silicon MBE growth. This means that sophisticated profile, high efficiency silicon solar cells will soon be grown by MBE, regardless of which laboratory does it first.

The graded profiles required to provide effective front, (shallow grading), and rear (deep grading), surface fields for minimum surface recombination, can only be provided by MBE. Thus, the optimum efficiency single cell will eventually need to be grown by MBE.

The much more complicated double cascade silicon cell that we have analyzed, can clearly only be made by MBE.

In addition, it is quite likely that good heterojunctions will soon be grown between silicon and some other semiconductor of very different band gap. The likely candidates are GaP (2.4 eV) and BP (2.0 eV). A cascade cell using silicon and one of these can have a theoretical efficiency much higher than a single cell in silicon or even a double cascade cell in silicon alone. Since such solar cells are being attempted, MBE will be an important part of a future effort for high efficiency cells.

On the other hand, there is little hope of achieving these advantages until extremely good MBE-grown p-n junctions are routinely achievable.

It is therefore recommended that a future effort be planned to continue the present program in silicon MBE solar cells as soon as some facility, available for contract work with JPL, demonstrates the requisite high quality junctions.

Specifically, the next objectives of any such program should be:

1. Demonstrate high efficiency single silicon cells with simple (flat) profiles.
2. Demonstrate improvements in efficiency with front and back-surface fields.
3. Demonstrate a good tunnel junction in silicon.
4. Grow double junction cascade cells in silicon connected in series by a tunnel junction.
5. Grow heterostructure cells between silicon and other semiconductors with high efficiencies.

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Appendix 1. List of Films Grown in Second Year

TABLE A.1
Films Grown 7/83 to 4/84

<u>DATE</u>	<u>SAMPLE</u>	<u>PROFILE</u>	<u>COMMENTS</u> *
7/10/83	SPE#8	$0.6\mu\text{m}$, $8 \times 10^{19}\text{cm}^{-3}\text{Sb}$	H,S
8/9/83	DIODETEST	p^+pn on n^+	D
8/22/83	PS1	undoped	amorphous, TEM
8/24/83	PS2	undoped	amorphous, TEM
8/30/83	PS3		surface pitted
10/19/83	1A→1C		test sample cleaning
10/26/83	JPL101	$0.2\mu\text{m}$ of $5 \times 10^{19}\text{cm}^{-3}\text{Sb}$ on $0.4\mu\text{m}$ of $2 \times 10^{19}\text{Sb}$ on $1\ \Omega\text{-cm p-type}$	SIMS, H
10/27/83	JPL102	"	S
10/27/83	JPL103	"	S
11/3/83	JPL104	$0.6\mu\text{m}$, $1 \times 10^{19}\text{Sb}$ on $1\ \Omega\text{-cm p-type}$	D,H
11/16/83	JPL105	$0.6\mu\text{m}$, $6 \times 10^{19}\text{Sb}$ on $1\ \Omega\text{-cm p-type}$	D, SIMS
11/21/83	JPL106		source damaged
12/7/83	DIODE7	$0.6\mu\text{m}$, $1 \times 10^{20}\text{Sb}$ on $1\ \Omega\text{-cm p-type}$	H

<u>DATE</u>	<u>SAMPLE</u>	<u>PROFILE</u>	<u>COMMENTS</u>
12/9/83	DIODE8	$0.6\mu\text{m } n^{++}$	amorphous, (N_D too high)
12/13/83	JPL109	$0.6\mu\text{m}, 1 \times 10^{20} \text{ Sb}$ on $1 \Omega\text{-cm p-type}$	S
12/14/83	JPL110	"	S, annealed in H_2 at 750°C for 1 hr.)
12/15/83	JPL111	"	D
1/7/84	JPL112	$0.2\mu\text{m}, 6 \times 10^{19} \text{ Sb}$ on $1 \Omega\text{-cm p-type}$	S
1/9/84	JPL113	"	S
1/10/84	JPL114	"	D
1/11/84	JPL115	n^+p on p-type	D
2/9/84	P1	$0.6\mu\text{m}, 5 \times 10^{18} \text{ Sb}$	amorphous
3/10/84	P2	$0.6\mu\text{m}, 10^{16} \text{ Sb}$	amorphous
2/13/84	P3	$0.6\mu\text{m}, 10^{16} \text{ Sb}$	amorphous
2/14/84	P4	$0.1\mu\text{m}, 3 \times 10^{17} \text{ Ga}$	poor LEED
2/21/84	P5		uncleanable
2/22/84	P6	$0.1\mu\text{m}, 10^{17} \text{ Ga}$ $0.1\mu\text{m}, 10^{16} \text{ Sb}$	no LEED

<u>DATE</u>	<u>SAMPLE</u>	<u>PROFILE</u>	<u>COMMENTS</u>
2/24/84	P7	$0.6\mu\text{m}, 10^{17}$ Sb	good LEED
4/20/84	PP1	$0.6\mu\text{m}, 5 \times 10^{16}$ Sb	SIMS, D
4/21	TJ1	$0.6\mu\text{m}, 10^{19}$ Ga on $2 \times 10^{18} \text{cm}^{-3}$ n-type	D, SIMS

*KEY: H = Hall/Van der Pauw Measurements

S = Solar Cell Fabricated

D = Mesa Diodes Made

TEM = Transmission Electron Microscopy

SIMS = Secondary Ion Mass Spectrometry

APPENDIX II. Listing of Cascade Cell Computer Program

```
// EXEC WATSUB
*JOB
C THIS VERSION WILL FIND THE DIMENSIONS TO MATCH THE SHORT
C CIRCUIT CURRENT IN THE TWO CELLS BY FINDING THE ZERO OF THE
C FUNCTION THAT CALCULATES THE DIFFERENCE IN THE CURRENTS OF THE
C CELLS. THE TOTAL CELL SIZE IS FIXED IN THIS PROGRAM.
C
C IT WILL THEN CALCULATE THE I-V CURVES FOR THE TWO CELLS AND
C FOR THE TOTAL CELL FORCING THE CURRENT TO BE CONSTANT.
C IT WILL CALCULATE THE OUTPUT POWER, FIND THE MAXIMUM
C AS WELL AS THE OPEN CIRCUIT VOLTAGE AND THE FILL FACTOR.
C
C PROGRAM NAME = TANDEM ***THIS VERSION IS TAN8 *****
C IN THIS VERSION, THE TWO CELLS CAN HAVE DIFFERENT LIFETIMES
C THE OUTPUT INCLUDES A BREAKDOWN OF THE CURRENT
C
REAL JN1,JN2,JP1,JP2,JDR1,JDR2
REAL ND1,NP2,KT,NI
REAL LN1,LN2,LP1,LP2
REAL J1,J2,JSC1,JSC2,J01,J02,JRG1,JRG2
REAL JINJ1,JINJ2,IOUT1,IOUT2,I2CHK,IMAX
C
EXTERNAL DIFFJ
C
COMMON/JOUT/JN1(300),JN2(300),JP1(300),JP2(300),JDR1(300),
$JDR2(300),JRG1(300),JRG2(300),JINJ1(300),JINJ2(300),J1,J2
COMMON/DATA/ F(300),ALPHA(300),R(300)
COMMON/OUTPUT/ V(300),IOUT1(300),IOUT2(300),POUT1(300),
$POUT2(300), DERIV(300), I2CHK(300), Z(300),P(300)
COMMON/SIZE/XN1,XN2,XPP1,XPP2,XTOT,X1,X2,X3,X4,X5,X6,XP2
COMMON/DOPING/ ND1,P1,PP1,NP2,P2,PP2
COMMON/LS/LN1,LN2,LP1,LP2,SN1,SN2,SP1,SP2,S1,S2
COMMON/D/DN1,DN2,DP1,DP2,Q,KT,NEND,W1,W2
C
C F(J)= SOLAR FLUX AT WAVELENGTH DESIGNATED BY J
C ALPHA(J)= ABSORPTION CONSTANT AT WAVELENGTH DESIGNATED BY J
C R(J)= REFLECTION COEFFICIENT AT WAVELENGTH DESIGNATED BY J
C X1-X6=WIDTHS OF THE LAYERS IN THE TANDEM CELL
C ND1,P1,PP1,NP2,P2,PP2= DOPING CONCENTRATION IN EACH LAYER
C LN1,LP1= DIFFUSION LENGTH IN THE P AND N REGION OF THE FIRST CELL
C LN2,LP2= DIFFUSION LENGTH IN THE P AND N REGION OF THE SECOND CELL
C SN1,SN2,SP1,SP2= RECOMBINATION VELOCITIES OF THE P+ AND N REGIONS
C IN THE FIRST AND SECOND CELLS
C NOTE: THE SN IS THE RECOMBINATION VELOCITY AT THE BACK OF THE P+
C REGION - THE BACK SURFACE FIELD IS INCLUDED BY CONVERTING SN TO
C S IN THE PROGRAM
C TO SPECIFY S(EFF), SET SN1 ACCORDING TO
C S(EFF)= SN1*P1/PP1
C DN1,DN2,DP1,DP2= DIFFUSION CONSTANTS OF THE P AND N REGIONS
C IN THE FIRST AND SECOND CELLS
C
C THE INPUTS ARE THE WIDTH OF THE TOP N LAYER = XN1, THE FIRST
C GUESS AT THE WIDTH OF THE TOP P LAYER = XP1, THE WIDTH OF THE
C P+ LAYER = XPP1, THE WIDTH OF THE BOTTOM N LAYER = XN2, THE
```

C WIDTH OF THE BOTTOM P+ LAYER = XPP2, AND THE TOTAL WIDTH OF THE
C CELL = XTOT.

C
 READ (9,10) XN1,XP1,XPP1,XN2,XPP2,XTOT
 READ (9,10) ND1,P1,PP1,NP2,P2,PP2
 READ (9,15) LN1,LN2,LF1,LP2
 READ (9,15) SN1,SN2,SP1,SP2
 READ (9,15) DN1,DN2,DP1,DP2
 READ (9,10) NI,TN01,TP01,TN02,TP02,DUM
 READ (9,15) W1,W2

C
 NEND = 101
 READ (10,25) (F(J),J=1,NEND)
 READ (11,25) (ALPHA(J),J=1,NEND)
 READ (12,25) (R(J),J=1,NEND)

25 FORMAT (E15.3)
 Q = 1.6E-19
 KT = .026

C ASSUME WIDTH OF P+ IS << DIFFUSION LENGTH, SO EXPRESSION FOR
C THE EFFECTIVE SURFACE RECOMBINATION VELOCITY SIMPLIFIES
 S1 = SN1*P1/PP1
 S2 = SN2*P2/PP2

C
C SET UP THE PARAMETERS FOR THE FUNCTION TO FIND THE ZERO
C THE SUBROUTINE ZBRENT IS IN THE INSL LIBRARY

C
 EPS = 1.0E-6
 NSIG = 6
 C = .3
 L1 = 0
23 A = (1.-C)*XP1
 B = (1.+C)*XP1
 MAXFN = 10
C
 CALL ZBRENT(DIFFJ,EPS,NSIG,A,B,MAXFN,IER)

C
C RECALCULATE THE SIZES WITH OUTPUT FROM ZBRENT
C

 XP1 = B
 X2 = XN1 + XP1
 X3 = X2 + XPP1
 X4 = X3 + XN2
 XP2 = X5 - X4
C
10 FORMAT (6E12.3)
12 FORMAT (6(1PE12.3))
15 FORMAT (4E12.3)

C
 IF (IER .NE. 0) GO TO 599
 WRITE (6,100)
 WRITE (13,100)
100 FORMAT (/ ' THESE RESULTS COMPUTED USING TAN8. ')
 WRITE (6,101) MAXFN
 WRITE (13,101) MAXFN

```

101  FORMAT (/ ' THE FUNCTION HAS CONVERGED IN ',I3,' ITERATIONS.')
      WRITE (6,103) B
      WRITE (13,103) B
103  FORMAT ( ' THE VALUE OF XP1 IS ',4PF8.3,' MICRONS.')
      WRITE (6,105) J1
      WRITE (13,105) J1
105  FORMAT ( ' THE SHORT CIRCUIT CURRENT IS ',3PF8.2,' MILLIAMPS.')
      DIFF = DIFFJ(B)
      WRITE (6,107) DIFF
      WRITE (13,107) DIFF
107  FORMAT ( ' THE DIFFERENCE IN CURRENTS IS ',6PF8.2,' MICROAMPS.')
      WRITE (6,110)
110  FORMAT (/ ' JN1(J)',6X,'JN2(J)',6X,'JP1(J)',6X,'JP2(J)',
$5X,'JDR1(J)',5X,'JDR2(J)')
      DO 300 J=1,NEND
          WRITE (6,10) JN1(J),JN2(J),JP1(J),JP2(J),JDR1(J),JDR2(J)
300  CONTINUE
C
C COMPUTE PARTIAL SUMS FOR THE CURRENTS AND PUT IN THE LAST SLOT.
      JN1(300) = 0.
      JN2(300) = 0.
      JP1(300) = 0.
      JP2(300) = 0.
      JDR1(300) = 0.
      JDR2(300) = 0.
      DO 310 J=1,NEND
          JN1(300) = JN1(300) + JN1(J)
          JP1(300) = JP1(300) + JP1(J)
          JN2(300) = JN2(300) + JN2(J)
          JP2(300) = JP2(300) + JP2(J)
          JDR1(300) = JDR1(300) + JDR1(J)
          JDR2(300) = JDR2(300) + JDR2(J)
310  CONTINUE
C
      JSC1 = 0.0
      JSC2 = 0.0
      DO 200 J=1,NEND
          JSC1 = JSC1 + (JN1(J)+JP1(J)+JDR1(J))/(1. - R(J))
200  JSC2 = JSC2 + (JN2(J) + JP2(J) + JDR2(J))/(1. - R(J))
C IGNORE THE DEPLETION WIDTHS IN CALCULATING THE WIDTHS OF THE LAYERS
C P-REGIONS.
      WN1 = X1
      WN2 = X4-X3
      WP1 = X2-X1
      WP2 = X5-X4
      AJ01 = Q*DP1/LP1*NI**2/ND1*( SP1*LP1/DP1 * COSH(WN1/LP1)
$ + SINH(WN1/LP1)) / ( SP1*LP1/DP1 * SINH(WN1/LP1) + COSH(WN1/LP1))
      AJ02 = Q*DP2/LP2*NI**2/NP2*( SP2*LP2/DP2 * COSH(WN2/LP2)
$ + SINH(WN2/LP2)) / ( SP2*LP2/DP2 * SINH(WN2/LP2) + COSH(WN2/LP2))
      BJ01 = Q*DN1/LN1*NI**2/P1*( S1*LN1/DN1 * COSH(WP1/LN1)
$ + SINH(WP1/LN1)) / ( COSH(WP1/LN1) + S1*LN1/DN1 * SINH(WP1/LN1))
      BJ02 = Q*DN2/LN2*NI**2/P2*( S2*LN2/DN2 * COSH(WP2/LN2)
$ + SINH(WP2/LN2)) / ( COSH(WP2/LN2) + S2*LN2/DN2 * SINH(WP2/LN2))
      J01 = AJ01 + BJ01

```

```

J02 = AJ02 + BJ02
FB = ATAN(1.)*2.
A1 = Q*NI*W1/SQRT(TN01*TP01)*2.*FB
A2 = Q*NI*W2/SQRT(TN02*TP02)*2.*FB
B1 = ALOG(P1*ND1/NI**2)
B2 = ALOG(P2*NP2/NI**2)
NV = 80
DO 400 J=1,NV
  V(J)= J/100.
  C = EXP(V(J)/KT)- 1.
  JINJ1(J) = J01 * C
  JINJ2(J) = J02 * C
  JRG1(J) = A1*SINH(V(J)/(2.*KT)) / (B1-V(J)/KT)
  JRG2(J) = A2*SINH(V(J)/(2.*KT)) / (B2-V(J)/KT)
  IOUT1(J) = JSC1-JINJ1(J)-JRG1(J)
  IOUT2(J) = JSC2-JINJ2(J)-JRG2(J)
  POUT1(J) = IOUT1(J)*V(J)
400  POUT2(J) = IOUT2(J)*V(J)
  WRITE (6,1101)
1101  FORMAT (/ '      V(J)',10X,'IOUT1(J)',8X,'POUT1(J)',8X,'IOUT2(J)',
$8X,'POUT2(J)')
  DO 500 J=1,NV
    WRITE (6,501) V(J),IOUT1(J),POUT1(J),IOUT2(J),POUT2(J)
500  CONTINUE
501  FORMAT (5E15.6)
C
C COMPUTE DERIVATIVE OF IOUT2
C
  DO 600 J=1,NV
    DERIV(J) = -(JINJ2(J)+J02)/KT - (A2*COSH(V(J)/(2.*KT))
$    + 2.*JRG2(J))/(2.*KT*(B2-V(J)/KT))
600  CONTINUE
C
  CALL MATCH(IOUT1,IOUT2,DERIV,V,Z,NV,IERR)
C
  IF (IERR .EQ. 2) WRITE (6,605)
605  FORMAT (' SOME VALUES OF Z WERE NEGATIVE WHEN COMPUTED')
C CHECK THE LINEAR INTERPOLATION
C IF Z(J) IS TOO LARGE THE RESULTING CURRENT IS TOO LARGE AND
C THE PROGRAM CRASHES. I WILL SET THE VALUES TO 0.0 IF Z(J)/KT IS
C GREATER THAN 100.
  L = 0
  DO 645 J=1,NV
    ZTEST = Z(J)/KT
    IF (ZTEST .LT. 100) GO TO 645
    L = 1
    Z(J) = 0.0
645  CONTINUE
  IF (L .NE. 1) GO TO 649
  WRITE (6,647)
647  FORMAT (' SOME OF THE VALUES OF Z(J) WERE TOO LARGE.')

```

```

C
649  WRITE (6,650)
650  FORMAT (/ '      V(J)',10X,'IOUT1(J)',8X,'I2CHK(J)',8X,'  Z(J)',
$8X,'P(J)')
      DO 700 J=1,NV
          I2CHK(J) = JSC2-J02*(EXP(Z(J)/KT)-1.) -
$              A2*SINH(Z(J)/(2.*KT))/(B2-Z(J)/KT)
700  CONTINUE
C
C  FIND THE POWER OUTPUT FOR EACH CURRENT
C
      DO 800 J=1,NV
          VTOT = V(J) + Z(J)
          P(J) = IOUT1(J)*VTOT
          WRITE (6,810) V(J),IOUT1(J),I2CHK(J),Z(J),P(J)
810  FORMAT (5F15.6)
800  CONTINUE
C
      PMAX = 0.0
      DO 900 J=1,NV
          IF (P(J) .LT. PMAX) GO TO 900
          K = J
          PMAX = P(J)
900  CONTINUE
      VMAX = V(K) + Z(K)
      IMAX = IOUT1(K)
      ETA = PMAX*1000./135.
C
C  FIND THE OPEN CIRCUIT VOLTAGE AND FILL FACTOR
C
      DO 930 J=1,NV
          IF (IOUT1(J) .LT. 0.0) GO TO 940
930  CONTINUE
          WRITE (6,935)
          WRITE (13,935)
935  FORMAT (/ ' NO ZERO OF CURRENT FOUND. INCREASE NV. ')
          STOP
940  K = J-1
          SLOPE1 = (V(J)-V(K))/(IOUT1(J)-IOUT1(K))
          VOC1 = V(J) - SLOPE1*IOUT1(J)
          DO 950 J=1,NV
              IF (IOUT2(J) .LT. 0.0) GO TO 960
950  CONTINUE
              WRITE (6,935)
              WRITE (13,935)
              STOP
960  K = J-1
          SLOPE2 = (V(J)-V(K))/(IOUT2(J)-IOUT2(K))
          VOC2 = V(J) - SLOPE2*IOUT2(J)
          VOC = VOC1 + VOC2
          FF = PMAX/(VOC*JSC1)
C
C  WRITE OUTPUT
C

```



```

WRITE (6,38) XN1,XP1,XPP1
WRITE (6,39) XN2,XP2,XPP2
WRITE (6,40) X1,X2,X3
WRITE (6,41) X4,X5,X6
WRITE (6,12) ND1,P1,PP1,NP2,P2,PP2
WRITE (6,42) LN1,LP1,LP2
WRITE (6,43) SN1,SN2,SP1,SP2
WRITE (6,44) DN1,DP1,DP2
WRITE (6,45) TN01,TP01,TN02,TP02
WRITE (6,46) NI,W1,W2

```

C

```

WRITE (13,38) XN1,XP1,XPP2
WRITE (13,39) XN2,XP2,XPP2
WRITE (13,40) X1,X2,X3
WRITE (13,41) X4,X5,X6
WRITE (13,12) ND1,P1,PP1,NP2,P2,PP2
WRITE (13,42) LN1,LP1,LP2
WRITE (13,43) SN1,SN2,SP1,SP2
WRITE (13,44) DN1,DP1,DP2
WRITE (13,45) TN01,TP01,TN02,TP02
WRITE (13,46) NI,W1,W2

```

C

```

38  FORMAT (/ ' XN1 = ',4PF9.4,' XP1 = ',4PF9.4,' XPP1 = ',4PF9.4,
    $' MICRONS')
39  FORMAT (' XN2 = ',4PF9.4,' XP2 = ',4PF9.4,' XPP2 = ',4PF9.4,
    $' MICRONS')
40  FORMAT (' X1 = ',4PF8.4,' X2 = ',4PF8.4,' X3 = ',4PF8.4,
    $' MICRONS')
41  FORMAT (' X4 = ',4PF8.4,' X5 = ',4PF8.4,' X6 = ',4PF8.4,
    $' MICRONS')
42  FORMAT (/ ' LN1 = ',4PF6.2,' LN2 = ',4PF6.2,' LP1 = ',4PF6.2,
    $' LP2 = ',4PF6.2,' MICRONS')
43  FORMAT (' SN1 = ',1PE9.2,' SN2 = ',1PE9.2,' SP1 = ',1PE9.2,
    $' SP2 = ',1PE9.2,' CM/S')
44  FORMAT (' DN1 = ',1PE9.2,' DN2 = ',1PE9.2,' DP1 = ',1PE9.2,
    $' DP2 = ',1PE9.2,' CM*CM/S')
45  FORMAT (' TN01 = ',6PF6.2,' TP01 = ',6PF6.2,
    $' TN02 = ',6PF6.2,' TP02 = ',6PF6.2,' MICSEC')
46  FORMAT (' NI = ',1PE9.2,'CM-3', ' W1 = ',4PF7.3,' MICRONS. ',
    $'W2 = ',4PF7.3,' MICRONS.')

```

C

```

WRITE (6,30) J01,J02
WRITE (13,30) J01,J02
WRITE (6,35) JSC1,JSC2
WRITE (13,35) JSC1,JSC2
30  FORMAT (/ ' J01 = ',1PE15.5,' J02 = ',1PE15.5,' AMPS')
35  FORMAT (' JSC1 = ',1PE15.5,' JSC2 = ',1PE15.5,' AMPS')
WRITE (6,36) JN1(300),JP1(300),JDR1(300)
WRITE (13,36) JN1(300),JP1(300),JDR1(300)
WRITE (6,37) JN2(300),JP2(300),JDR2(300)
WRITE (13,37) JN2(300),JP2(300),JDR2(300)
36  FORMAT (/ ' JN1 = ',1PE15.5,' JP1 = ',1PE15.5,' JDR1 = ',
    $1PE15.5)

```

```

37  FORMAT (' JN2 = ',1PE15.5,' JP2 = ',1PE15.5,' JDR2 = ',
      $1PE15.5)
      WRITE (6,910) PMAX,ETA,VMAX,IMAX
      WRITE (13,910) PMAX,ETA,VMAX,IMAX
910  FORMAT (/ ' THE MAXIMUM POWER IS ',3PF8.3,' MILLIWATTS/CM/CM'
      $/ ' THE EFFICIENCY IS ',2PF6.2,' %, FOR P(INCIDENT)=135MW/CM/CM',
      $/ ' THE OUTPUT VOLTAGE IS ',OPF8.3,' VOLTS AND THE CURRENT',
      $' IS ',3PF8.3,' MILLIAMPS'/)
      WRITE (6,915) VOC,VOC1,VOC2,FF
      WRITE (13,915) VOC,VOC1,VOC2,FF
915  FORMAT (/ ' THE OPEN CIRCUIT VOLTAGE IS ',F6.3,' VOLTS.',
      $/ ' THE TOP CELL CONTRIBUTES ',F6.3,' VOLTS AND THE BACK ',
      $' CELL CONTRIBUTES ',F6.3,' .',
      $/ ' THE FILL FACTOR IS ',F6.3,' .'/)
C
      STOP
C
599  IF (IER .EQ. 129) GO TO 610
      IF (IER .EQ. 130) GO TO 630
      WRITE (6,601)
      WRITE (13,601)
601  FORMAT (' THE ERROR MESSAGE FROM THE SUBROUTINE IS UNKNOWN.')
      STOP
610  WRITE (6,611) MAXFN, B
      WRITE (13,611) MAXFN,B
611  FORMAT (' THE FUNCTION DID NOT CONVERGE IN ',I3,' ITERATIONS.'
      $/ ' THE LAST GUESS FOR XP1 WAS ',4PF8.3,' MICRONS')
      STOP
630  WRITE (6,631) A,B
      WRITE (13,631) A,B
631  FORMAT (' THE INTERVAL DOES NOT INCLUDE THE ZERO.'/
      $' IT WAS: A =A',4PF8.3,' AND B = ',4PF8.3,' MICRONS.')
      C = 0.9
      IF (L1 .EQ. 1) STOP
      L1 = 1
      GO TO 23
      END
C
      SUBROUTINE MATCH(Y1,Y2,DERIV,X,Z,N,IERR)
      DIMENSION Y1(300), Y2(300), DERIV(300), X(300), Z(300)
C
C  THIS SUBROUTINE ACCEPTS ARRAYS Y1,Y2,AND DERIV WHICH ARE COMPUTED
C  FOR THE RANGE OF VALUES IN ARRAY X.  FOR EACH Y1(X(J)) IT FINDS THE
C  VALUE OF Y2(X(K)) CLOSEST TO Y1(X(J)).  THEN IT COMPUTES A LINEAR
C  INTERPOLATION BETWEEN THE Y2 VALUES TO FIND THE VALUE OF X
C  SUCH THAT Y2(X)=Y1(X(J)).  IT PUTS THAT VALUE IN POSITION Z(J).
C
      IF (N .GT. 300) GO TO 999
      IERR = 0
C
      DO 100 J=1,N
          K = 1
          DIFF = ABS(Y2(1)-Y1(J))

```

```

      DO 200 I=1,N
        IF (ABS(Y2(I)-Y1(J)) .GT. DIFF) GO TO 200
        DIFF = ABS(Y2(I)-Y1(J))
        K = I
200    CONTINUE
        Z(J) = (Y1(J)-Y2(K)+X(K)*DERIV(K))/DERIV(K)
        IF (Z(J) .GE. 0.) GO TO 100
        Z(J) = 0.0
        IERR = 2
100    CONTINUE
        RETURN
999    WRITE (6,1000)
1000   FORMAT ('N MUST BE LESS THAN 301')
        IERR = 1
        RETURN
      END

C
C  DEFINE THE FUNCTION DIFFJ WHICH COMPUTES THE DIFFERENCE IN THE
C  CURRENTS OF THE TWO CELLS.
C
      FUNCTION DIFFJ(XP1)
C
      REAL JN1,JN2,JP1,JP2,JDR1,JDR2
      REAL ND1,NP2,KT,NI
      REAL LN1,LN2,LP1,LP2
      REAL J1,J2,JSC1,JSC2,J01,J02,JRG1,JRG2
      REAL JINJ1,JINJ2,IOUT1,IOUT2,I2CHK,IMAX
C
      COMMON/JOUT/JN1(300),JN2(300),JP1(300),JP2(300),JDR1(300),
$JDR2(300),JRG1(300),JRG2(300),JINJ1(300),JINJ2(300),J1,J2
      COMMON/DATA/ F(300),ALPHA(300),R(300)
      COMMON/OUTPUT/ V(300),IOUT1(300),IOUT2(300),POUT1(300),
$POUT2(300), DERIV(300), I2CHK(300), Z(300),P(300)
      COMMON/SIZE/XN1,XN2,XPP1,XPP2,XTOT,X1,X2,X3,X4,X5,X6,XP2
      COMMON/DOPING/ ND1,P1,PP1,NP2,P2,PP2
      COMMON/LS/LN1,LN2,LP1,LP2,SN1,SN2,SP1,SP2,S1,S2
      COMMON/D/DN1,DN2,DP1,DP2,Q,KT,NEND,W1,W2
C
C  NOTE THAT THE BACK SURFACE FIELD IS INCLUDED IN THIS
C  CALCULATION VIA THE CHANGE FROM SN TO S IN THE MAIN
C  PROGRAM
C
      J1 = 0.0
      J2 = 0.0
      X1 = XN1
      X2 = XN1 + XP1
      X3 = X2 + XPP1
      X4 = X3 + XN2
      X5 = XTOT - XPP2
      X6 = XTOT
      XP2 = X5 - X4
      H1= XP1 - W1
      H2= XP2 - W2

```

```

DO 200 J=1,NEND
  TEST1= ALPHA(J)*X1
  IF (TEST1 .GT. 100.) TEST1= 100.
  TEST2= ALPHA(J)*(X1+W1)
  IF (TEST2 .GT. 100.) TEST2=100.
  TEST3= ALPHA(J)*H1
  IF (TEST3 .GT. 100.) TEST3= 100.
  TEST4= ALPHA(J)*W1
  IF (TEST4 .GT. 100.) TEST4= 100.
  TEST5= ALPHA(J)*X3
  IF (TEST5 .GT. 100.) TEST5= 100.
  TEST6= ALPHA(J)*XN2
  IF (TEST6 .GT. 100.) TEST6= 100.
  TEST7= ALPHA(J)*H2
  IF (TEST7 .GT. 100.) TEST7= 100.
  TEST8= ALPHA(J)*(XN2+W2)
  IF (TEST8 .GT. 100.) TEST8= 100.
  TEST9= ALPHA(J)*W2
  IF (TEST9 .GT. 100.) TEST9= 100.
  JP1(J)=Q*F(J)*(1.-R(J))*ALPHA(J)*LP1/(ALPHA(J)**2*LP1**2-1.)*
$*((SP1*LP1/DP1+ALPHA(J)*LP1-EXP(-TEST1)*(SP1*LP1/DP1*COSH(X1/LP1)
$+SINH(X1/LP1)))/(SP1*LP1/DP1*SINH(X1/LP1)+COSH(X1/LP1))
$-ALPHA(J)*LP1*EXP(-TEST1))
  JN1(J)=Q*F(J)*(1.-R(J))*ALPHA(J)*LN1/(ALPHA(J)**2*LN1**2-1.)*
$EXP(-TEST2)*(ALPHA(J)*LN1-(S1*LN1/DN1*(COSH(H1/LN1)
$-EXP(-TEST3))+SINH(H1/LN1)+ALPHA(J)*LN1*EXP(-TEST3))
$/(S1*LN1/DN1*SINH(H1/LN1)+COSH(H1/LN1)))
  JDR1(J)=Q*F(J)*(1.-R(J))*EXP(-TEST1)*(1.-EXP(-TEST4))
  FP= F(J)*EXP(-TEST5)
  IF (FP .LT. 1.E-5) FP= 0.
  JP2(J)=Q*FP*(1.-R(J))*ALPHA(J)*LP2/(ALPHA(J)**2*LP2**2-1.)*
$(((SP2*LP2/DP2+ALPHA(J)*LP2)-EXP(-TEST6)*(SP2*LP2/DP2*
$COSH(XN2/LP2)+SINH(XN2/LP2)))/(SP2*LP2/DP2*SINH(XN2/LP2)
$+COSH(XN2/LP2))-ALPHA(J)*LP2*EXP(-TEST6))
  JN2(J)=Q*FP*(1.-R(J))*ALPHA(J)*LN2/(ALPHA(J)**2*LN2**2-1.)*
$EXP(-TEST8)*(ALPHA(J)*LN2-(S2*LN2/DN2*(COSH(H2/LN2)
$-EXP(-TEST7))+SINH(H2/LN2)+ALPHA(J)*LN2*EXP(-TEST7))
$/(S2*LN2/DN2*SINH(H2/LN2)+COSH(H2/LN2)))
  JDR2(J)= Q*FP*(1.-R(J))*EXP(-TEST6)*(1.-EXP(-TEST9))
  J1= J1+JN1(J)+JP1(J)+JDR1(J)
  J2= J2+JN2(J)+JP2(J)+JDR2(J)
200 CONTINUE
  DIFFJ = J1 - J2
  RETURN
  END

*RUN
//GO.FT09F001 DD DISP=SHR,DSN=EPP5PDS.INPUT
//GO.FT10F001 DD DISP=SHR,DSN=EPP5PDS.F
//GO.FT11F001 DD DISP=SHR,DSN=EPP5PDS.ALPHA
//GO.FT12F001 DD DISP=SHR,DSN=EPP5PDS.R
//GO.FT13F001 DD DISP=OLD,DSN=EPP5PDS.OUTTAN
//

```

END