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Summary

The preliminary results of a development program to minimize beam perturbation resulting from ripple current generated by the CBA Main Magnet Power Supply are presented. The assessment of the magnitude and causes of the ripple generated led to a modification of the SCR Gate Driver and the addition of a bandpass amplifier correction loop which gave significant improvement. A description of the changes made and the results obtained are included. A second design approach was developed in which the timing of the SCR gate pulses is directly determined by a VCO. The results reported with this VCO Loop indicate superior performance particularly at frequencies below 60 Hz. A shunt transistor regulator design is proposed to minimize higher SCR switching frequency harmonics.

Introduction

The 5 KA, 50V power supplies built by NWL Transformers of New Jersey as prototypes of the CBA Main Magnet Power Supply (MMPS) generate an unacceptable amount of ripple current at sub-harmonics of 720 Hz, the basic switching frequency, and other random variations. This ripple can drive the beam into magnetic nonlinearities and cause undesirable beam-beam interaction.

In the 1st cell test application of the power supply shown in Figure 1, the output of the SCR bridges was applied to a passive filter and then to a .36 H_y superconducting magnet load via quench protection circuitry. The current was sensed by a highly accurate DCCT. The DCCT output was compared with a DAC reference to form the input to a high gain amplifier A_R whose output was applied directly to the SCR Gate Driver (H and G₁ were not used). The A_R constants were chosen to give a unity gain at 5 Hz and DC loop gain of 10⁵, thus it had no effect on frequencies of 60 Hz and above which are of interest. The SCR Gate Driver, G₂, was composed of two parallel

6 pulse FPE-602 modules which were found to contribute to the random variations and the observed subharmonic ripple. Ripple component magnitudes relative to the output current were as high as 140×10^{-7} at 180 Hz at 3000 Adc. The root-sum-squared of the 60 Hz to 480 Hz ripple components was 203×10^{-7} compared to the 1×10^{-7} which is required.⁸

FPE-602 Problems

The FPE-602 SCR driver provides no means for correction of individual SCR gate drive pulse timing to enable compensation for transformer errors and/or voltage imbalance. Any timing correction required can only be accomplished by dynamic modulation of the input control voltage through some feedback control system...The SCR gate is driven each cycle by a train of 30 μ sec pulses at a 14 KHz rate. These pulses are generated by a 555 astable multivibrator and gated through logic to the driver output. The initial pulse in the train is generated by applying an added trigger to the 555 at the required time. However, the means of triggering results in a random 0.5° jitter in the output...Instead of a 3 ϕ reference input with its zero crossing detection problems, the module uses a 1 ϕ , 60 Hz reference into a phase locked loop (PLL) from which 3 ϕ ramp voltages are eventually generated. The PLL includes a phase comparator (PC2) and a voltage controlled oscillator (VCO) and A₄, a ring counter.¹ However, the choice of PC2 filter components and the frequency determining resistors of the VCO do not follow the standard practice and resulted in time and temperature instability and consequently output pulse changes.

SCR Driver III

For the reasons above and others it was decided to build a modified version of the FPE-602 which would more closely meet our needs. The modified SCR gate pulse generator system, SCR Driver III, includes a modified PLL which develops all (12) 60 Hz wave-

Figure 1. MMPS Equip. Ckt., 1st Cell

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The preliminary results of a development program to minimize beam perturbation resulting from ripple current generated by the CEA Main Magnet Power Supply are presented. The assessment of the magnitude and causes of the ripple generated led to a modification of the SCR Gate Driver and the addition of a bandpass amplifier correction loop which gave significant improvement. A description of the changes made and the results obtained are included. A second design approach was developed in which the timing of the SCR gate pulses is directly determined by a VCO. The results reported with this VCO Loop indicate superior performance particularly at frequencies below 60 Hz. A shunt transistor regulator design is proposed to minimize higher SCR switching-frequency harmonics.

The 5 KA, 50V power supplies built by NWL Transformers of New Jersey as prototypes of the CBA Main Magnet Power Supply (MMPS) generate an unacceptable amount of ripple current at sub-harmonics of 720 Hz, the basic switching frequency, and other random variations. This ripple can drive the beam into magnetic nonlinearities and cause undesirable beam-beam interaction.

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6 pulse FPE-602 modules which were found to contribute to the random variations and the observed subharmonic ripple. Ripple component magnitudes relative to the output current were as high as 140×10^{-7} at 180 Hz at 3000 Adc. The root-sum-squared of the 60 Hz to 480 Hz ripple components was 203×10^{-7} compared to the 1×10^{-7} which is required.⁸

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For the reasons above and others it was decided to build a modified version of the FFE-6C2 which would more closely meet our needs. The modified SCR gate pulse generator system, SCR Driver III, includes a modified PLL which develops all (12) 60 Hz wave-

Figure 1. MMPS Equiv. Ckt., 1st Cell

*Work performed under the auspices of the U.S. Department of Energy.

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forms required. In the modified configuration, the natural frequency, ω_n , and damping factor, ξ , of the PLL can be adjusted by varying the constants of loop. Values of $\omega_n = 10 \text{ rad/sec}$ and $\xi = 0.8$ minimize PLL jitter.^{2,3} The mistrigging of the 555 multivibrator was corrected and control potentiometers were added to select a static correction voltage to be applied to the phase comparator input to correct for transformer unbalance and other system offsets. Other minor improvements were also made.

Preliminary tests were conducted with SCR Driver III installed in a prototype of the CBA flattop MMPS with a warm inductive load replacing the superconducting magnet of Figure 1. The results are shown in Table I along with the results of other approaches described below.

Correction Loops

Static correction for system errors is inadequate to minimize subharmonic output ripple components because as the current level changes, spectrum analysis of the output current indicates a wide variation in the amplitudes of these frequency components. Significant long term changes also occur from day to day for reasons as yet undetermined. A dynamic correction loop is therefore required if ripple in this frequency region is to be minimized. However, it has been amply shown by others that, given a 12 pulse controlled rectifier system with a basic 720 Hz switching frequency, the 360 Hz component cannot be reduced by shifting of the SCR triggering point. Difficulties can also arise when correction of the 180 Hz and 240 Hz components is attempted.^{4,5}

A tuned amplifier correction loop was developed which closely parallels the work done by Yarema.⁴ H in Figure 1 becomes a parallel system of bandpass amplifiers for which $Q = 15$. An active filter circuit utilizing a current inversion negative impedance converter (INIC) is used for the bandpass amplifier simplifying the problems of component selection, stability and tuning. Three such parallel bandpass amplifiers with center frequencies of 60, 120 and 180 Hz were assembled. Each of these can be switched in or out. The assembly also includes a d.c. amplifier, G_1 , with gain between -10db and +7db. The magnitude of the loop gain of the system nominally rises to +22db at the center frequencies. Loop phase shift is between $\pm 90^\circ$ in the frequency region of interest. With this configuration, the low frequencies are greatly reduced, however, the ripple reduction does not vary linearly with G_1 . A type of intermodulation distortion develops in the phase comparator when the correction signal component is large which also increases the 360 Hz component. If the 180 Hz amplifier is not used as in Table I this effect is minimized.

VCO Loop

An alternate design strategy which attempts to more directly zero the time averaged integral of the output voltage error at triggering instants is the voltage controlled oscillator loop or phase-locked oscillator system described by Ainsworth.⁶ A modification of this strategy was also used at CERN.⁷

The basic components of the control circuit are shown in Figure 2. The voltage controlled oscillator (VCO) generates a train of pulses at a frequency f_1 , which is dependent on a control voltage v_F . With $v_F = 0$, the VCO is adjusted to make $f_1 = 12f_0$ where f_0 is the nominal a.c. line frequency. Thus $f_1 = K_V v_F + 12f_0$ where K_V is a constant of the oscillator. The oscillator drives a 12 stage ring counter and each

counter stage output is gated through logic directly to the pulse generator which drives the appropriate SCR gate. The SCR trigger frequency is then $f(t) = f_0 + K_V v_F(t)/12$. The SCR output is $v_D \sin \alpha$ ($0 < \alpha < \pi$) where E_m is the peak line-line voltage of the bridge input, α is the SCR trigger phase delay and neglecting commutation. If $\theta = \pi/2 - \alpha$, $v_D = -E_m \sin \theta$ for $-\pi/2 < \theta < \pi/2$. The trigger phase angle, $\theta(t)$, decreases as $f(t)$ increases thus

$$\theta(t) = -2\pi \int f(t) dt = -2\pi \int \left(f_0 + \frac{K_V v_F(t)}{12} \right) dt$$

$$\theta(s) = -\frac{2\pi f_0}{s} - \frac{2\pi K_V}{12} \frac{v_F(s)}{s} = \frac{\theta_0}{s} + \theta_e(s)$$

The first term synchronizes the system to the nominal ac line frequency. By generating v_F from the amplified difference between the output of the SCR bridge, v_D , and the reference, v_R , the second term automatically adjusts to just that value required to make $f(t)$ equal actual line frequency and α (or θ) the value required to make the average value of $v_D/B = v_R$. A change in load or line voltage or line frequency causing a change in v_D results in θ correction to correct v_D . In the phase angle limit stop logic, square waves related to the ac line voltage zeros gate the counter output pulses to the appropriate pulse generator only in the correct half cycle of the ac line voltage. After the positive transition of the counter output which results in an initial SCR drive pulse, the logic passes a 1.4 msec train of 15 KHz SCR pulses to insure SCR turn on.

Figure 2. VCO Loop Block Diagram

$$\frac{v_D}{v_R} = \frac{1/H(s)}{1 + 1/G(s)H(s)} = \frac{B}{1 + \left(\frac{12}{2\pi K_V} \right) \left(\frac{R}{Z_F} \right) \left(\frac{B}{E_m} \right) s}$$

For $Z_F = 1.35 R$, $K_V = 188 \text{ Hz/V}$, $E_m = 27 \text{ V}$, $B = 4$

$$\frac{v_D}{v_R} = \frac{B}{1 + \tau s} = \frac{4}{1 + (1.11 \text{ msec}) s}$$

Figure 3. Small Signal VCO Loop equiv; $v_D \approx -E_m \theta$

The system was built and tested and it was found that at turn-on the loop locks into any output voltage within the range of the peak rectifier output without difficulty. The transient response is controlled by the A3 feedback network. Various networks were used, but optimum response was obtained with simple resistive feedback; the system then recovers from a 5% transient impulse within 1.4 msec. With the loop parameters of Figure 3, the loop is unconditionally stable. Operation at $T < 1.0$ msec causes growth in the 360 Hz ripple; at higher values of T , the lower frequencies are not controlled. Bandpass amplifier feedback from v_p to modify the reference voltage, v_r , was used to further reduce the 60 Hz and 120 Hz ripple. See Table I. The VCO Loop also does not exhibit the random output variations at frequencies below 60 Hz which is characteristic of both the systems discussed above. The data of Table II which demonstrates this was obtained by amplifying the DCCT output at frequencies below 60 Hz and chart recording the zero suppressed result at a sensitivity of 35 mV/mm. This VCO Loop characteristic is due to the fact that trigger pulse timing is more directly locked to line voltage frequency and phase to phase changes. Thus its output is virtually free of variation with line voltage perturbation. The ramp generator-comparator and the required balancing of the former system are eliminated and there are other simplifications as well. As a result this approach seems to have more possibilities than the approaches discussed above.

Active Shunt Filter

To reduce the current ripple at 360 Hz and 720 Hz either penalties must be paid to change the passive output filter, or some sort of active filter after the passive filter is required. Depending on the operating level various active filter approaches have been used. Given the ac currents through the filter inductance of the order of 10A rms or less in the frequency region of interest and the relatively low dc output voltage which we have in this case, a transistor shunt regulator across the line is the simplest solution.

Such a regulator was designed and built which is driven by the amplified ripple voltage from the output node of the power supply. An SCR is used in series with the transistor bank to protect against reverse voltage failure which might occur when the output current is interrupted in the event of a quench of the superconducting load. The (12) 50A transistors are operated well below ratings with redundant overcurrent protection. The frequency response of the direct coupled driving amplifier can be adjusted to give the desired overall filter response. The design attenuation of the 360 Hz and 720 Hz ripple components should approach 40db.

Conclusion

An important finding of this study is the large sub-60 Hz variations which can occur in SCR power supply systems and the degree to which this can be reduced with the VCO Loop described above which is phase locked to the input line frequency. These low frequency perturbations can cause large field errors in accelerator magnets if not corrected. Dynamic bandpass amplifier loop correction of SCR gate pulses appears to be the best way to minimize 50, 120 and 180 Hz ripple. An active shunt filter operating on the power supply output filter impedance was developed to reduce the higher frequency output ripple current. Some combination of these approaches can be used to meet the ripple performance required for the full CBA magnet current or for small scale test applications.

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Table I
5 KA, 50V MMPS, 18D36 Load (30 mhy, 35 m²)
(HP 3580A Spectrum Analyzer)

Conditions	I _o (ADC)	Load 60 Hz	Ripple 120 Hz	Components (mA rms) 180 Hz	360 Hz
Baseline:	300	50-60	80	10	20
FPE-602	600	30	50	10	15
SCR Drives, no feedback.	1200	20-30	65	5-10	32
Drvr III:	300	92	26	5	10
Equal firing	600	80-85	45-50	2	15
intervals.	1200	55	73	9	35
Drvr III:	300	<5	1	10	22
60, 120 Hz	600	<5	2	4	19
bandpass amp, 1200		<5	5	11	43
GH=22db max.					
VCO Loop:	300	<3	19	4	26
R _f =8.7K.	600	<5	39	7	17
f _c =140Hz.	1200	<10	68	4	40
VCO Loop:	300	<5	3	5	21
60, 120 Hz.	600	<5	5	8	14
amp feedback.	1200	<8	10	5	43

Table II

	I _o (ADC)	Sub-60 Hz Current Jitter (mApp)		
		4 sec	5 min. (max Spike)	5 min. (95%)
Baseline:	300	1140	1210	1140
FPE-602	600	350	550	450
SCR Drives	1200	450	1180	700
Drvr II:	300	100	280	140
w/or w/o	600	140	845	200
bandpass amp	1200	160	830	280
feedback				
VCO Loop:	300	10	15	15
w/or w/o	650	10	15	15
bandpass amp	1200	15	15	15

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