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PHASE 2. ARRAY AUTOMATED ASSEMBLY TASK, LOW COST SILICON
SOLAR ARRAY PROJECT

Quarterly Technical Report No. 2, April 1—June 30, 1978

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U.S. Department of Energy

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PREFACE

The information presented in this report, represents the work performed from April 1st, 1978 through June 30th, 1978 by Sensor Technology, Inc., in Chatsworth, California. The program is directed by Sang S. Rhee. Principal contributors include Gregory T. Jones, Kimberly L. Allison, Sanjeev Chitre, Charles Snyder, Louis R. Rosinski, Nelson E. David, and A. PeBenito.

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ABSTRACT

Work on Phase 2 of the Array Automated Assembly Task, a low-cost solar array project, was conducted during this quarter. This project covers the period from April 1, 1978 through June 30, 1978.

Data was gathered and analysis continued on seventeen process groups. Five process groups were completed. They include: solar cell test data acquisition, plasma etching of resist, laser trimming and holing operation, wafer surface preparation and wafer printing. With the exception of plasma etching of thick film resist, the four other process groups listed above have been shown to be on line with the 1986 LSA goals. Work on all other tasks remains in the intermediate stage.

Preliminary results to date show very promising results for other task groups. Silicon nitride anti-reflective coating equipment with modifications has high potential for low-cost automation. An electroless nickel plating system has been designed and is under construction to demonstrate the processing of 1500 wafers per hour. The conceptual design of two fully automated laser trimming and holing lines has been completed and has very promising low-cost, high volume potential. The spray-on dopant model equipment construction is nearly completed. Preliminary spray-on tests have shown very good results. Dopants can be sprayed on without wafer edge overlap and good dopant uniformity can be achieved.

SAMICS has been applied to most process groups. It has been very effective in analyzing process steps for low-cost potential for meeting the LSA 1986 goals. The laser trimming and holing automation task, one of two tasks to be given major emphasis in this program (the second task is spray-on dopants), has concluded from a SAMICS study that the serial flow laserscribe system is far more cost effective than the parallel flow laser-scribe system. Since approximately 90% of the total process cost resides in utility costs alone, a reduction in the overall process cost can occur only with an improvement in laser beam efficiency.

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INTRODUCTION

The automated process sequence is being investigated in seventeen groups. The process groups, which are not in sequential order, each cover a number of process steps. Analysis of each process step will be performed in one of these groups. Each group is discussed in the technical section of this report. A SAMICS report will be made after our analysis of each process group is complete. Data was gathered and analysis continued for seventeen process groups during this quarter. They are discussed below.

TECHNICAL DISCUSSION

1. Cell Test Data Acquisition

All work has been completed for this task. A solar cell test data acquisition system has been fabricated and its feasibility in terms of production line applications has been evaluated and found to comply with previous expectations. This equipment has demonstrated that an automated system for collecting data on solar cell performance is extremely conducive for module assembly.

2. Plasma Etching of Resist

The process of plasma etching of resist has been reviewed and its applicability towards the removal of thick film resist has undergone extensive investigation. The available evidence points conclusively to the fact that the process time for a 5 mil thick resist used throughout the photovoltaic industry will be approximately 40 hours. SAMICS shows that the cost per watt for this process is \$1.02. Detailed calculations are shown in a separate section in this report. In view of this result the application of plasma etching to thick film resist removal does not look promising in the near future and therefore no further study will be undertaken on this task.

3. Laser Trimming and Holing Operation

All work on this task has been completed. A laserscribe computer program has been received and is presently undergoing debugging. A chuck with a circular moat is now being constructed and the expected delivery time is set for next month. A logic board has been fabricated and will be received by the end of next month. A software flow chart and operating procedures manual for the combined hexagon and central hole program is now available.

4. Wafer Surface Preparation

All work has been completed for this task. No additional work on the wafer surface preparation task is planned for the near future, however, if any promising new low-cost production ideas should evolve, they will be pursued for further investigation.

5. Laser Scanning Inspection

In the previous quarter, it had been reported that among the three diverse scanning methods under consideration for usage as a solar cell inspection mechanism on an automated assembly line, the laser scanning method exhibited the highest potential for successful application. This quarter, three systems that utilize the laser scanning technique were identified. A comparative analysis

of the three solar cell inspection systems is scheduled to be performed in the near future. The manufacturers of the above-mentioned scanning systems are as follows:

- (1) Quantronix Corporation
- (2) Jet Propulsion Laboratory
- (3) Advanced Semiconductor Materials

Quantronix Corporation will investigate the possibility of designing a laser scanning system based on the JPL Rejection Criteria No. 5101-21 Revision A. The system presently utilized by JPL will be studied for its applicability towards usage on an automated assembly line. The commercially available Advanced Semiconductor Materials Automatic Surface Inspection System is another potential system which could be used for automated solar cell inspection. The performance evaluation of each individual system has been initiated, however, no conclusive results are available at the present time.

The ASM Automatic Surface Inspection System (ASIS) is an MPU-controlled system that quantitatively measures the defect level present on a highly reflective surface. Primarily designed for application in the semiconductor industry, ASIS automatically monitors wafer surface quality before and after critical processing steps.

The ASIS system incorporates a highly sensitive solid-state detector to collect laser energy that has been scattered by defects such as surface haze, particles, scratches, fingerprints, moisture, hillocks, spikes, and

surface fractures. The laser beam traverses the wafer surface forming an Archimedes spiral, which ensures 100% coverage of wafer surfaces up to 5 inches (12.5 cm) in diameter in 4 seconds. The system compares product wafers against standard or "clean" wafer data stored in memory. This unique capability makes it possible to measure patterned wafers at any process step, up to metallization. This system is equipped with automated cassette loaders and sorting stations with control electronics and software to provide sorting of measured wafers into pre-selected surface quality groups.

The throughput of the ASIS system is currently 900 wafers/hr. which falls short of the projected 1986 pricing goals. This figure can, however, be significantly enhanced by utilizing multitrack systems.

A preliminary cost estimate has been performed for the ASM automatic surface inspection system for the purpose of establishing its cost-effectiveness. The resulting process step cost corresponding to the system was found to be 0.672¢/Watt in terms of 1975 dollars which is low enough to ensure the feasibility of this system for usage in an automated assembly line. In addition, potential equipment modifications designed to enhance the throughput of this system will serve to lower the process costs even further.

The only problem area foreseen at the present moment is the detection of hidden cracks or defects such as

poor solder contacts. This problem area is scheduled for further investigation at the ASM Laboratory next quarter.

6. Wafer Printing

The general review of thick film printing machines conducted during the previous quarter provided the indication that state-of-the-art technology can adequately transform the through-put capability of the current machines to the elevated rate of 7200 wafers/hr. The manufacturers possessing this capability include Presco Division of Affiliated Manufacturing Inc., Universal Instrument Co. and Fursland Division of Hutchinson Industrial Co. For the purpose of obtaining a process cost estimation, the commercially available Fursland Model 33 was chosen since it is an automated version of the equipment currently in use at Sensor Technology, Inc.

The satisfactory completion of the printing process hinges upon the inclusion of a drier system within the framework of the overall system design. In the general case, this drier system is made in accordance with customer specifications since the drying conditions will vary with the type of resist ink used. The resist ink consumption rate obtained by Sensor Technology was utilized in the design and equipment cost estimations for the drier.

A detailed SAMICS cost analysis for this process is presented in a separate SAMICS section in this report. The SAMICS calculation indicates that the printing process

cost accounts for 0.77¢/peak watt and the drying process cost is 0.44¢/peak watt. The total printing process cost thus becomes 1.21 cents/peak watt in terms of 1975 dollars which conforms to the cost standards set forth by the LSA 1986 pricing goals.

7. Low Pressure Vapor Metal Deposition

The original plan devised for this task was formulated exclusively to investigate the deposition of p⁺ copper onto silicon wafers. The low pressure vapor metal deposition of p⁺ copper onto silicon wafers would serve primarily as a back surface field.

Despite the fact that numerous companies were contacted which reportedly possessed the capability of performing low pressure vapor metal depositions, no one has yet been found to have successfully performed p⁺ copper depositions. Consequently, any conclusive results pertaining to the viability of this process will not be available until the constraints imposed by technology and cost have been overcome.

8. Silicon Nitride A.R. Coating

The LFE 8000 system was selected as a potential mechanism for depositing silicon nitride A.R. coatings onto silicon

wafers on the basis of a comparative analysis performed last quarter on commercially available plasma A.R. coating systems. Consequently, a detailed description of the LFE 8000 System will be presented along with the proposed equipment modifications designed to elevate the existing through-put.

a) Description of the LFE 8000 System

The LFE 8000 system is presently being utilized by semiconductor manufacturers to deposit 5000 to 8000A of silicon nitride onto silicon wafers, in order to provide a hermetic encapsulant. A simplified line diagram which delineates the overall system can be found in Figure 1. The LFE 8000 system is composed of a vacuum processing chamber which contains five separate process zones with the wafer receiving 20% of its total film in each zone in a sequential manner. The wafer must pass through a vacuum lock at the entrance to the chamber and exits the chamber through an identical vacuum lock after it has been processed at all five process locations. Upon completion of this procedure, a fully coated wafer will emerge every 120 seconds. This figure incorporates the 60 seconds required for wafer movement through a vacuum lock on the main track as well as the 60 seconds expended for the deposition of 1200A of silicon nitride. The throughput of this system which is therefore 30 wafers per hour, will need to undergo considerable improvement in order to conform to the stipulations set forth by the LSA 1986 pricing goals.

Figure 1. LFE 8000 system for silicon nitride anti-reflective coating.

Since Sensor Technology requires only 800Å of silicon nitride for its present application, the expected deposition time will amount to only 40 seconds using the current deposition rate of 1200Å/minute. By adopting suitable equipment modifications, the 5-stage wafer movement sequence will encompass only 20 seconds, thus resulting in a cost-effective through-put of 300 wafers/hour.

b) Modifications Resulting in an Enhanced Throughput

The primary objective of the proposed modifications is to reduce the cumulative wafer movement time from the current figure of five minutes to a range of approximately 20 seconds. In order to facilitate the fulfillment of this goal, five wafers will be simultaneously deposited; i.e. each wafer will make only one stop within the process chamber instead of the present requirement of five stops. By marching wafers in groups of five into the entry lock, out of the entry lock and into the chamber, out of the chamber and into the exit lock, etc., this should considerably reduce the time required for wafer movements, thereby resulting in an enhanced wafer throughput. The system operation would then break down into the following two time periods:

- (1) Movement of five unprocessed wafers into the entry lock from the sender will take place at the same time five processed wafers are moved out of the exit lock, into the receiver. While this wafer movement

is occurring external to the chamber, wafer depositions will take place within the chamber.

- (2) A sequential movement of the five processed wafers from the process chamber into the exit lock and then movement of the five unprocessed wafers from the entry lock into the process chamber will take place. This process sequence must occur within 20 seconds in order to achieve the goal of a 300 wafers/hour throughput.

The key design modifications which will facilitate an enhanced wafer throughput are as follows:

- (1) The wafer velocity on the process track should be increased and positioning control improved. It is imperative that the wafer velocity on the process track be increased from 2 inches/sec. to 3 inches/sec. This can be achieved by redesigning the vibratory subsystem so that an upper velocity limit is established. Since each wafer must be accurately positioned in the process zone in order to obtain the proper degree of film uniformity, it is necessary to provide a "stop pin" on the process track. The stop-pins retreat into the track during wafer movement and then resurface when the

wafer movement ceases. The wafer movement is controlled by a microprocessor which receives wafer positioning data from the capacitive sensors which are imbedded in the process track. The microprocessor controls the turn-on of the vibratory mechanism and the stop-pins in accordance with the particular timing sequence under consideration and wafer positioning information.

- (2) The wafer transition time through the vacuum locks should be decreased. The transition time of a single wafer from the sender to the vacuum lock and then from the vacuum lock to the process chamber is 30 seconds for the present system. In order to move five wafers through this sequential transition operation within a 40 second time period a new design is required. This new design has a cassette mechanism located within the entry lock (and also the exit lock) allowing for a buffer of five wafers in the "ready" zones, namely, the entry and exit locks. As each wafer moves into the lock lock cassette, the cassette will index up (or down) one notch in preparation for the next wafer until all five wafers are received (or dispatched in the case of the exit lock).

c) Process Costs for the Modified System

The process cost for the modified system has been obtained under the following assumptions:

- (1) The electric power consumption rate will increase by 35% due to the power requirement of the vibratory structure.
- (2) The equipment cost is expected to increase by approximately 35% of the current price due to the addition of a transition buffer system and larger microprocessor unit.
- (3) The material consumption rate is proportional to the deposition rate which will remain identical to that of the current LFE 8000 system.

The resulting process cost calculation is presented in Table 1, where the process cost of the unmodified system is shown for comparison.

d) Verification Test for the A.R. Coating

The performance verification for the silicon nitride A.R. coating process will take place at LFE Corporation in Waltham, Mass. A batch of one-hundred wafer samples have been sent out. No results are available at the present time.

The primary objective of the verification test is to establish the effect of the silicon nitride A.R. coating process on the overall cell efficiency level, in addition to evaluating the film uniformity and process repeatability potential.

Table 1. The 1986 anti-reflective coating process cost
in 1975 cents per peak watt.

	LFE 8000 SYSTEM	MODIFIED LFE SYSTEM
EQUIPMENT	15.02	2.500
FLOOR SPACE	1.770	0.236
LABOR	3.820	0.510
MATERIALS	9.430	1.257
UTILITIES	1.664	0.274
TOTAL	31.704	4.78

9. Wafer Plating

The conceptual design of a proposed wafer plating system has been introduced in the previous quarterly report. During the present quarter, a detailed design had been finalized and was subsequently sent out for fabrication.

The design drawing for the wafer plating system is depicted in graphic detail in Figure 2. A minor revision instituted for this design consisted in rotating the first cleaning tank and metallization tank by 90° so that they would be easily accessible during the process sequence and also more readily adapted to complete automation. An additional modification in the preliminary design has been necessitated as the result of the poor thermal conductivity of polyethylene which implies an excessive warming-up period for the nickel tank. In order to correct this situation, a Corning Glass tank was chosen to supersede the polyethylene tank.

The standard-sized Corning Glass tank currently available in today's market is much too small to comply with the designated design size requirements as set forth in the design drawing, and the special fabrication of this design size will evidently be extremely costly. Consequently, four standard sized Corning Fast Baths (Model No. 6796VC8) will be used in place of the former two large-sized baths for the remainder of the experimental study.

The Corning VC-8 model has been specifically designed for rapidly heating numerous varieties of liquids

Figure 2. Nickel plating tank system.

and maintains an eight liter capacity. This equipment is composed of a heating container fabricated from Corning's VYCOR glass, which sustains a resistance against various concentrations of hot acids such as phosphoric, chromic, nitric, sulfuric, and organic based photoresistant stripping solutions. The vessel design allows for a rapid warming-period of ten to twenty minutes with a temperature control of $\pm 2^{\circ}\text{C}$ at equilibrium over a 40 to 180°C range. The inner vessel of the bath contains a recessed mill for the accommodation of the Corning PC-353 magnetic stirring bar.

An additional component incorporated into the cascade rinse tank consists of a conductance sensor used in conjunction with a servo-mechanism, which exerts complete control over the flow rate of the cascade rinse water in accordance with the degree of contamination present in the rinse water.

The above mentioned equipment modifications have been incorporated into the finalized version of the design drawing, and all essential parts required for the complete system fabrication have been placed on order.

10. Solder Coating and Flux Removal

According to a recent literature survey, the most widely used solder coating and flux removal technique currently practised on production lines in the semiconductor industry has been found to be wave soldering and solder dipping.

The dipping method is a single process cycle whereas the wave soldering machine requires a two process cycle since it is capable of coating only one side at a time. The dipping method is therefore more economical and maintains a higher production rate relative to the wave soldering method.

Fully automated dipping machines are readily available in the semiconductor components market. Experimental studies pertaining to the soldering characteristics of the silicon solar cells will be conducted in an existing solder bath at Sensor Technology.

The crucial parameters to be investigated in the experimental study are as follows:

- (a) dipping direction
- (b) orientation of wafer surface
- (c) preheat-temperature
- (d) optimum solder temperature
- (e) optimum fixture design

Temporary fixtures have been designed and will be tested next quarter.

The following areas pertaining to the flux removal process and the drier process are scheduled to be investigated:

- (a) rinse tank with ultra-sonic
- (b) nitrogen bubbler
- (c) I.R. oven drier
- (d) hot clean air blower

A preliminary test conducted in response to the flux removal study indicated that a rinse tank with an ultra-sonic agitator is the only known rinse system which will yield admissible results. The over-flow rinse method is completely ineffectual in this application, and the nitrogen bubbler system was found to be equally unsuitable due to the fact that flux residue was observed during the course of the process cycle.

11. Cell Handling for Module Construction

Cell handling for module construction will require precision postitioning techniques in addition to an approximate rate of 2 cells per second if the module construcion line is to produce 7200 wafers per hour or 60 modules per hour in accordance with the projected 1986 industrial production goals.

Several varieties of cell handling units are available from semiconductor industries and most of them are designed to fit a particular machine. For example, the printing machine industry uses cassette to conveyor loading which requires an additional positioning system, and is capable of handling up to 3600 wafers/hr.

A precision positioning system used extensively in the semiconductor industry is the robot arm system which operates at a slow rate. This rate is primarily dependent upon the number of degrees of freedom required

to locate a cell and usually exceeds 2 seconds/cycle.

An alternate dispensing technique utilizes the hopper dispensing unit. It has the advantage of being able to simultaneously dispense several cells so that the cycle time can be enhanced to the degree necessary for the attainment of the desired production rate. However, the hopper dispenser unit is unable to deposit the cells within a close enough proximity such that the gap between cells is approximately 50 mils. It has therefore been concluded that the most promising technique of cell deposition will be the robot arm method with multi-pickup cups.

The module which is to be used in this study will contain six full cells and two half cells per row, with each alternating row maintaining the same sequential cell arrangement.

The conceptual drawing of the solar cell handling system is shown in Figure 3. Two robot arms will each simultaneously deposit the six full cells and two half cells placed in a pre-arranged pattern of their respective cell storage racks.

This new technique will deposit a total of 16 cells per cycle with good pattern reproducibility. The required cycle time has been determined to be 6 seconds and the conveyor will move by two rows during each cycle.

In view of the above considerations, the robot arm technique has been determined to be extremely suitable for our present requirements.

Figure 3. Conceptual drawing of cell handling system for automatic module assembly line.

12. Laser Trimming and Holing Automation

The satisfactory conclusion of the laser trimming and holing automation task will depend primarily upon the constraints imposed by the technology and costs necessary to invoke a higher throughput from Quantronix Corporation's Model 603 laserscribe. Consultation between Quantronix Corporation personnel and representatives from Sensor Technology has resulted in a proposal detailing the materials and services required to implement laserscribing techniques to the production of scribed silicon solar cells with central hole.

A study was subsequently devised which set out to investigate the utility and cost effectiveness of a system capable of accepting a batch of wafers in the form of a multiple track conveyor. The system will (a) receive wafers from the conveyor, (b) orient and position the wafer (c) scribe and trapan the wafer, (d) break along the hexagonal scribes and remove the trepanned plug and finally (e) reload the finished wafers onto the conveyor.

Two potentially automated systems capable of laserscribing silicon wafers to produce hexagonally shaped wafers with central holes are currently being

reviewed in order to establish the output capability, maintainability, reliability, and economic characteristics of each system.

The first system to be considered is the serial flow laserscribe system. This unit is comprised of 2 loaders, 2 aligners, 3 dual beam lasers, 4 trepanning (holing) lasers, 4 wafer crackers and a moving surface onto which are mounted, at evenly spaced intervals, wafer holding chucks as shown in Figure 4. One wafer at a time is removed from its storage container and transferred onto a holding chuck which carries the wafer through the scribing process. The wafer is moved along by conveyor to the wafer aligner where the wafer grid lines are oriented in preparation for scribing. The wafer is then passed under a dual beam laser whose beams are aligned and focused so that two parallel sides of a hexagon are simultaneously scribed. The wafer is next moved at constant speed to the chuck rotator which is indexed to turn the wafer 60° , and it will then be transferred to laser number 2 where the second pair of parallel sides are scribed. The partly scribed wafer is again rotated 60° and the last pair of parallel sides are scribed by laser number 3. The hexagon scribed wafer will be offloaded from the conveyor and then distributed to the trepanned (hole) scriber/cracker units. Since it takes four times as long to produce holes as to scribe the hexagon, four trepanned/cracker units are needed for each hex/scriber unit.

FIGURE 4. SERIAL FLOW LASERSCRIBE SYSTEM FOR 7200 WAFERS PER HOUR.

The finished wafers are finally off-loaded from the trepanned/cracker and loaded onto the carousel conveyor which carries them to the packer where the scribed wafers are returned to storage containers. The empty chucks are transferred to the return conveyor and to the loader to receive the next wafer. The scrap silicon, meanwhile, is collected and returned to the recycling station.

The second system under consideration is the parallel flow laserscribe system. It contains four dual beam lasers aligned as shown in Figure 5. Wafers are offloaded from cassettes, aligned and loaded onto platens accepting eight wafers each. The loaded platen is moved to the X-Y table where it is keyed and locked in position under the laser beams. The table is programmed to scribe first the hexagon and then the central hole.

The platen containing the scribed and trepanned wafers is next moved to the cracker unit where the edges and the center hole materials are removed from all eight wafers at the same time. The scribed and trepanned wafers are carried to the packer to be off-loaded from the platen and loaded into cassettes. The scrap is collected and returned by conveyor to the recycling station. Note that the various operations - loading/aligning, scribing/holing, cracking, and packing operations - are simultaneous steps timed so that each operation is accomplished

FIGURE 5. PARALLEL FLOW LASERSCRIBE SYSTEM FOR 4800 WAFERS PER HOUR.

in the same time interval. The time interval between wafer sets depends on scribing time and the time required between moves.

A cost analysis designed to identify the best cost effective system has been performed and the resulting conclusions are presented in a separate SAMICS section. All input data utilized in the standard Format A has been obtained directly from Quantronix Corporation.

13. Cell and Module Test and Data Storage

Literature pertaining to the microprocessing equipment currently available in today's market has been obtained. This literature has been studied and a system was identified which appeared to be compatible with our present requirements. The Motorola M6800 microprocessor development system integrates the CRT display/keyboard with the mainframe of the central processing unit and thus requires no special interfacing. No comparable system was found in the current market which will approach the performance capabilities and cost of the M6800 system.

The M6800 system was placed on order and was recently received by Sensor Technology. A performance verification test for the M6800 system is in its initial stages, and no conclusive results have been reported to date.

14. Module Construction Study

The module construction study is composed primarily of the following three major areas:

- (1) Cell dispensing at the precise location
- (2) Interconnection soldering operation
- (3) Encapsulation process

The cell dispensing area has already been discussed in Task 2 and consequently, the remaining two areas will occupy a major portion of the discussion which follows.

By utilizing a flexible printed circuit sheet, the only key problem which is expected to occur will be the simultaneous soldering of the front and back contacts. Induction soldering and IR soldering are both widely used procedures for producing simultaneous multiconnections, but unfortunately, neither method is applicable to a cell containing soldered gridlines since the re-flow of solder from the gridlines may damage the metal contacts which in turn will adversely affect the cell efficiency.

A preliminary soldering test on a flexible printed circuit sheet has been performed with the primary objective of evaluating three prospective materials for use as a base material in the flexible pc sheet, and then selecting from these, that material which displays the most admissible characteristics.

The three materials which have been evaluated during this test are:

K1 = 1 mil Kapton with 2oz Cu.

K2 = 2 mil Kapton with 2oz Cu.

M3 = 3 mil Mylar with 2oz Cu.

A highly skilled operator performed the actual soldering task with the use of a hand-soldering iron with controlled tip at a temperature of 700°F. The entire soldering sequence was precisely timed and the following results were subsequently obtained:

K1: Time: 4 sec, no damage to Kapton - satisfactory.

K2: Time: 10 sec, no damage to Kapton - solder does not melt.

M3: Time: 4 sec, Mylar melts - good soldering

In retrospect, the soldering iron has been found to be completely ineffectual with regard to the melting of solder on material type K2 due primarily to material K2's good thermal insulation quality. On the other hand, the characteristics of material type K1 have been found to be adequate. The Mylar material had melted due to its low melting point and therefore evinced good heat transfer characteristics which caused the solder to melt instantaneously.

The back surface contact soldering gave poor results since it acted like a large heat sink and consequently exhibited poor thermal conductivity. A more

accurate and intense heat source will thus be needed for the contact soldering task.

A flameless inert gas soldering method was investigated in order to determine its applicability for use in conjunction with a specified base material for the flexible pc sheet. The flameless heating unit studied offers extremely precise temperature control for production soldering, brazing, bonding, curing or melting at temperatures up to 1600⁰F. The heater consists of a tungsten filament inside a quartz tube over which air or inert gasses such as argon or nitrogen are passed. The coil design provides extremely efficient energy transfer which permits precision non-contact heating of parts in open or confined areas. Controls permit regulation of gas flow, pressure, and electrical input into the heater thus allowing pin-point repeatable heat control.

The following experiments have been performed with this equipment:

- (1) Front surface contact soldering
- (2) Back surface contact soldering
- (3) Soldering cell to a 2 oz. copper Kapton sheet

All experimental results proved to be extremely satisfactory and thus it is highly recommended that this process be pursued for further investigation and study.

The encapsulation study was unable to proceed according to schedule due to an extended delay in the fabrication of the flexible printed circuit sheet. Despite the fact that the design had been finalized, relatively few manufacturers to date, have offered a concession to fabricate the flexible printed circuit sheet due to the extremely high precise measurement requirements involved in its construction.

A small company which utilizes a manual process sequence has quoted a figure of \$500/sq ft. for the fabrication of the flexible printed circuit sheet. On the other hand, a somewhat larger company has offered to mass produce the flexible printed circuit sheet at a cost of \$8/sq ft. with the stipulation that a sufficiently large quantity be placed on order. In view of the above considerations, an investigation will be conducted for the purpose of identifying a new, low-cost flexible printed circuit board fabrication method.

15. Spray-on Dopants

Sensor Technology submitted a purchase order to Advanced Concept Equipment Division of Huestic Machine Corporation, Bristol, Rhode Island to fabricate a spray chamber module, conveyor and pallet system, and infra-red drying system. A description of this equipment is discussed in detail in the last quarterly report.

An investigation is being conducted by Advanced Concepts for the purpose of identifying various techniques for turning wafers over so that they may be sprayed on both sides. The conceptual drawings of the recommended techniques will be submitted to Sensor Technology next quarter. A study is also being undertaken to determine the feasibility of constructing a prototype, hand operated, bench model twin-track loader for handling wafers from the air track onto the stationary pallet which is similar to a unit presently manufactured by Advanced Concepts.

Upon completion of the above-mentioned studies, the best wafer turn-over mechanism will be identified and then utilized in a conceptual drawing for a pilot plant array automated assembly line.

In-house preliminary experimentation was performed during this quarter in the area of spray-on dopants. The two types of dopants used in this respect are as follows:

- (1) Phosphosilica film for N^+ front surface
- (2) Borosilica film for P^+ back surface

A plastic fixture was fabricated to test the wafers. Each wafer was manually placed in the fixture recess and sprayed with either the N^+ Phosphosilica film or the P^+ Borosilica film. It was observed that no dopant creeping around the edges of the wafer occurred when the surfaces were initially dry. The wafer surface coverage was uniform and the experiments were reproducible without

any problems. This technique looks very promising and will be pursued in much greater detail after the model equipment has been completed.

A preliminary process cost estimation for the spray-on dopant task has been performed on the basis of the conveyORIZED model spray equipment and the in-house experimental studies. Even though the resulting figure was compatible with the 1986 pricing goals, a considerable portion of the total cost was due to material costs. It is therefore recommended that an extensive study be performed to minimize the dopant consumption rate which is a direct function of nozzle performance.

16. Conveyorized Dopant Diffusion

Conveyorized dopant diffusion is being investigated as an alternative dopant diffusion method. An initial contact was made with Pacific Western Systems, Inc. in Mountainview, California regarding the Pacific Western Model PWS 5000 Vapox Reactor which is a fully automated and conveyorized system. It is reportedly an efficient, low capital cost vapor phase oxidation system designed specifically for depositing both doped and undoped silicon dioxide film in the 380°C to 450°C temperature range. The Model PWS 5000 Vapox Reactor is capable of automatically depositing single, dual and triple layers of dopants onto silicon wafers. The system utilizes a wafer transport

mechanism that moves wafers under a gas dispersion head which dispenses the gas in a downward direction.

The method of approach to be followed in the experimental investigation will be to sample test a batch of twenty-five wafers on location at Pacific Western Systems, Inc. No experimental results have been reported to date, however a preliminary process cost estimate has been performed. The process cost estimation proceeded without the inclusion of the dopant gas cost since this figure has not been determined at the present time. The estimated process cost was found to exceed 9.5¢/peak watt which therefore renders this process completely unsuitable in its present configuration for usage in the 1986 industry.

17. Module Fabrication

The implementation of a new module fabrication concept will require the formulation of a new module design. In the previous quarter, a design was presented for the flexible printed circuit sheet required in the automatic interconnection procedure. The final designs of all remaining crucial elements of this task have been completed.

a) Cell Design

A hexagonal cell with a central hole has been selected for usage in the proposed module. The most pronounced difference between the new cell design and the

cell currently produced by Sensor Technology lies in the central hole current collection of the new cell as opposed to the present method of edge current collection.

The new cell will be fabricated from standard sized 90mm diameter silicon wafers. Hexagonally shaped wafers with point to point diameters of 3.54 inches and central hole diameters of .150 inches will be formed by means of an automated laserscribe machine. The gridline pattern will be designed so that the combined effect of the shadowing and ohmic power loss components will be minimized. The ohmic power loss encompasses both the diffusion layer ohmic loss and the metal grid line ohmic loss.

The gridline pattern optimization was calculated according to the following specifications:

- (1) The gridline width is fixed at 7 mils which is the technological limit imposed by the thick film printing equipment.
- (2) Each gridline will be separated by equal areas which results in an equal current flow into each gridline.
- (3) The trunk-line will extend through the center of each triangular area which enables the cell to be cut through any diagonal thus preparing the cell for placement in the module.

- (4) The approximate values of the resistances used in the various power loss calculations are as follows:

Diffusion layer resistance: $30\Omega/\square$

Gridline sheet resistance: $0.004\Omega/\square$

Trunkline sheet resistance: $0.001\Omega/\square$

- (5) Current density was assumed to be 32.5 mA/cm^2 and the voltage at the maximum load was assumed to be 0.5 volts.

Upon utilizing the above assumptions, it was found that the optimum number of gridlines should be seven for the hexagonal solar cell with central hole. The gridline pattern is delineated in graphic detail in Figures 6 and 7.

The calculated results for the fractional power loss of each element of the hexagonal solar cell with central hole are presented in Table 2. It is evident from the table that the largest contributing element to the total fractional power loss resides with the gridline shadowing power loss. In order to minimize this loss, the gridline widths should be proportionately reduced. Unfortunately, the gridline width can only be reduced to a certain point due to the constraints imposed by the technological limits of the current thick film printing equipment. A second alternative is to increase the spacing between the gridlines so that fewer gridlines

METRIC
ENGLISH

Figure 6. Hexagonal solar cell with central hole.

All Widths of Gridlines = 0.007

Trunk Width = 0.010 to 0.040

Number of Gridlines = 7

Figure 7. Hexagonal solar cell grid pattern with central hole.

Table 2. Fractional power loss of each element of the hexagonal solar cell with central hole.

Element	Shadowing Loss (%)	Ohmic Loss (%)
Diffusion layer	-----	2.761
Gridline	4.374	0.402
Trunk line	2.364	2.49
Center "O" ring	1.810	0.161
Total	8.548	5.814
Total fractional power loss = 14.362%		

are needed. However, by decreasing the number of gridlines from, for example, seven to six, the total fractional power loss increased from 14.36% to 14.9%. This fractional power loss occurred because the shadow reduction due to less gridlines produced a smaller fractional power loss than the combined diffusion layer and ohmic power losses. Calculations also show that the number of gridlines and gridline patterns are relatively insensitive for an optimized amount of shadowing on a solar cell. One can improve the fractional power loss two to three percent by reducing the gridline width. This is due to the fact that the ohmic loss for our gridlines is very small.

The final point to be considered will be the "O" ring contact line which maintains a large shadowing loss and a small ohmic power loss. This situation cannot be easily rectified since tab soldering requires a finite area.

b) Module Design

(1) Dimensions

The dimensional aspects of the new 2'X 4' module have been selected on the basis of the recommended standard sizes allocated by the LSA project. The 2'X 4' module will facilitate easy handling during the

manufacturing process sequence and will thus obviate the requirement for heavy equipment.

(2) Cell Interconnection

One module will contain a total of 118 hexagonal solar cells. The packing arrangement of 102 full cells and 34 half cells is exemplified in Figure 8, where the spacing between cells is 0.05 inches, the solar cell area is 968.65in^2 , the cell nesting area is 1030.58in^2 and the module area is 1113.09in^2 . The packing ratio has been determined to be 87% and the solar cell nesting efficiency is 94%. To minimize electrical power loss due to cell failure a group of three full cells and one half cell will be connected in parallel and thirty-four groups will be connected in series. Upon utilizing the 1986 goals set for the cell performance level: encapsulated cell efficiency is 14.5% and peak power is 0.76 watts per cell. The expected module performance will be as follows: peak power is 90 watts, voltage at maximum power is 17.14 volts, and current at maximum power is 5.25 amps. All cell interconnections will be achieved by means of the flexible printed circuit board.

DATE	LTN	REVISION	DR	CHK	APP

NOTE: UNLESS OTHERWISE SPECIFIED

ITEM	PART NO.	DESCRIPTION	DR	CHK	APP
<div> <div> <p>SENSOR TECHNOLOGY, Inc. CHATSORTH • CA. 91311</p> </div> <div> <p>DR: <i>[Signature]</i> CHK: <i>[Signature]</i> APP: <i>[Signature]</i> WORK ON: JH-L RFP ED-2-857</p> </div> </div>					
TITLE: SOLAR CELL MODULE					
MATERIAL		SCALE: 5:1	AWG. NO.	SHEET	REV
		c	FIG. 8	OF	

c) Encapsulant Materials

The selection of suitable encapsulant material is imperative if a reduction in the total module cost is to occur. Since a detailed analysis of encapsulant materials is beyond the scope of the present study, the final selection will be formulated on the basis of literature provided by companies actively involved in this pursuit.

An exploded view of the proposed solar cell module is shown in Figure 9. The soda lime glass which was utilized as a substrate material also serves the additional function of acting as a structural support. The cells are bonded to the soda lime glass by a silicon adhesive or pressure sensitive PVB laminated sheet. The flexible printed circuit sheet that is soldered to the cell will be widely dispersed with circular holes which permit a back protection sheet to be securely bonded to the cell with the use of the proper adhesive. The exposed edges of the bonded glass will be sealed with a butyl rubber gasket or tape to facilitate the effective prevention of moisture penetration. An aluminum frame which will be used to house the glass module, also serves as a mechanism for mounting the module. The tentative materials selected for use in this task are summarized in Table 3. The final selection of encapsulant materials will be based upon empirical results.

Figure 9. Exploded view of hexagonal solar cell module.

Table 3. Selected encapsulant materials for module elements.

Elements	Selected Materials
Superstrate	ASG SUNADEx (Rolled water white, 0.0190 iron oxide) glass, tempered, 1/8" thick.
Flexible Circuits	0.001" Kapton with 2 oz. copper laminated.
Adhesive Materials	Silicone adhesive, or polyvinyl Butynal film laminated (0.01" - 0.2" thick)
Substrate	Fiber glass, FEP teflon (Type B or CB) or other polymer sheet (0.02" - 0.05" thick)
Edge Sealant	Butylrubber or polysulfide sealants or tapes
Frame	Extruded Aluminum frame anodized

The cost estimations for the tentatively selected encapsulant materials are summarized in Table 4. It is apparant that the major contributing factor to the high encapsulant material costs lies in the excessive flexible printed circuit sheet cost. It is therefore recommended that the expensive flexible printed circuit sheet be replaced by a lower priced stamped copper sheet or other equivalent connector to achieve a reduction in the overall module fabrication cost.

Table 4. Encapsulant material costs in 1978 dollars.

<u>Elements</u>	<u>Cost Per Unit Area</u> <u>(\$/ft²)</u>	<u>Cost Per Watt</u> <u>(\$/watt)</u>
Glass 0.125" thick	0.940	0.0836
PVB 0.01" thick	0.258	0.023
Mylar 0.005" thick	0.0684	0.0061
RTV 108 Adhesive 2 mils thick	0.468	0.0416
Flexible circuit sheet	8.00	0.711
Aluminum frame structure	<u>0.474</u>	<u>0.0421</u>
	\$10.208.	0.9074

SAMICS

1. Introduction

Two separate cost estimations are performed for each process study. A preliminary cost estimation is performed prior to the establishment of an in-depth automation study for the specific purpose of determining the process feasibility in terms of 1986 pricing goals in addition to indicating which direction to proceed in order to optimize the process. A final SAMICS calculation will subsequently be performed, and then utilized in the overall process line cost estimation.

2. Preliminary SAMICS

In order to obtain a preliminary approximation for the overall process cost, y , a simple formula was derived on the basis of the standard SAMICS formula.

The standard working formula from SAMICS is as follows:

$$y = \sum_{j=1}^J y_j = \left\{ \sum_{j=1}^J \sum_{i=1}^5 a_i x_{ij} \right\} / z \quad (1)$$

where $a_1 = 0.49$, $a_2 = 97$, $a_3 = 2.10$, $a_4 = a_5 = 1.3$

J = Total number of processes

x_{1j} = Equipment cost in designated year

x_{2j} = Floor space in square feet

x_{3j} = Annual labor cost at j th step

x_{4j} = Annual material cost in designated year

x_{5j} = Total utility cost in designated year

z = Total annual quantity of designated product

The annual quantities can be expressed as

$$z = f_x \cdot t_m \cdot r_p \quad (2)$$

where

f_x = fraction of useable time

t_m = total operational time for a year

r_p = production rate

Equation (1) can be modified to apply to a single process step based on the following assumptions:

- (1) the production yield at each step is 100%
- (2) the wafer cost is zero
- (3) the fractional required time for each step is identically 0.875.
- (4) one machine operator, 0.1 inspector, 0.1 maintenance man, and 0.014 production planner will be used for each process step.
- (5) the company will operate 24 hours per day and a total of 7245 hours per year. Four shifts are required per day.
- (6) the average power per cell is assumed to be 0.7563 watts.
- (7) the designated goal year is 1986

Using the above assumptions in conjunction with equations (1) and (2), the process cost for a particular process step in 1986 in terms of 1975 dollars is as follows:

$$y = \frac{(0.0606 \cdot EQPT + 1.339 \cdot SQFT + 11.53 \cdot N + 1.8r_m + 1.678r_u)}{0.7563r_p} \quad (3)$$

where

EQPT = equipment in thousand dollars of 1978

SQFT = floor space in hundred dollars

N = number of people needed to operate machinery per shift

r_m = material consumption in 1978 dollars per hour
 r_n = utility consumption in 1978 dollars per hour
 r_p = production rate per hour

In equation (3) the inflation rate utilized for each item is based upon the recommended inflation rate advocated in the SAMICS Cost Account Catalog (ERDA/JPL-954800-77/2.1). In addition, the annual labor costs used in Equation (3) were also obtained from the SAMICS catalog.

The calculated results obtained from Equation (3) will be extremely close to the step by step SAMICS calculation as long as the unit material and utility costs are estimated by means of the largest specified annual quantity presented in the SAMICS catalogue.

3. Plasma Etching by LFE's Model PDS-504-AP(4) (Ref. Task 2)

The currently available model PDS-504-AP(4) plasma etching equipment manufactured by LFE was used in the estimation of the overall process cost. All input data has been obtained from LFE's published catalog. The data required for the preliminary process cost estimation will be as follows:

Equipment = 814,620
Floor Space = 36 ft²
Utility = 510 watts
Oxygen Gas = 300cc/min

Operator = one operator can handle up to 20 machines.

Production Rate = For an 8000Å thick film, the rate is 6.66 wafers/min. For a 5 mil thick resist film, the rate is 2.564 wafers/hr.

Utilizing the above data and equation (3), the following result has been obtained for the total process cost in terms of 1975 cents per peak watt:

Equipment	45.7
Floor Space	24.9
Labor	29.8
Material	0.365
<u>Utility</u>	<u>1.41</u>
Total	102.18 cents/peak watt

This result indicates that the process cost for the plasma etching of thick film resist will exceed one dollar per peak watt in terms of 1975 dollars. Consequently, this method is not recommended for the removal of thick film resist.

A similar calculation for the removal of an 8000Å thick photoresist film yielded a process cost of only 0.82 cents per peak watt. In this respect, the plasma etching method is very promising since the process cost for a typical wet chemical etching procedure will be in the range of 10¢/peak watt.

4. Laser Scanning and Inspection (Ref. Task 5)

Advanced Silicon Material Company's automatic surface inspection system was used to estimate the process

cost for the laser scanning and inspection task. This model is currently available in today's market and is fully automatic.

The basic data obtained from Advanced Silicon Material Company's catalog is as follows:

Equipment:	Main system	\$35,500
	X-Y plotter	11,500
	<u>Card reader</u>	<u>3,750</u>
	Total	\$50,750

Floor space: Allowing space for the operator, 20 sq. ft. will be required

Labor: Since the machine is fully automated, one operator can handle up to 10 units.

Power: 110 volt X 15 amp = 1.65 kw

Material: None

Production rate: 900 wafers/hour

Upon utilizing equation (3) the process cost in terms of 1975 dollars is as follows:

Equipment:	0.452
Floor space:	0.039
Labor:	0.168
Material:	0
<u>Utility:</u>	<u>0.013</u>
Total	0.672 cents/peak watt

Since this result is very promising, it is recommended that a performance verification test be performed with the use of defective photovoltaic solar cells.

5. Silicon Nitride A.R. Coating with a Modified LFE 8000
System (Ref. Task 8)

The preliminary cost estimation for the present LFE 8000 system has been evaluated and reported in the Quarterly Report No. 2. Since this result wasn't very promising, an investigation was initiated for the purpose of obtaining a higher throughput from the LFE 8000 system. It was concluded that a few minor modifications of the wafer handling system would serve to elevate the throughput from 40 wafers/hr. to 300 wafers/hr.

The data which was used for the cost estimation is as follows:

Equipment: the modifications which will take place are: (1) a new vibratory conveyor system, (2) new buffer cassette at the entry and exit locks, and (3) a larger microprocessor. The projected cost of the modified equipment is \$93750.

Floor Space: the floor space will remain unchanged from the previous figure of 40 square feet.

Labor: it is assumed that one operator can handle up to 10 machines.

Utility: Since the deposition rate will remain unchanged, the power increase will be due exclusively to the wafer handling unit. It was estimated that the total electric power consumption rate will increase by 25%. The power requirement of the modified equipment will therefore be 10.29kw. Using the rate of 0.036 dollars/kw-hr., the utility consumption rate will be \$0.37/hr.

Material: Since the gas consumption rate is contingent upon the film deposition rate, the gas consumption rate will remain identical to that of the current module. The total material cost will therefore be \$1.584/hr.

Production Rate: The expected new production rate will be 300 wafers/hr.

Using equation (3) in conjunction with the above data, the following results have been obtained in terms of 1975 cents per peak watt:

Equipment	2.50
Floor Space	0.236
Labor	0.510
Material	1.260
<u>Utility</u>	<u>0.270</u>
Total	4.78 cents/peak watt

This result indicates a significant departure from the previously calculated high process cost of the unmodified system. Unfortunately, this process cost is still in excess of the projected 1986 pricing goals. In order to rectify this situation, further improvements taking the form of a multiwafer chamber or parallel track system will be necessary.

6. Spray-on Dopant (Ref. Task 15)

The conveyORIZED model spray machine now under construction at Advanced Concepts will be used to estimate the process cost for the spray-on dopant process.

The process sequence will require two of the above mentioned machines and a flip-over device which would allow each side of the wafer to be sprayed with a different dopant.

The following data is used in the cost estimation:

Equipment: The current fabrication cost for one unit is \$20,000. \$40,000 will be required for the two units including the flip-over device.

Floor Space: The required floor space for the two machines in addition to operator space will amount to 40 sq. ft.

Labor: It is assumed that one operator can handle up to 5 units.

Material: Phosphosilica and borosilica dopants are used. The unit price for both dopants is \$25/gallon. The dopant consumption rate is between 1cc and 2cc per wafer. The rate of 1cc/wafer will be utilized in this study which implies that the material cost will be \$9.90/hr.

Utility: 124W of power is required in order to operate two units.

Production Rate: Three, 3.5 inch diameter wafers occupy one boat. The belt speed of 1.5ft/min. will move 5 boats/min; thus, the production rate will be 15 wafers/min.

Using the above data, equation (3) gives the following process cost in terms of 1975 cents per peak watt:

Equipment	0.356
Floor Space	0.077
Labor	0.340
Material	2.618
<u>Utility</u>	<u>0.111</u>
Total	3.502 cents/peak watt

The result indicates that this process is compatible with the 1986 pricing goals. Furthermore, since

the largest contributing factor to the total process cost is the material cost, an extensive study is needed to minimize the dopant consumption rate which is directly dependent upon the nozzle performance.

7. Conveyorized Dopant Diffusion (Ref. Task 16)

A large-scale junction formation process considered in this program is conveyorized dopant diffusion. Pacific Western Company's Automatic PWS 5000 Vapox Reactor is suitable for use in this task. Since the precise gas consumption rate is not available at the present time, the process cost estimation will proceed by assuming that the material cost is \$2.00/hr. The following data was utilized for the process cost estimation:

Equipment	\$19,750
Floor Space	22 sq. ft.
Labor	One operator per machine (manual loading)
Material	Assumed to be \$2.00/hr
Utility	50 gal/hr cooling water 8.8kw electric power

The process cost breakdowns obtained from the above data are as follows:

Equipment	0.65
Floor Space	0.158
Labor	6.313

Material	1.967
<u>Utility</u>	<u>0.413</u>
Total	9.501 cents/peak watt

This process cost is not low enough to render it feasible in terms of the 1986 pricing goals. Since this process requires the deposition of dopants on both sides of the wafer, the overall process cost will be even higher. Further study will therefore be imperative if this process cost is to be minimized.

8. Wafer Printing (Ref. Task 6)

a) Prototype Design

Front surface pattern printing is the third process step in the CELLCO Model Company which was defined in Quarterly Report No. 2. The company structure and production quantities were also defined in the previous Quarterly Report. The prototype design which will be used in this study is shown schematically in Figure 10.

The system consists of a printing machine and an I.R. drier tunnel. It has a capability of processing 3000 wafers per hour. The printing machine is the Model 33 printing machine manufactured by Fursland Co. The I.R. drier tunnel used for this study is a conceptual design.

The Fursland Model 33 can easily be equipped with an automatic loader and unloader. The wafers make their entrance from the junction formation process station

Figure 10. SCHEMATIC LAYOUT OF AUTOMATIC WAFER PRINTING SYSTEM (3000 WAFER/HOUR).

by means of a conveyor, and are then loaded by a pick-up arm device to the printer. The printer will print the front surface pattern and then proceed to unload the wafers onto the transfer conveyor. The transfer conveyor is equipped with a hot gas blower which serves as a preliminary ink drying mechanism and thus facilitates easy wafer handling between the loader and the tunnel drier.

The experimentally established drying condition was a fifteen minute drying cycle at 60°C . With a 3 ft. wide conveyor belt in the tunnel drier and a belt speed of 1.7 feet/min; the total length of the run must be 26 feet for a processing yield of 3000 wafers/hour. Upon taking into account the additional two feet required for both the loader and unloader, the total drier length will become 30 ft. A total of five, 3kw capacity I.R. heaters are required for the continual maintenance of a 60°C I.R. tunnel drier temperature.

The total electric power necessary for the operation of this system is estimated to be approximately four horsepower, which allows for the operation of two connection fans, two motors for the loader and unloader, and one main drive motor.

b) SAMICS Calculations

All input data necessary for the evaluation of this process cost is presented in the Standard Format A.

A detailed explanation of all relevant data used in the process cost calculation will follow.

(1) Equipment Costs:

PRINTER

Main Machine \$14000

Loader and Unloader \$ 6000

Total \$20000

TUNNEL DRIER

Tunnel chamber and conveyor \$10000

Fans & main driers \$ 5000

Heater and control \$ 5000

Total \$30000

(2) Floor Space:

The floor space estimation of 360 square feet has been obtained from the layout drawing.

(3) Labor:

One operator will operate one printing system. The remaining necessary personnel are assumed to be identical to those required on other process steps. Four shifts are assumed to operate 24 hours/day for seven days/week.

(4) Materials:

The crucial materials needed in this operation are printing ink and thinner. The consumption rate of these

materials and their unit prices in
terms of 1978 dollars are:

ink	4.0×10^{-5} gal/wafer	\$36.16/gal
thinner	8.67×10^{-6} gal/wafer	\$45.20/gal

(5) Utilities:

The electric power required for each
individual unit is as follows:

printer	0.315kw
fan motors	0.5 hp X 2 = 1 hp
loader and unloader	0.5 hp X 2 = 1 hp
main drive	2 hp
I.R. heaters	3kw X 5 = 15kw
Total	18.3kw

c) SAMICS Conclusions for Wafer Printing

A detailed presentation of all input data is delineated in Format A. The resulting process cost per peak watt in terms of 1986 and 1975 cents has been computed on the basis of the standard SAMICS procedure. The results are presented in Table 5.

The resulting process cost of 1.07¢ per peak watt in terms of 1975 dollars is sufficient for use in the 1986 industry and is thus compatible with the LSA price goal.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

A1 Process Referent FSPF.

A2 Description (Optional) FRONT SURFACE PATTERN PRINTING

PART 1 – PRODUCT DESCRIPTION

A3 Product Referent FSPPW

A4 Name or Description FRONT SURFACE PRINTED WAFER

A5 Units Of Measure _____

PART 2 – PROCESS CHARACTERISTICS

A6 Output Rate 50 Units (given on line A5) Per Operating Minute

A7 Average Time at Station 16 Calendar Minutes

A8 Process Usage Time Fraction 0.875 Average Number of Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS

A9 Component Referent	<u>PRINTER</u>	<u>DRIER</u>	_____
A10 Base Price Year For Purchase Price	<u>1978</u>	<u>1978</u>	_____
A11 Purchase Price (\$ Per Component)	<u>20,000</u>	<u>30,000</u>	_____
A12 Anticipated Useful Life (Years)	<u>8</u>	<u>8</u>	_____
A13 Salvage Value (\$ Per Component)	<u>2,000</u>	<u>3,000</u>	_____
A14 Cost of Removal & Installation (\$/Component)	<u>200</u>	<u>1,500</u>	_____

A14 Process Referent (From Page 1) _____

PART 4 – DIRECT REQUIREMENTS PER MACHINE

A16 Catalog Number	A17 Requirement Description	A18 Amount Required Per Machine	A19 Units
<u>A2064D</u>	<u>Factory Space (Type A)</u>	<u>360</u>	<u>Sq. Ft.</u>
<u>B3704</u>	<u>Operator</u>	<u>.2</u>	<u>Persn.-year</u>
<u>B3736D</u>	<u>Maintenance Mech. II</u>	<u>0.2</u>	
<u>B3256B</u>	<u>Production Planner</u>	<u>0.028</u>	
<u>B3720</u>	<u>Inspector</u>	<u>0.2</u>	

PART 5 – DIRECT REQUIREMENTS PER BATCH (A continuous process has a "batch" of one unit)

A20 Catalog Number	A21 Requirement Description	A22 Amount Required Per Min	A23 Units
<u>G1003D</u>	<u>Resist Ink</u>	<u>2 min. X 10⁻³</u>	<u>gal/min.</u>
<u>G1004D</u>	<u>Thinner</u>	<u>0.334 X 10⁻³</u>	<u>gal/min.</u>
<u>C1032B</u>	<u>Electric power</u>	<u>0.305</u>	<u>kw-hr/min.</u>

PART 6 – INTRA-INDUSTRY PRODUCT(S) REQUIRED

A24 Product Reference	A25 Product Name	A26 Yield Factor (Usable Output/Input)	A27 Units
<u>JUNFW</u>	<u>Wafer After Diffused</u>	<u>0.999</u>	<u>wafers/wafer</u>

Prepared by Sang S. Rhee Date 6/15/78

Table 5. Process costs for wafer printing in cents per peak watt.

	1986 cents	1975 cents
Equipment	0.2943	0.1534
Floor Space	0.2124	0.1107
Labor	0.7351	0.3833
Materials	0.7989	0.4165
Utilities	0.0118	0.0062
Total	2.0525	1.0701

9. Laser Trimming and Holing Automation (Ref Task 12)

Two distinct automated equipment lines designed for hexagonal scribing and central hole cutting will be comparatively evaluated on the basis of their process costs.

a: Serial Flow Laserscribe System

This automated system has a throughput of 7200 wafers/hour. The detailed equipment description is presented in Task (12). All input data has been provided by Quantronix Corporation on the basis of their conceptual design work. The input data is displayed in standard SAMICS Format A. The resulting process cost computations are presented in Table 6.

b) Parallel Flow Laserscribe System

The throughput of this system is 4800 wafers/hour. A detailed description of this system is provided in Task (12). The input data for the SAMICS calculation is presented in Format A. The process cost has been computed in accordance with the standard SAMICS procedure and the results are shown in Table 7.

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

JET PROPULSION LABORATORY
California Institute of Technology
4800 Oak Grove Dr. / Pasadena, Calif. 91103

PROCESS DESCRIPTION

A1 Process Referent HEXLS

A2 Description (Optional) Serial Flow Laserscribe System.
(Hexagonal Scribing & Holing Operation).

PART 1 – PRODUCT DESCRIPTION

A3 Product Referent HEXC

A4 Name or Description Hexagonal Cell.

A5 Units Of Measure Cells

PART 2 – PROCESS CHARACTERISTICS

A6 Output Rate 120 Units (given on line A5) Per Operating Minute

A7 Average Time at Station 0.317 Calendar Minutes

A8 Process Usage Time Fraction 0.95 Average Number of Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS

A9	Component Referent	<u>Serial Flow</u>		
A10	Base Price Year For Purchase Price	<u>1986</u>		
A11	Purchase Price (\$ Per Component)	<u>520,000</u>		
A12	Anticipated Useful Life (Years)	<u>6</u>		
A13	Salvage Value (\$ Per Component)	<u>78,000</u>		
A14	Cost of Removal & Installation (\$/Component)	<u>15,600</u>		

A14 Process Referent (From Page 1) HEXLS - SFS**PART 4 - DIRECT REQUIREMENTS PER MACHINE**

A16 Catalog Number	A17 Requirement Description	A18 Amount Required Per Machine	A19 Units
<u>A2064D</u>	<u>Factory Space</u>	<u>250</u>	<u>Sq. Ft.</u>
<u>B3704D</u>	<u>Machine Operators</u>	<u>4</u>	<u>Person-year</u>
<u>B3720D</u>	<u>Inspector (Q.C.)</u>	<u>0.4</u>	<u>"</u>
<u>B3736D</u>	<u>Maintenance</u>	<u>0.2</u>	<u>"</u>
<u>B3688D</u>	<u>Electronics Main.</u>	<u>0.2</u>	<u>"</u>
<u>B3256B</u>	<u>Production Planner</u>	<u>0.057</u>	<u>"</u>

PART 5 - DIRECT REQUIREMENTS PER BATCH (A continuous process has a "batch" of one unit)

A20 Catalog Number	A21 Requirement Description	A22 Amount Required Per Min	A23 Units
<u>E1608D</u>	<u>Spare Parts</u>	<u>0.0127 min</u>	<u>dollar/min.</u>
<u>C1016B</u>	<u>Cooling Water</u>	<u>5.615</u>	<u>cu.ft./min.</u>
<u>C1032B</u>	<u>Electric Power</u>	<u>1.117</u>	<u>kw-hr/min.</u>

PART 6 - INTRA-INDUSTRY PRODUCT(S) REQUIRED

A24 Product Reference	A25 Product Name	A26 Yield Factor (Usable Output/Input)	A27 Units
<u>CLNC</u>	<u>Cleaned Cell</u>	<u>0.99</u>	<u>cells/cell</u>

Prepared by Sang S. Rhee Date 6/15/78

Table 6. Process costs for serial flow laserscribe system
in cents per peak watt.

	1986 cents	1975 cents
Equipment	0.5219	0.2721
Floor Space	0.0564	0.0294
Labor	0.5612	0.2926
Materials	0.0247	0.0129
Utilities	9.1261	4.7580
Total	10.2903	5.3650

SOLAR ARRAY MANUFACTURING INDUSTRY COSTING STANDARDS

FORMAT A

PROCESS DESCRIPTION

A1 Process Referent HEXLS

A2 Description (Optional) Parallel Flow Laserscribe System

PART 1 – PRODUCT DESCRIPTION

A3 Product Referent HEXC

A4 Name or Description Hexagonal Cell with Hole

A5 Units Of Measure Cells

PART 2 – PROCESS CHARACTERISTICS

A6 Output Rate 80 Units (given on line A5) Per Operating Minute

A7 Average Time at Station 0.517 Calendar Minutes

A8 Process Usage Time Fraction 0.95 Average Number of Operating Minutes Per Minute

PART 3 – EQUIPMENT COST FACTORS

A9 Component Referent Parallel Flow

A10 Base Price Year For Purchase Price 1986

A11 Purchase Price (\$ Per Component) 387,000

A12 Anticipated Useful Life (Years) 6

A13 Salvage Value (\$ Per Component) 58,000

A14 Cost of Removal & Installation (\$/Component) 11,600

A14 Process Referent (From Page 1) HEXLS - PFS**PART 4 - DIRECT REQUIREMENTS PER MACHINE**

A16 Catalog Number	A17 Requirement Description	A18 Amount Required Per Machine	A19 Units
A2064D	Factory Space	180	Sq. Ft.
B3704D	Machine Operator	4	Person-year
B3720D	Inspector (Q.C.)	0.4	"
B3736D	Maintenance	0.2	"
B3688D	Electronics Main.	0.2	"
B3256B	Production Planner	0.057	"

PART 5 - DIRECT REQUIREMENTS PER BATCH (A continuous process has a "batch" of one unit)

A20 Catalog Number	A21 Requirement Description	A22 Amount Required Per Min	A23 Units
E1608D	Spare Parts	0.00983	dollar/min.
C1016B	Cooling Water	4.411	cu.ft./min.
C1032B	Electric Power	0.9033	kw-hr/min.

PART 6 - INTRA-INDUSTRY PRODUCT(S) REQUIRED

A24 Product Reference	A25 Product Name	A26 Yield Factor (Usable Output/Input)	A27 Units
CLNC	Cleaned Cell	0.990	cells/cell

Prepared by Sang S. Rhee Date 6/15/78

Table 7. Process costs for parallel flow laserscribe system in cents per peak watt.

	1986 cents	1975 cents
Equipment	0.5850	0.3049
Floor Space	0.0612	0.0319
Labor	0.8449	0.4400
Materials	0.0192	0.0100
Utilities	11.0986	5.7869
Total	12.6089	6.5737

c) SAMICS Conclusions for Laser Trimming and
Holing Automation

Upon comparing the two systems, it is evident that the serial flow scribing system is more effective than the parallel flow system. The cost analysis indicates that the critical cost factor is the utility cost which is almost 90% of the total process cost. This conclusion is not entirely unexpected since the laser efficiency is only 0.5% for the most technologically advanced laser system currently available in today's market. Consequently, the only method of reducing the laser scribing process cost will be to improve the laser efficiency.

CONCLUSIONS AND RECOMMENDATIONS

A preliminary SAMICS equation has been derived on the basis of the Standard SAMICS formula. This equation can establish the feasibility of the process under consideration, as well as indicating which direction to pursue for optimization.

A preliminary cost analysis has been performed for several process steps which resulted in the formulation of a number of conclusions and recommendations:

The plasma etching process has been found to be cost effective for the removal of 8000Å thick resist, however, it is completely unfeasible for the removal of thick film resist. Since the laser scanning and inspection process cost was extremely favorable, it is recommended that a performance verification test be conducted for the purpose of establishing the viability of the method. A significant process cost reduction for the silicon nitride A.R. coating task can be achieved by means of a modified LFE 8000 system. Since a considerable portion of the total spray-on-dopant process cost resides in material costs alone, it is recommended that an extensive study be performed to minimize the dopant consumption rate which is a direct function of nozzle performance. The conveyORIZED dopant diffusion process costs were excessively high which renders this technique unsuitable in its present form, and will thus warrant further study and investigation.

A standard SAMICS calculation indicated that the thick film resist printing process cost will comply with the LSA 1986 pricing goals. In addition, it was concluded that the serial flow laserscribe system is far more cost effective than the parallel flow laserscribe system. Since approximately 90% of the total process cost resides in utility costs alone, a reduction in the overall process cost can occur only with an improvement in laser beam efficiency.

Due to the excessive costs of flexible printed circuit sheets, it is recommended that an investigation be conducted for the purpose of identifying a new, low cost flexible printed circuit board fabrication technique.

NEW TECHNOLOGY

the cost-effectiveness and utility of the serial flow laserscribing system has been confirmed on the basis of a preliminary SAMICS calculation. This system is designed to (a) receive wafers from the conveyor, (b) orient and position the wafer, (c) scribe and trepan the wafer, (d) break along the hexagonal scribe lines and remove the trepanned plug and finally (e) reload the finished wafers onto the conveyor.

Equipment modifications performed on the Fursland Model 33 thick film printing machine will serve to elevate the current throughput to a rate of 7200 wafers/hour.

The ASM Automatic Surface Inspection System which quantitatively measures the defect level present on a highly reflective surface, can be readily adapted for usage in the automated solar cell inspection task if multitrack systems are utilized.

The novel idea of spraying dopants onto silicon wafers which will subsequently be fabricated into silicon solar cells has been identified and various technological methods for accomplishing this feat are currently under investigation.

PROGRESS SUMMARY AND PROGRAM PLAN

The progress summary and program plan for Phase 2 of the Array Automated Assembly Task is shown in Figure 11.

Figure 11. Phase 2 Array Automated Assembly Task
Progress Summary and Program Plan.

△ planned goals
▲ completed goals