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SILICON PIN DIODE HYBRID ARRAYS FOR CHARGED PARTICLE DETECTION: BUILDING BLOCKS FOR VERTEX DETECTORS AT THE SSC*

GORDON KRAMER** AND STEPHEN GAALEMA
Hughes Aircraft Company, Carlsbad, CA 92009

STEPHEN L. SHAPIRO AND WILLIAM M. DUNWOODIE
Stanford Linear Accelerator Center, Stanford University, Stanford, CA 94309

JOHN F. ARENS AND J. GARRETT JERNIGAN
Space Sciences Laboratory, University of California, Berkeley, CA 94720

ABSTRACT

Two-dimensional arrays of solid state detectors have long been used in visible and infrared systems. Hybrid arrays with separately optimized detector and readout substrates have been extensively developed for infrared sensors. The characteristics and use of these infrared readout chips with silicon PIN diode arrays produced by MICRON SEMICONDUCTOR for detecting high-energy particles are reported. Some of these arrays have been produced in formats as large as 512 × 512 pixels; others have been radiation hardened to total dose levels beyond 1 Mrad. Data generation rates of 380 megasamples/second have been achieved. Analog and digital signal transmission and processing techniques have also been developed to accept and reduce these high data rates

INTRODUCTION

High-resolution vertex and tracking devices at the SSC will be important for the reconstruction of complex events, including secondary vertices close to the primary interaction point. The main properties required of these devices are: fast response time, fine spatial resolution, multiple particle resolution, and radiation hardness.

A resolution of better than 10 μm and the ability to distinguish the many particles of a jet can be achieved with two-dimensional pixel devices. Due to the three-dimensional nature of the coordinate information provided, these provide efficient track finding with a minimum number of layers in the high-multiplicity environment of the SSC.

The SSC beam crossing period will be 15 ns, and interesting events will occur every 100 to 10,000 crossings. Hit times must be recorded to an accuracy of one crossing period, and the readout time of the detectors must be less than the mean interval between interesting events to avoid large dead time losses.

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**Permanent address: Electro-Optical & Data Systems Group, Hughes Aircraft Company, El Segundo, CA 90245.

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The expected combination of high luminosity and large particle multiplicity will produce a high-radiation environment in the vicinity of the collision point. For a proton-proton total cross section of approximately 100 mbarn, the SSC will yield approximately 10^8 interactions per second when operating at its design luminosity of $10^{33}/\mathrm{cm}^2/\mathrm{sec}$. At a distance of 5 cm from the beam, the absorbed radiation dose will be approximately 1 Mrad per year.

New electronic detector systems usually require at least several years for development. Examples are CCDs, infrared detector arrays and x-ray bolometers. The schedule for the SSC construction is commensurate with the schedule for new vertex detector development if the latest existing technology is used as a base.

DEVICE CANDIDATES

Candidates for vertex/tracking devices at the SSC include: wire chambers, scintillating fiber detectors, silicon microstrip detectors, double-sided microstrip detectors, silicon drift chambers; and pixel devices in the form of CCD arrays, monolithic silicon arrays and hybrid microdiode arrays. It is generally recognized that in terms of space, momentum and two-track resolution, wire chambers at present are inferior to silicon devices. It is also generally recognized that pixel devices are preferable to strip devices or drift devices, as far as two-track resolution is concerned.

Pixel devices – in particular, silicon diode arrays – are a natural choice for vertex detectors. These devices provide three-dimensional coordinate information with a spatial resolution of a few microns. However, as we move farther from the collision point to the tracking detector, many of the other devices mentioned above become attractive candidates for a variety of reasons.

A vertex detector based on the use of a pixel device would provide efficient track finding with a minimum number of layers in the high-multiplicity environment of the SSC due to the three-dimensional nature of the coordinate information provided. The absence of ambiguities in coordinate matching which are always present in nonpixel devices allows the number of detector layers to be minimized, thereby reducing the size and cost of the vertex detector.

The only pixel devices presently in use in high energy physics experiments today are CCDs.[1] These devices are inappropriate to the SSC environment for a variety of reasons, including: (i) a small signal size of about 1000 electrons, which necessitates their being cooled, renders them extremely susceptible to degradation caused by radiation damage, and requires costly and delicate readout electronics; (ii) a varying transfer efficiency across their faces; (iii) no off gate during readout, resulting in a time/space ambiguity; and (iv) a serial readout resulting in a readout time of about 10 msec for a device with 10^5 pixels.

A number of researchers are presently working on the problem of fully integrated pixel detectors in monolithic arrays.[2,3] The goal is to fabricate the readout electronics on the same high-resistivity silicon as the detector diodes. Success in these efforts will result in detectors having the minimum thickness possible. However, there will be a loss of flexibility. A change in either the detector specification or the readout specification will result in not only a circuit change, but also a re-analysis of the production process, since they are now intimately coupled. There will be difficulty in production, since both the detector and the readout electronics must be fabricated in high-resistivity facilities which can hand[illegible] new process. There are far fewer of these facilities worldwide than there [illegible] those which can produce more conventional circuits.

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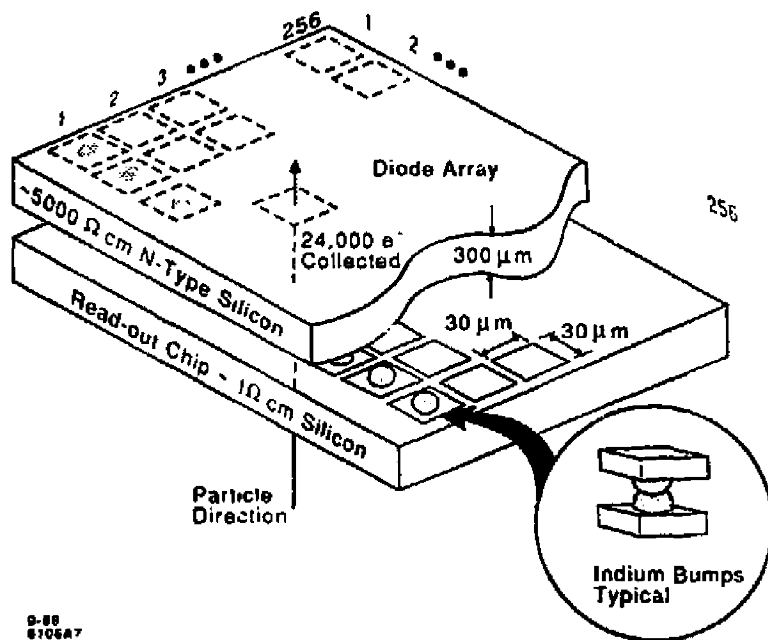

Fig. 1 : Schematic representation of a Silicon PIN Diode hybrid detector.

The architecture which we find to be well suited for charged particle detection at the SSC is that of a hybrid.[4] The charged particle detector and the readout electronics are constructed as two separate silicon chips, each optimized for its specific function. The two chips, indium bump bonded together, then provide the basic building block for the construction of a detector array.

SILICON HYBRID ARRAY EXPERIENCE

The choice of the hybrid design (*viz.*, one in which each diode of the detector array is bonded to an independent amplifier readout circuit on a mating VLSI chip via an array of aligned indium metal bumps that cold weld under pressure to form ohmic contact), allows for additional flexibility in the selection of detector and readout electronics.[5] For instance, a change in the leakage current specification of the detector array will not affect the readout electronics, nor will a change in the VLSI chip oxide thickness to accommodate a radiation hardness specification affect the detector array. Figure 1 is a schematic representation of a silicon PIN diode array hybrid. Figure 2 is a microphotograph of an array of indium bumps prior to the bonding process. The bumps shown are approximately 15 μm in diameter. A small (10×64 pixel) hybrid mounted in a 68-pin leadless carrier is shown in Fig. 3. The readout chip in this device, the Hughes CRC-198, was originally designed to mate with a long-wave infrared detector chip which for optical reasons required 120 μm square pixels. The success of this chip lead to a series of larger arrays with smaller pixels (for 3–4 μm infrared platinum silicide Schottky barrier detectors) as shown in Table I. A photograph of the 256×256 pixel CRC-365 hybrid, which has become fairly mature, is shown in Fig. 4. Figure 5 is a histogram of the infrared sensitivity of each pixel of a 256×256 hybrid array. Of note is the nearly identical electronic response of the 65,536 pixels of the array and the notation that only three pixels in the array are dead. Currently being developed are 512×512 (see Fig. 6) and larger arrays. The circuit used in the array unit cell of all of the chips listed in

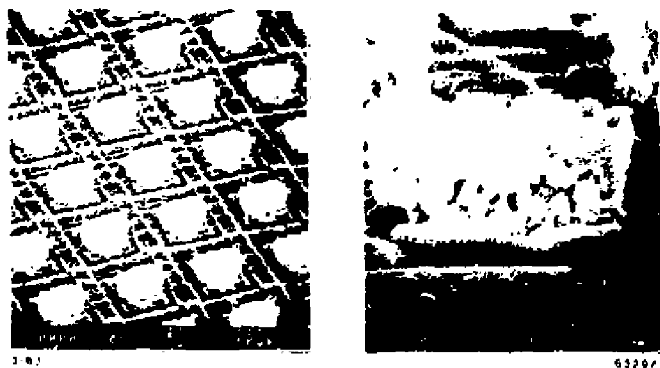

Fig. 2 : A microphotograph of an array of indium bumps prior to the bonding process.

Table I is called a source follower per detector (pixel) or SFD with direct readout (DRO) multiplexing as opposed to CCD multiplexing.

Figure 7 is a schematic diagram of the MOSFET circuit of the 10×64 readout array. The diagram has been divided into its several functional portions. The section replicated for each pixel contains four MOSFETs. Signal charge is generated by the detector diode, and is fed to the gate of the signal MOSFET, where it stays until a readout is made. The pixel selection circuit indicates how a sequence of address lines can select an individual pixel by turning on the gates of the V_{DD} bias MOSFET and the enable gate of the reset MOSFET. The U_{reset} signal allows the gate of the signal MOSFET to be reset to the V_{reset} level for any pixel that is enabled by the reset MOSFET. All of the signal MOSFETs in a column of the array are connected to a readout MOSFET in a source follower configuration which provides power for driving an external circuit.

PIN DIODE HYBRID ARRAYS

The existing infrared readout chips can be mated to PIN diode arrays to produce hybrids with a number of advantages as high-energy particle detectors.

The present readout chips allow random access to any pixel, which then operates as an independent detector. By virtue of its geometry alone, each pixel detector (PIN diode)

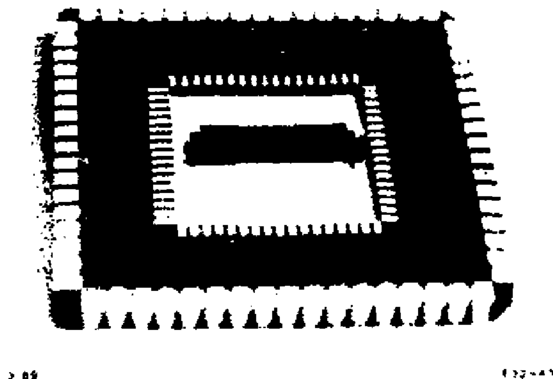

Fig. 3 : A photograph of a 10×64 readout chip bump bonded to a Silicon PIN diode array.

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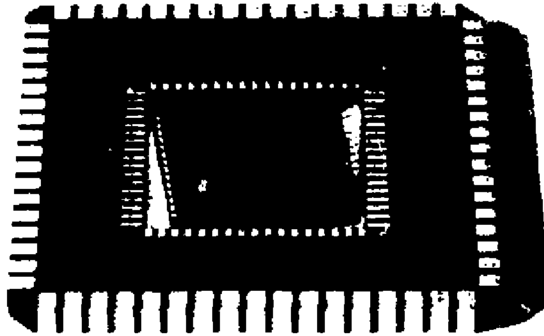

Fig. 4 : A photograph of a 256 × 256 silicon hybrid.

provides about 3,000 times less sensitivity to diode leakage current than a microstrip detector, which will increase the radiation hardness to neutrons. To complement this increase in the radiation hardness of the detector diode, one of the present readout chips (the 10×64 array) has been fabricated in a technology which is radiation hard at cryogenic temperatures to 1 Mrad of Cobalt 60 gamma rays.

The hybrid operates at room temperature, eliminating the need for a cryostat and easing the problems of installation, alignment and accessibility for power and control cabling.

The detector thickness itself can now be optimized. The PIN diode array can be fabricated to give the requisite signal (80 ϵ/μm of silicon), while the VLSI chip can be thinned to less than 100 μm if necessary. This feature is important for minimizing multiple-scattering effects and also for limiting the number of adjacent pixels turned on by tracks incident at large angles to the surface.

It should be noted that the diode anodes are indium bump bonded to the silicon readout chip, leaving the cathode available to be etched into a pattern of pads or strips. Signals picked up on the cathode pads would be available for fast triggering or for reducing

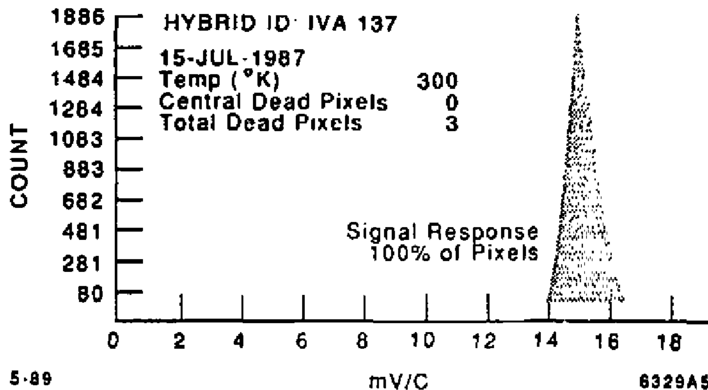

Fig. 5 : A histogram of the infrared sensitivity of each pixel of a 256 × 256 hybrid array.

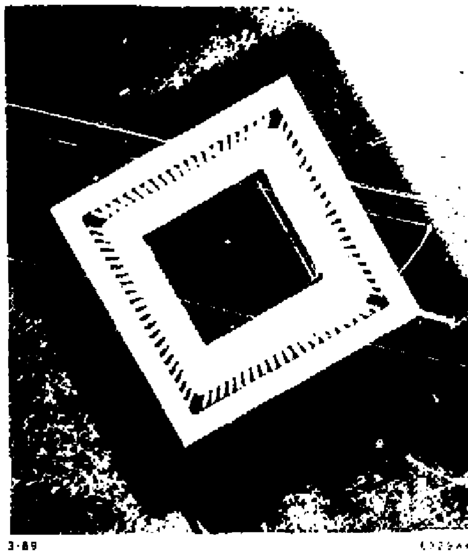

Fig. 6 : A photograph of a 512 × 512 silicon infrared hybrid.

the readout time by using the random access nature of the readout electronics. System considerations will determine if the cathode signals are useful.

To address the problem of data which may accumulate during the readout cycle gating circuitry can be designed to inhibit the flow of charge between the detector and the readout chip after an event is tagged. Alternatively, an input buffer can be added which leaves the detector alive but which does not alter the data being read out. These features do not exist on the present readout chips.

To address the problem of data being recorded from various beam crossings, a design must be adopted which allows the data and the time of arrival to be correlated. Present chips do not have this feature. They do appear to have the ability to provide a "fast indication that a particle has been recorded by the detector. However, we have not yet explicitly studied this feature in the laboratory. This ability, important if confirmed, can

Table I.

Design	Array Size	Pixel Size (μm)	Year
CRC 171	10 × 32	120 × 120	1980
CRC 198	10 × 64	120 × 120	1981
CRC-228	58 × 62	75 × 75	1983
CRC-234	128 × 128	50 × 50	1984
CRC-304	256 × 256	30 × 30	1985
CRC-350	256 × 256	30 × 30	1986
CRC-352	244 × 400	24 × 24	1986
CRC-365	256 × 256	30 × 30	1986
CRC-389A	244 × 400	24 × 24	1987
CRC-389B	512 × 512	20 × 20	1987
CRC-412	488 × 640	20 × 20	1988

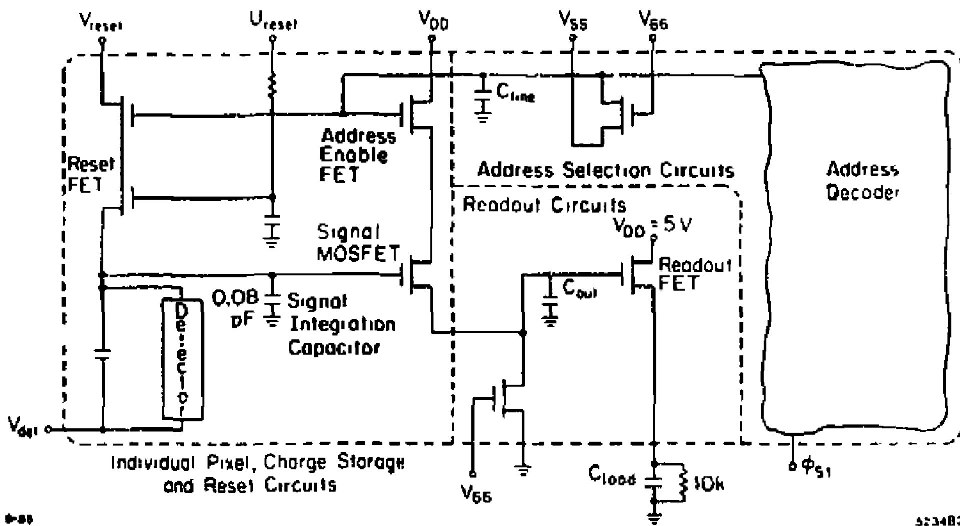

Fig. 7 : Schematic drawing of the readout electronics of the 10 × 64 readout array.

be used in designs to strobe shift registers which record time information while retaining the small pixel size of our present chips.

In the present generation of readout chips, it should be noted that the power used during the write cycle is essentially zero. Power is used only when reading, and cooling needs thus are lessened.

DESCRIPTION OF PRESENT HARDWARE

There are two readout chip geometries currently being built into detector arrays. Figure 8 is a photograph of the two mating PIN diode arrays on a production wafer.[6] Shown are a number of 10×64 arrays with 120 μm square pixels and a number of 256×256 arrays with 30 μm square pixels. The diode arrays are identically processed and differ only in that they must mate with their respective readout chips. The readout chips are

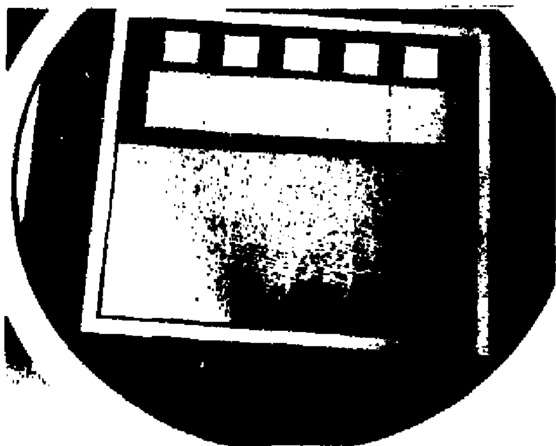

Fig. 8 : A photograph of 256 × 256 and 10 × 64 PIN detectors on a wafer. The five square structures at the top of the wafer are test diodes. The wafers have been manufactured by MICRON SEMICONDUCTOR, LTD., Sussex, England.

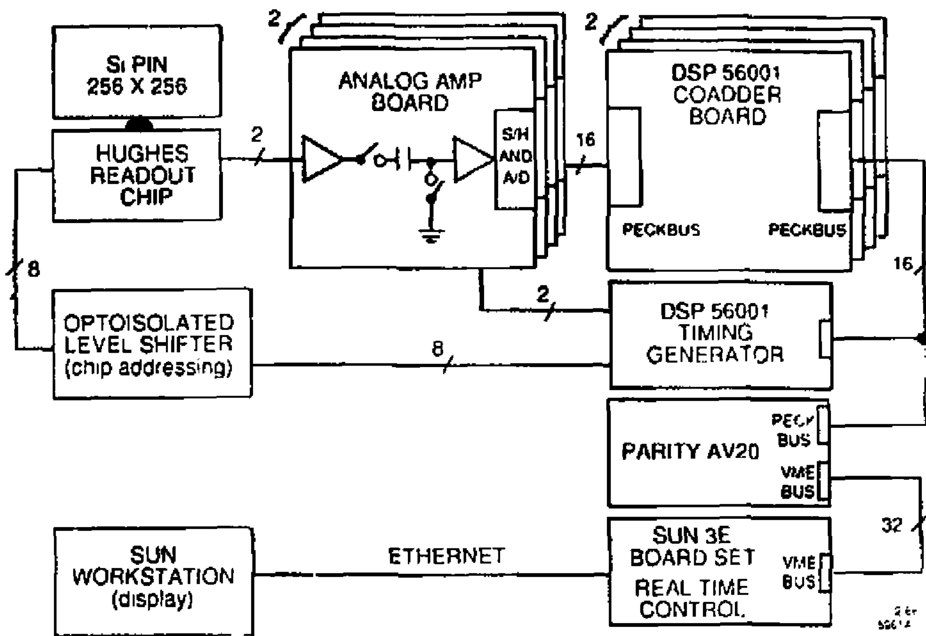

Fig. 9 : A block diagram of the high energy physics data acquisition electronics.

similar, but have some differences. For instance, the 10 × 64 array has been optimized to be radiation hard to 1 Mrad at 10° K. It has a random access architecture in that a unique setting of its address lines will select one and only one row of pixels. The 256 × 256 array, on the other hand, is random access in that the pixels are addressed via row and column shift registers. This feature makes addressing a given pixel more complicated but allows easy implementation of a sparse scan algorithm. This particular readout chip has been optimized to collect electrons but is bipolar at the signal levels we expect.

Figure 9 is a block diagram of the high energy physics data acquisition system. A Sun Microsystems Sun-3/110LC-4 workstation controls a system housing a Sun 3/E CPU, a Motorola 68020 bus converter board, amplifiers, ADCs, digital signal processors and a clock generator. The digital signal processor is the Motorola DSP56001. This device acquires data at a rate of 10 MIPS, processes it and passes it via the MC68020 to the Sun 3/E. The bus converter board, a Parity systems AV20 dual-port processor, interfaces the local analog bus (PECKBUS) to the VME bus.

The noise performance of the 10 × 64 readout chip at 10° K has been measured to be 45 electrons rms referred back to the input. This is within a factor of two of the expected Johnson noise of the gate of the input signal MOSFET. At room temperature, the expected noise signal should be about 200 electrons rms, taking into account the square root of the temperature ratio in the Johnson noise component. However, the measurement has not yet been made. If the noise performance is as expected, detectors thinner than the traditional 300-μm-thick devices currently being fabricated would offer more than adequate signal-to-noise performance.

RESEARCH PROGRESS

Using Detector Development funds from the Department of Energy, a contract was made with Micron Semiconductor to design and fabricate two silicon PIN diode arrays

The array specifications were chosen to allow the detector chips to mate with two Hughes Aircraft Co. readout chips. The arrays fabricated are a 10×64 array with 120 μm square pixels and a 256×256 array with 30 μm square pixels. The first silicon 10×64 hybrid arrays were completed in December 1988, and the silicon 256×256 hybrid arrays are being built. The data discussed in this paper were taken with the 10×64 array.

Additional Detector Development funds were used to begin the fabrication of the dedicated high energy physics data acquisition system described above. The amplifier/ADC/DSP56001 boards and the clock generator in the present system, however, are circuits remaining from the infrared data acquisition system.[7] These need to be re-designed to high energy physics criteria. Figure 10 is a photograph of the data acquisition electronics for the 256×256 array.

A data acquisition and display software package based on the infrared system has been written. The operating system is UNIX, the DSP has been programmed in assembly language, and various control functions are written in Magic/L, an interactive language

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Fig. 10 : A photograph of our present data acquisition system for the 256×256 array.

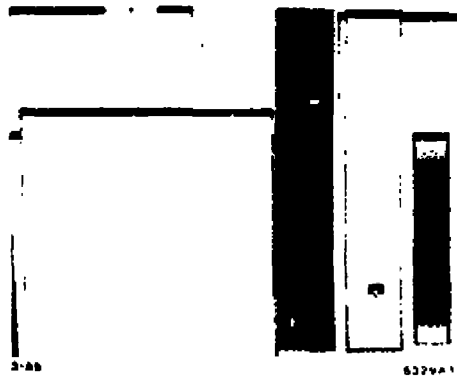

Fig. 11 : A photograph of the SUN display screen. Included is a display of the timing and control pattern, the pulse height scale, and two event windows each showing a 10 × 64 representation of the hybrid.

derived from Forth. The Parity AV20 dual port processor has been programmed in C, and the DSP will be reprogrammed in C. Figure 11 is a photograph of a SUN display during data acquisition. The large window on the left displays the timing pattern used to read out the hybrid. The small window on the right shows the pulse height scale, which is a color scale from blue at the top to white at the bottom. The two rectangular windows just right of the center represent the pixel array and contain two events, the one on the right has detected an alpha particle, while the event on the left has two alphas and a 59.5 KeV x-ray.

Figure 12 is a photo of the hybrid placed under an Americium 241 alpha source. Americium 241 is also a source of 59.5 KeV and 26.3 KeV x-rays. The mounting fixture is a low temperature Dewar for tests to be performed later, which will characterize the hybrid's performance as a function of temperature.

Figure 13 is a scope trace of an output channel. The faint traces are the signals from the detected alpha particles. Correlated double-sampling electronics described

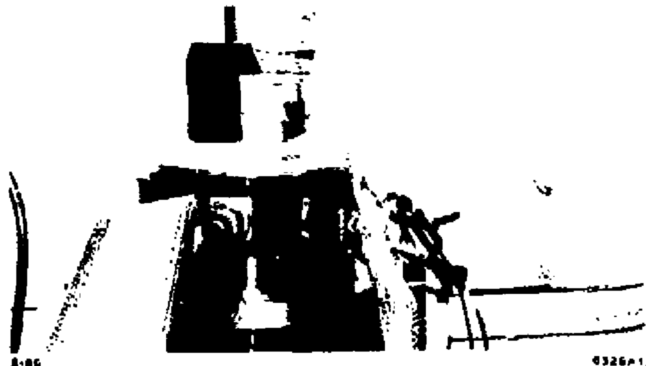

Fig. 12 : A photograph of the hybrid mounted in the Dewar, under an Americium source.

Fig. 13 : A photograph of a scope trace of an output channel (one row) of the 10 × 64 detector.

elsewhere[8] is needed to reduce the 1/f noise and provide the excellent signal-to-noise ratio performance observed.

At the present time, a system exists which can read with either of two detector geometries: 10 × 64 or 256 × 256. The program of testing and characterizing these devices has just begun. The first hybrid arrays have just been manufactured. Preliminary data demonstrate the detection of alpha particles and 60 KeV x-rays with a high signal-to noise ratio. However, the readout system has not been optimized. The timing pattern and bias voltages have not been swept through their respective ranges, and environmental noise has not yet been removed. The preliminary data are encouraging. The detection of a 60 KeV x-ray means that we have detected a signal having approximately 16,700 electrons. This is less than the 24,000 electrons generated by a minimum ionizing particle traversing 300 μm of silicon.

Table II is a summary of current device characteristics.

LOW-MASS, HIGH-DATA-RATE PACKAGING

Packaging techniques have also been developed for the infrared application of these chips that should be very useful for the SSC. A beryllium module pedestal is shown in Fig. 14 that holds several 10 × 64 hybrids used on the Airborn Optical Adjunct (AOA) Program.[9] The beryllium structure that holds up to 48 of these modules in a focal plane (Fig. 15) is over 16 inches long. This focal plane generates over 380 million analog data

Table II: Summary of Device Parameters.

Array dimension	10 × 64	256 × 256
Pixel size	120 μm	30 μm
Detector material	Germanium Silicon	Silicon
Number of readout channels	10	2
Power during "write" cycle	0 mW	0 mW
Power during read cycle	10 mW	2 mW
Present clock speed	1 MHz	2 MHz
Theoretical clock speed	10 MHz	10 MHz
Readout mode	Random Access	Random Access
Processing power	20 MIPS/channel	20 MIPS/channel
Radiation hardness	1 Mrad	?
Noise at room temperature	< 300 e^- rms	< 300 e^- rms

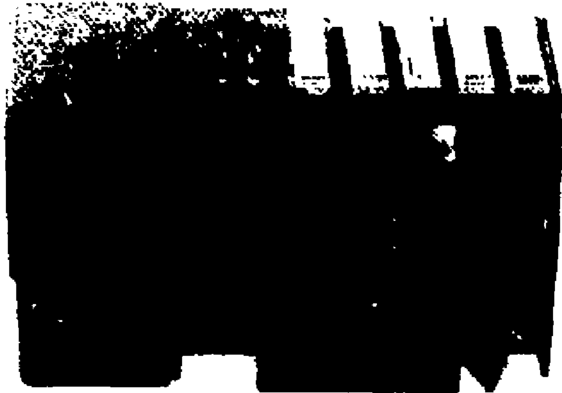

Fig. 14 : A photograph of a beryllium module pedestal holding several 10 × 64 hybrid arrays.

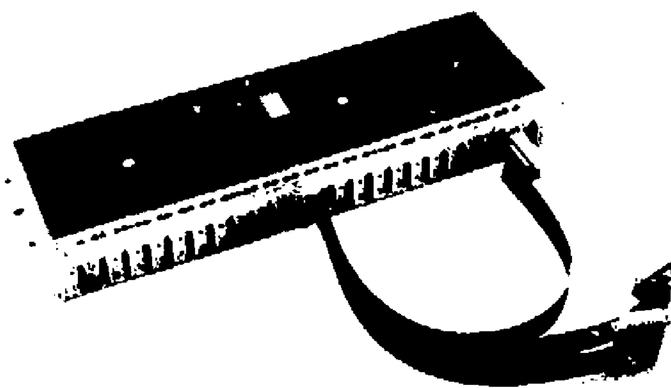

Fig. 15 : A photograph of the AOA focal plane.

samples per second. The data is then converted from analog to digital information and processed at a rate of 15 billion operations per second by the data processor shown in Fig. 16.

CONCLUSION

Silicon PIN diode pixel detectors appear to be the prime candidate for an SSC vertex detector. Pixel detectors should have the best performance in terms of resolution, signal to-noise ratio, radiation hardness and unambiguous high-speed response. An architecture to achieve correlation between the pixel containing the data and the time of the beam crossing using a combination of on-chip and off-chip signal processing appears feasible to implement advanced radiation-hardened silicon CMOS technology. More study is required to ensure that the power that must be dissipated to achieve full operating speed is compatible with the maintenance of PIN diode operating temperatures. The producibility of large hybrid diode array/readout chips of up to 512 × 512 pixels has been demonstrated.

Very preliminary data from our present 10 × 64 silicon hybrid arrays demonstrate the detection of alpha particles and 60 KeV x-rays.

Fig. 16 : Sensor signal processor for the AOA program.

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