WA80 BGO CALORIMETRY ELECTRONICS *

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Abstract

This paper describes instrumentation designed for BGO scintillator-based calorimetry of particles covering a very wide range of energies (from less than 50 MeV to 50 GeV). The instrumentation was designed to have a measurement accuracy of 0.1% over as much of the energy range as possible so the energy resolution of BGO would be the limiting factor. Two 1.5-cm² photodiodes were used per 2.5 cm x 2.5 cm x 25 cm BGO crystal. Both a charge-sensitive preamplifier and a pulse processor were developed specifically for the needs of the WA80 experiment. The preamplifier was designed for high detector capacitance (100 to 700 pF), low integral and differential non-linearity and low power consumption (200 mW). The pulse processor is a time-invariant shaping amplifier with integral peak-detect-and-hold and automatic gain selection circuits. The amplifier uses quasi-triangular shaping with 4 μ s peaking time, and the hold circuit is gated with a fast first level trigger. The system has more than 20 bits of effective resolution when used with an external 12-bit ADC. Results from beam tests at CERN are presented.

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This paper describes instrumentation designed for BGO scintillator-based calorimetry of particles covering a very wide range of energies (from less than 50 MeV to 50 GeV). The instrumentation was designed to have a measurement accuracy of 0.1% over as much of the energy range as possible so the energy resolution of BGO would be the limiting factor. Two 1.5-cm² photodiodes were used per 2.5 cm x 2.5 cm x 25 cm BGO crystal. Both a charge-sensitive preamplifier and a pulse processor were developed specifically for the needs of the WA80 experiment. The preamplifier was designed for high detector capacitance (100 to 700 pF), low integral and differential non-linearity and low power consumption (200 mW). The pulse processor is a time-invariant shaping amplifier with integral peak-detect-and-hold and automatic gain selection circuits. The amplifier uses quasi-triangular shaping with 4 μ s peaking time, and the hold circuit is gated with a fast first level trigger. The system has more than 20 bits of effective resolution when used with an external 12-bit ADC. Preliminary results from beam tests at CERN are presented.

1 INTRODUCTION

The design of instrumentation for a high resolution electromagnetic calorimeter is a challenging problem because of the very wide dynamic range required. In the case of the WA80 experiment, it was desired to cover the range from < 50 MeV to > 50 GeV with energy resolution limited by the BGO scintillator. It was decided that a goal of the electronics design should be 0.1% resolution over that energy range. The designers of the readout electronics for the L3 electromagnetic calorimeter faced the same sort of problem and developed a scheme that split the signal from the preamplifier into several different paths with different gains before analog to digital conversion [1, 2]. Unlike L3, WA80 is a fixed target experiment with asynchronous triggers, and therefore a somewhat different architecture is required for the readout electronics. The remainder of

this paper describes the preamplifier and pulse processor developed specifically for the WA80 experiment.

2 PREAMPLIFIER

The charge-sensitive preamplifier was designed for high detector capacitance (100 to 700 pF), low power consumption (200 mW), low integral non-linearity (<0.025% from 0 to 10 V) and low differential non-linearity (<0.005% from -1 to +10 V). The preamp conversion gain is 0.56 V/pC and the maximum linear output is approximately 10 V, which corresponds to a charge of 18 pC. With two 1.5-cm² photodiodes mounted on a 2.5 cm x 2.5 cm x 25 cm BGO crystal the output is 1.27×10^6 e-h pairs per GeV or 0.203 pC/GeV, so the maximum preamplifier output corresponds to 89 GeV. With the photodiodes connected (200 pF detector capacitance) and using a semi-Gaussian shaping filter with 4 μ s peaking time, the preamp noise was approximately 1000 electrons rms which corresponds to 0.8 MeV.

The preamplifier topology is similar to those published previously [3, 4], but does have some features unique to this implementation. As shown in Fig. 1, the topology is basically a JFET-bipolar folded cascode (Q1, Q5) with a frequency compensated current gain (Q2, Q3). The frequency compensation allows the use of detector capacitances ranging from 100 to 510 pF with resultant risetimes varying from 19 to 32 ns respectively. The output stage is comprised of two transistor arrays (Q6 and Q7) that form a diamond driver. Arrays were chosen over discrete transistors because the improved device matching allows more consistent control of bias currents thus maintaining low power consumption and wide bandwidth with minimal unit to unit variation over a large production run of preamplifiers. Because for this application, the preamplifier needed only to drive unipolar signals, we were able to optimize the topology for maximum slew rate in the positive direction. The optimization was accomplished by noting that the combination of Q1, Q2, Q3, and Q5 will turn "off" faster than the topology presented earlier [4], for a negative input. The slew-rate is then determined solely by the current in Q4 and the total capacitance present at the collector node of Q4. Another feature is the inclusion of

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Figure 1: Charge sensitive preamplifier circuit diagram.

R16 in the emitter circuit of Q5. Bipolar transistors that operate with large capacitances in the emitter may exhibit oscillations due to resultant negative resistances appearing in the base. A resistance in the emitter in series with the capacitance will effectively isolate the capacitor from the transistor [5]. This preamplifier was designed to be used with large geometry FET input devices that can have C_{rss} values of 10 pF or more. This resistor had little if any significant effect on the overall noise.

The preamplifier utilizes surface mount parts placed on both sides of a 1 by 3 inch printed circuit board. The small size allows the preamp to be mounted directly behind the crystal and photodiodes, thereby minimizing the possibility of noise pickup. This mounting arrangement necessitates low power dissipation to prevent heating of the BGO.

3 PULSE PROCESSOR

The WA80 BGO pulse processor is a shaping amplifier with integral peak-detect-and-hold and automatic gain selection circuits. A design using several parallel pulse processing networks with different gains was chosen because of the large dynamic range (1000:1) and high accuracy (0.1%) required. This is similar to the approach taken by the de-

signers of the L3 BGO electromagnetic calorimeter [1, 2], and it allows the use of a 12-bit ADC instead of the 20-bit ADC that would be required for a single pulse processing network to achieve 0.1% accuracy over a 1000:1 range. Fig. 2 illustrates the major components of the pulse processor. The signal from the preamplifier passes through the pole-zero compensation network and is split into two sub-channels each consisting of an active pulse shaping network (4 μ s peaking time) with a gated baseline restoration circuit (BLR) and a peak-detect-and-hold (PDH) circuit. The sub-channels are identical except for their gains. Following each PDH circuit, the signal is split into three paths, each with a different gain. The range select logic chooses the path with the greatest gain that is not saturated and connects it to the output and therefore the external ADC. The PDH circuits can be gated by a fast trigger.

3.1 Pole-zero cancellation and buffer amplifiers

The output of the preamplifier is differentiated with a CR network modified to provide pole-zero cancellation. The pole-zero cancellation is adjustable and allows the use of preamplifiers with decay time constants ranging from 40 μ s to infinity. The nominal input impedance of the pulse processor is 5 k Ω .

Figure 2: WA80 BGO pulse processing module block diagram.

Following the pole-zero network, the signal is routed into both a high-energy sub-channel and a low-energy sub-channel. For high-energy pulses, little gain is required and a low-gain buffer amplifier (x1) is used. For low-energy pulses, a large gain is required so the pulse amplitude will be large enough to digitize and so the pulse shaping circuits will not degrade the signal-to-noise ratio. The high-gain buffer has a nominal gain of 32, and this splits the 1000:1 energy range into two approximately equal ranges. Since high-energy pulses will saturate the high-gain buffer, it is designed so its output is limited to 12 V with good overload recovery characteristics. The buffer amplifiers drive the two pulse shaping sections.

3.2 Pulse shaping and baseline restoration

Active filters are used to produce an approximately triangular pulse shape. This requires only slightly more circuitry than that needed for CR-(RC)⁴ shaping (quasi-Gaussian) and gives better noise performance. To accommodate an expected maximum count rate of 10k counts/s, the pulse processor was designed to function with a maximum rate of 50k counts/s in order to provide a safety margin. This maximum rate dictated that the shaped pulse should return to the baseline in no more than 20 μ s and that the peaking time should be less than 10 μ s. Measurements made using the WA80 BGO preamplifier and photodiodes with a commercial shaping amplifier indicated

Figure 3: Pulse shaping circuit.

Figure 4: Shaped pulse (2 μ s/div and 0.2 V/div).

that a peaking time of 6 to 12 μ s provided optimal noise performance, but slightly shorter peaking times provided faster return to baseline with only a slight noise penalty. A peaking time of 4 μ s was chosen as a compromise.

The actual shaping circuit is shown in Fig. 3. It is a simplified implementation of a concept developed by Goulding, Landis and Madden [6]. After differentiation, the pulse passes through two second-order lowpass filters in cascade, and their outputs are summed to produce a nearly triangular pulse as shown in Fig. 4. The second-order lowpass filters are implemented as Sallen-Key filters using MC34082 opamps. These dual opamps are unity gain stable and low cost, and have a 8-MHz gain-bandwidth product and FET input stages for low input bias currents. The gain-bandwidth product is large enough so nearly ideal characteristics are obtained for the active filters.

Each of the pulse shaping circuits are equipped with a gated baseline restoration circuit (BLR). This circuit maintains the output of each pulse shaping circuit near 0 Vdc except when a pulse is being processed. This minimizes the effects of amplifier offset voltages. When an incoming pulse exceeds a threshold that is set just above the noise level, the BLR is gated off so that it has no effect on the pulse shape or amplitude.

3.3 Peak detect and hold

The peak detect and hold circuit (PDH) records the pulse amplitude for later digitization. It actually consists of a peak detector and a sample and hold circuit. The partially shaped pulse (the output of the first second-order lowpass filter) is differentiated and the zero crossing (which corresponds to the peak) is detected and used to trigger a one-shot. Its period is adjusted so it times out synchronously with the peak of the triangular shaped pulse. This pulse is used to indicate that a peak has been detected and to cause the sample and hold circuit to hold the peak value.

Both the pulse shaping circuit and peak detect and hold are duplicated for each sub-channel. This requires more circuitry, but is necessary since the fast sample and hold circuits used do not have sufficient dynamic range to allow the use of a single pulse shaping circuit and a single peak detect and hold followed by the two buffer amplifiers.

3.4 Gain selection and timing

In order to maintain at least 10-bit (0.1%) accuracy while using a 12-bit ADC, the minimum signal that can be converted is 1/4 of the full scale value or, in other words, the dynamic range of signals to be converted should be no more than 4. Thus, to maintain measurement accuracy over the full dynamic range, each sub-channel is subdivided into several paths with gains differing by no more than a factor of four. The low-energy sub-channel is therefore subdivided into x1, x4 and x16 ranges and the high-energy sub-channel is subdivided into x1, x2, and x8 ranges.

The range select circuitry automatically selects the highest gain output that is not more than 7.5V and passes that output to the ADC. This range selection (the gain used) is reported to the data collection electronics through a rear panel connector. The automatic gain selection can be overridden and manually selected via a switch located on the front panel.

The module timing sequence is initiated by the peak detected signal. When a peak is detected, the sample and hold is placed in the hold mode. A delay is used to allow the range select comparators to settle, and then their outputs are latched into the range select logic. Another delay allows the logic to settle and output the range code to the analog multiplexer before it is enabled. This code selects the correct input, and thereby passes the amplified peak value to the output buffer amplifier. When this output settles, it can be read by the ADC. The multiplexer is enabled for 10 μ s and then the system resets itself. This sequence of events is illustrated in Fig. 5. The output to the ADC should be valid for the period spanning 8 to 16 μ s after the input pulse leading edge, and the ADC should be triggered during this period. The entire sequence of events requires approximately 18 μ s.

Figure 5: Pulse processor timing.

3.5 Coincidence logic

The pulse processor has two modes of operation: one where a coincidence signal is required and one where it is not. When the coincidence signal is used, a peak detected inside the coincidence window will result in the pulse being processed normally. If no peak is detected inside the coincidence window or if no coincidence signal is present when a peak is detected, the pulse processor does not initiate the timing sequence or go to hold mode. The coincidence logic uses the coincidence signal as an enable for the zero crossing signal that triggers the peak detect and hold one-shots. Without the coincidence signal, the one-shots cannot trigger. Since the timing sequence is not initiated if a peak is detected without coincidence, the pulse processor can process another pulse as soon as the shaper output returns to the baseline. For the expected maximum count rate, this should result in few missed events.

4 RESULTS

More than 100 preamplifiers and pulse processors were assembled, tested and used. Modules were made by mounting a preamplifier and photodiodes on a BGO crystal and then connecting this subassembly to a pulse processor. An 8 by 8 array of BGO modules was constructed, calibrated and used in beam tests. The array consisted of 29 non-segmented modules and 35 longitudinally-segmented modules read out at both the front and back of the crystals.

The calibration procedure used electrons of known momenta (10 GeV/c) incident in the center of each module to gain match all modules. Once the gains were matched, the electron beam was centered on the BGO array, and the signal in all modules was summed to give a total signal which then gave the calibration signal to GeV. Intercalibration between the gain ranges of each pulse processor was determined by using an electronic pulser with amplitude fixed at the region of overlap between the various gain ranges. In this procedure, pulses with an amplitude corresponding to the lower limit of a given gain range were processed and digitized. The processor was then switched to the next higher gain range and the pulses were again processed and digitized. Care was taken to ensure that the pulse amplitude did not change during this procedure, and the results gave a set of simultaneous equations for which both the channel intercept and relative gains could be determined.

Table 1 gives typical pulse processor measured gain and energy ranges when used with the WA80 preamplifier, photodiodes and BGO. For the highest gain (lowest energy) range, the electronic noise was typically 1.25 MeV rms and 1.3 MeV rms on the next lower gain range. In the case of the highest gain range (x480), the lowest energy is determined by the peak detect threshold. This threshold was set at a level several times the rms electronic noise. For the higher energy ranges, the resolution of the electronics is limited to no better than 0.1% by the 12-bit ADC. The worst case resolution occurs for a signal at the extreme low end of an energy range. Such a signal corresponds to 0.25 of full scale for the ADC. With a pulse of 5 GeV equivalent, the measured resolution was 7 MeV rms.

Tests of the complete system showed that the resolution was $\sigma/E = 1.4\%$ at 4 GeV when E is measured in GeV. It is suspected that large temperature variations (around 2% on a daily basis) of the BGO affected this result. Preliminary measurements indicated that the position resolution was $\sigma_x/E = 3\text{mm}/\sqrt{E}$.

5 CONCLUSIONS

The preamplifier and pulse processor developed for the WA80 BGO electromagnetic calorimeter performed as designed. The system was able to process pulses corresponding to energies ranging from 20 MeV to 73 GeV.

Table 1: Pulse processor gain and energy ranges

Range	Gain	Energies
6	1	37 GeV–73 GeV
5	2	9 GeV–37 GeV
4	8	2.2 GeV–9 GeV
3	30	610 MeV–2.4 GeV
2	120	150 MeV–610 MeV
1	480	20 MeV–150 MeV

6 ACKNOWLEDGEMENTS

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