MASTER

SLAC-TN 81-7
August 1981

TWO-DIMENSIONAL BEAM-PROFILE MONITOR USING THE RETICON MC510A ARRAY CAMERA*

B. Gottschalk**

Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

*Work supported in part by NSF Grant PHY 79-20821 and in part by the Department of Energy, contract DE-AC03-76SF00515.

**Present address: Harvard Cyclotron Laboratory, 44 Oxford Street, Cambridge, MA 02138.

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

319

CONTENTS

	Abstract	1
I.	INTRODUCTION	1
II.	GENERAL DESCRIPTION	3
	A. Input/Output Specifications	
	1. Camera Interface	
	2. Logger Module	
	3. Display Module	
	B. Camera Setup	
	C. Timing	
III.	DETAILED DESCRIPTION	12
	A. Camera Interface	
	B. Logger Module	
	C. Display Module	
	D. Scaler	
	E. Aperture Control	
	F. Glossary of Acronyms	
IV.	OPERATING EXPERIENCE	29
	A. Sensitivity	
	B. Radiation Damage	
V.	ACKNOWLEDGEMENTS	30
	References	31
	Figure Captions	32
	Figures	35

TWO-DIMENSIONAL BEAM PROFILE MONITOR USING THE RETICON MC510A ARRAY CAMERA*

B. Gottschalk**
Stanford Linear Accelerator Center
Stanford University, Stanford, California 94305

ABSTRACT

A quantitative two-dimensional beam profile may be obtained from a scintillator viewed by a Reticon¹ camera which uses a 32 x 32 array of photodiodes as its sensing element. In this note we describe CAMAC-oriented data acquisition electronics which allows one either to transmit the profile to a computer, or to use the monitor in a stand-alone mode.

I. INTRODUCTION

At accelerator labs one commonly obtains a visual intensity distribution or two-dimensional "profile" of a beam (for focussing, steering, etc.) by passing it through a scintillator viewed by a TV camera. This data could be transmitted to a computer by using a "frame grabber". However, the analog output of vidicon tubes is not particularly stable or linear. In the present system, we use a Reticon¹ MC510A camera whose sensing element is a 32 x 32 array of photodiodes. This leads to a manageable amount of data (1024 words), good linearity and, in our application (the analysis of the SLAC beam) the ability to take a

*Work supported in part by NSF Grant PHY 79-20821 and in part by the Department of Energy, contract DE-AC03-76SF00515.

**Present address: Harvard Cyclotron Laboratory, 44 Oxford Street, Cambridge, MA 02138.

"snapshot" of a single beam pulse.

Figure 1 shows the overall system. The thin scintillator (1 mm CsI tilted at 45°) is mounted in the accelerator tube in such a way that it can be retracted for normal accelerator operations. The camera is located about 12 inches away and views the scintillator through a vacuum window. A camera interface, which adapts the camera signals for transmission over the long cable run, and supplies power to the camera, is mounted a few feet from the camera. The remainder of the system is in the control room. Three coaxial cables carry the video signal, a clocking signal, and a DC control voltage to adjust the lens aperture (optional but highly recommended). A means of inserting and retracting the scintillator, and of illuminating the fiducial grid which surrounds it, must also be provided.

The equipment in the control room consists of a CAMAC "logger" module, a "display" module, a dual scaler (optional), a TV set used as a monitor (optional) and a simple circuit used to power the aperture control. The logger scans the diode array via the interface, digitizing each cell. The number obtained is proportional to the photocurrent in that cell integrated from the previous scan to the present one. The logger stores these numbers in a digital memory (1024 x 10 bits). The data are then transferred (at an appropriate time) to a second memory contained in the display module, updating the TV picture. Then the logger obtains new data or, if it is in HOLD mode, holds the old data for readout through CAMAC. Since all these operations must be synchronized with the accelerator, the TV set, and the computer readout, and since the array must also be cleared (by a "dummy" scan) before the beam pulse

arrives, the actual timing sequence is somewhat complicated, and will be discussed separately.

In addition to the TV picture, the display module provides features which allow one to analyze the beam spot to a certain extent without using the computer; such results are immediately available for tuning or steering the beam. Specifically, one can obtain a contour of equal beam flux at any chosen level, as well as readouts of the total beam intensity in the frame and the total intensity above the selected level. In addition, cells in which the intensity is within 12% of saturating the system are cross-hatched in the video display as a warning.

Section II of this paper discusses the system from the point of view of the person who wishes to use it correctly but is not interested in the electronic details. Section III is a detailed circuit description. Our very limited operating experience with the system is summarized in Section IV.

II. GENERAL DESCRIPTION

A. Input/Output Specifications

1. Camera Interface

a. Test/Operate Switch

Use TEST for stand-alone operation to aim and focus camera, or for bench testing camera/interface system; otherwise use OPERATE.

b. Inputs/Outputs

CAMERA IN and VIDEO IN must be connected to the camera.

X, Y, and Z can be used to drive an X-Y scope in stand-alone mode. Z is the video signal passed through an inverting AGC amplifier, usually VIDEO

OUT works better for aiming/focussing.

CLOCK IN is the timing connection to the logger module.

This line is terminated (50 Ω) at both ends. Positive, 150 mV clock pulses are sent from the logger to the interface where they cause the selection of the next picture element. If this is an active element (that is, not one of the dummy diodes at the ends of the line), the interface returns a negative TAKE pulse to the logger on the same cable.

VIDEO OUT is the video connection to the logger module.

The signal at this point is negative and about 6 volts max.

EOF OUT is the end-of-frame signal from the camera and

TRIG OUT is a scope trigger generated in TEST mode. These are not generally used.

Summary: For normal operation CAMERA IN and VIDEO IN are connected to camera, CLOCK IN and VIDEO OUT are connected to the logger via long 50 Ω cables and the switch is in OPERATE position.

2. Logger Module

a. Power

+24	100 mA
+6	520 mA
-6	20 mA
-24	30 mA

b. Controls

START DELAY is set so that beam pulse occurs midway between "clear" and "real" scans on TIMING MONITOR. Screwdriver STRT DEL. gives additional range.

TEST/CLEAR push button puts module in HOLD state and selects the next test mode (0, 1, checkerboard, address) each time it is

pushed. HOLD delay is updated by CAMAC C function if the computer is being used; otherwise it times out returning the module to "tracking" mode.

c. Inputs/Outputs

BEAM is a NIM input which should be synchronous with the beam (although an error or jitter of many microseconds is tolerable). BEAM pulses should not be gated.

ARM is a NIM pulse which is applied when the module is used in HOLD mode to prime the module to take the next possible beam event.

CLOCK and VIDEO are described in previous section.

VIDEO MON is the video signal as seen by the ADC.

TIMING MON is a superposition of the BEAM pulse and internal memory WRITE pulses. It gives a general idea of when the module is scanning the Reticon, transferring data to the display module, and transferring data to CAMAC. A large short negative spike is put in as the logger switches to MEASURE state; this can be used to trigger the scope.

d. Screwdriver Adjustments

STRT DEL is a logical extension of the START DELAY pot.

HOLD determines the HOLD timeout, that is, the length of time CAMAC may remain inactive before the logger module reverts to tracking mode.

SETTLE determines how long the ADC waits after the next picture element is selected, before digitizing (see Section IIC for timing adjustments).

GAIN should be set so that a very bright picture saturates at +12 volts as seen at VID MON. This guarantees that the ADC will be the linearity-limiting element in the system and, therefore, that the overload warning which occurs at 87% of full range will be valid.

OFFSET is set so that every picture element gives a positive output (only then will a background subtraction be valid). See Fig. 1 for an example. Note: If this adjustment cannot be made, it probably means that the camera is out of adjustment and may be suffering radiation damage; offset level drift appears to be the first sign.

e. CAMAC Protocol

The module is read by successive $F\phi$'s in a stop-mode block transfer of 1024 x 10-bit words (Q asserted on every valid word, deasserted on first word past block). First the module must be put in HOLD mode by a CAMAC C (CLEAR) function.

A number written into the logger module by F16, after the CAMAC C, will cause the next cycle (which must still be initiated by BEAM and ARM pulses) to be one of four memory tests: write 4 for all zeros, 5 for all ones, 6 for checkerboard (alternating all zeros and all ones) and 7 for address test (each word contains its own address). The next event after the test will be normal. One may also step through the tests by pushing the button at the logger.

Incidentally, the tests can be checked quantitatively using the external scaler, without using the computer. The zeros test gives a blank display; ones test gives $(1023 \times 1024) = 1047552$ and the checkerboard and address tests each give half that or 523776. This will

show up even one bad bit. Of course, the ROI scaler will read less unless the ROI is first set to full field with the aid of the ones test.

3. Display Module

The display module controls and settings are used for stand-alone display and analysis of the beam profile and have no effect on the CAMAC data. The module itself is, however, necessary since the logger will not complete its cycle without it.

a. Power

+24	30 mA
+6	540 mA
-6	5 mA
-24	25 mA

b. Controls

SLICE LEVEL selects a beam intensity contour in the black/white display mode.

GRAY or B/W display switch selects a halftone or black-and-white display of the beam spot. The latter is used either to display the cells above the SLICE level or to display the memorized region-of-interest (ROI), by appropriately setting the ROI/SLICE toggle.

SET ROI will memorize the displayed contour when the toggles are on B/W and SLICE (both down). In other words, to change the ROI you must be looking at the new ROI.

c. Inputs/Outputs

TV SIG delivers a channel 3 signal to a TV set. (In one module this output has been converted to deliver a video/synch "composite" signal to an external modulator.)

SCOPE TRIG provides a positive trigger at the upper

left corner of the raster (start of memory scan) for use in trouble-shooting the module.

TOTAL is a TTL level which is high while counts related to the total frame are being issued and low while counts relating only to the ROI are issued. This level is used to direct the counts to the proper external scaler.

COUNT is a stream of positive TTL pulses (approx. 5 MHz) for counting by an external scaler. Cables from TOTAL and COUNT may not be terminated and should therefore be kept fairly short.

d. Screwdriver Adjustments

SYNCH adjusts the horizontal oscillator and should be set to zero-beat the slight line-related effects you will probably see on the screen. HORIZONTAL SIZE, HORIZONTAL POSITION and VERTICAL POSITION are self-explanatory. WAIT should be set so that the WAIT one-shot in the scaler control section (IC 5J, Fig. 16F) fires for 100 msec. This allows the external scaler system to do internal housekeeping after a measurement ends and before the next one starts. If this time is too short, the scaler will give erratic results.

B. Camera Setup

In accelerator applications the camera is usually set up at a location remote from the logger and display modules. Therefore the camera interface has been designed so that it, the camera and an oscilloscope with X-Y capability will form a stand-alone system to allow the camera to be aimed and focussed. First one should consult Fig. 5 to get the camera in approximately the right position. This Figure shows, for a 50 mm lens and various extender rings, the range of object distances

(measured from the front of the camera box) which can be accommodated and the total field width obtained at the object in each case.

Having mounted the camera at about the right distance, connect it (multiconductor cable and video cable) to the interface, switch the interface to TEST mode, and connect its X, Y and VIDEO OUT outputs to the X, Y, and Z inputs of a scope. (Interface Z, which is the video seen through a variable-gain amplifier for dynamic compression, usually works less well.) You should immediately see a 32 x 32 raster if the camera/interface is working at all. Whether you see an image depends critically on:

Focus

Aiming

Lens Aperture

Target Illumination (we assume there is a graticule in the target plane to act as an object)

Scope Intensity Setting

Therefore it may take some fiddling before you see your first picture; after that you can home in on the best settings fairly quickly.

The image you see on the scope (if the camera is upright) will be the same image as seen by the eye; in contrast, the image on the final TV monitor is erect (up and down are OK) but right and left are swapped.

When you leave the beam area, be sure that the scope is disconnected (and taken away); that the CLOCK IN and VIDEO OUT cables are connected and running to the control room; and that the interface is left powered and in OPERATE mode.

6. Timing

The overall timing of the system is done by the logger module and illustrated in Fig. 3. The logger is synchronized to the accelerator by an (ungated) stream of BEAM pulses. These should be approximately synchronous with the beam (for instance, at SLAC they can be the klystron triggers); however, since the figure is drawn to a scale of milliseconds, it is clear that a few microseconds "error" in the BEAM pulses will be unimportant. An ARM pulse must be provided a sufficient time before the beam pulse which one wishes to analyze.

Important: If the profile monitor is part of a larger system of detectors and it is desired that all detectors analyze the same beam pulse, the ARM pulse must itself be synchronized with the BEAM pulses. Only in this case will it be certain which beam pulse after the ARM is used. If the machine repetition rate is low enough, it will be the next pulse; if too high, one or more pulses will be skipped, but in any case the action will be predictable.

The ARM pulse initializes a shift register in the logger which has the four states STANDBY, MEASURE, VIDEO CAMAC. In the STANDBY state the logger waits for the next delayed beam pulse (internally derived from BEAM and front-panel adjustable) which will advance it to the MEASURE state. In this state the logger will perform a camera scan (to clear the Reticon array); a short wait (during which the beam should hit the scintillator) and another scan (which obtains the profile). The logger then advances to the VIDEO state. Here it waits until an appropriate time (specifically, when the display module starts its next raster scan) and then transmits the data in memory to the display module,

updating the TV picture.

The final step depends on whether the logger is in HOLD mode (which is activated either by a CAMAC C operation or by a front-panel pushbutton) or in non-HOLD ("beam tuning") mode. In HOLD, the logger will go into the CAMAC state and remain there until the data are read by the computer or HOLD times out. Another ARM pulse is then required to get back to STANDBY. In non-HOLD, the logger skips the CAMAC state and goes immediately back to STANDBY, ready for the next delayed beam pulse.

Two timing adjustments are necessary: settling time and start delay. The settling time adjustment depends only on the lengths of cables from the camera interface to the logger, and can be made on the bench using dummy cables of about the right length. (A useful test fixture for this and other purposes consists of four red LED's inserted into a circuit board on 0.2" centers in an "L" pattern. These can be pulsed through appropriate resistors with a 1 msec pulse at about 60 Hz coming from a test pulser; another pulser output is used to mimic the BEAM pulse at the same time. The waveforms of Fig. 4 were taken with such a setup.) The SETTLE pot is adjusted so that the write pulses at TIM MON occur after each voltage step at VID MON has been flat for at least two microseconds. Since the write pulse occurs just after digitizing, and the digitize time is two microseconds, this ensures that the voltage representing the output of each picture element has settled before the ADC starts. In our setup, with 500' dummy cables (750 nsec) this leads to a total cycle time of 6 microseconds corresponding to a total scan time of 7 milliseconds (there are 1152 picture elements if

one counts the two dummy diodes at each end of each line). As mentioned above, there is no need to change SETTLE provided the cable lengths stay about the same.

The START DELAY adjustment depends on the accelerator repetition rate and must be checked from time to time. It is set, using the logger front panel knob, so that a beam pulse occurs in the space between the two clusters of clock pulses at TIM MON (Fig. 4a, lower trace). This is the waiting period between the "clear" scan and the "real" scan. Obviously, the delay should be set as short as possible, that is, the logger should take the next possible beam pulse. If the knob has insufficient range, a screwdriver adjustment below it provides additional range. If START DELAY is badly mis-set, part of the picture may be lost.

III. DETAILED DESCRIPTION

A. Camera Interface (Figures 10, 11)

The MC510A camera as furnished by Reticon, though ostensibly designed to be incorporated into digital systems, presents several problems to the designer. Input logic levels are ± 7 volts. Protocol is complicated because the array is essentially designed to be self-scanning; for instance, there is no single "reset" input to return the scan to a definite point in the raster. The video output can only drive 8 feet of cable. Each line of the raster begins and ends with two dummy (inactive) cells which must be scanned but do not contribute to the picture. Finally, the camera circuit performs some operations on the leading edge of the external clock and other things on the trailing edge, so clock width is critical. These features, plus the need for a camera power supply, argue for designing an interface that will make the camera

look simpler to the outside world.

In our interface, synchronization of the camera with the logger works as follows: The logger puts out a stream of clock pulses somewhat longer than the 1152 required to get through all active and dummy cells. This guarantees that at some point the interface will detect end-of-frame (EOF), which is true during the last line of the raster, in coincidence with end-of-line (EOL) which is true during the last two cells of each line (i.e., the dummy cells). On detecting this condition the interface waits two more clock cycles and then disconnects the clock, stopping in such a way that the first clock pulse of the next scan sequence will select the second dummy cell of the first line of the raster. In other words, the interface always pauses just before the upper left corner of the raster.

In a bit more detail (see Fig. 10A): Suppose we are in the middle of a line. A clock from the logger fires CLK via the comparator IC1 and OR gate 10. The clock is passed to the camera via IC15 causing the camera to select the next cell. At the same time TEST DEL is triggered which provides time for the camera outputs to become valid. At the end of this time a short pulse from TAKE TEST will pass through the AND gate (10/3) and be returned along the clock cable to the logger, where it will cause the logger to store the selected cell after digitizing it.

If, however, the selected cell is the first dummy location at the end of the line, the camera will return EOL which sets the two-bit shift register IC7, shutting off 10/3 so that the TAKE pulse is suppressed. Accordingly the logger will digitize the cell (this keeps the basic clock

rate the same which is desirable) but not store it. Note that the shift register is held set for two cycles by EOL and then it takes two more cycles to shift out the 1's, so that four successive cycles have TAKE suppressed (two at the end of this line and two at the beginning of the next).

When the dummy cells at the end of the very last line are reached, an output from gate 10/8 (EOF and EOL) is presented to the two-bit shift register IC11. This delays cutoff of the CLK one-shot until the dummy cells at the end of the last line have been passed; if this were not done, the camer. EOF and EOL outputs would still be present and the interface would hang permanently. Accordingly the scan stops where the next clock pulse will select the second dummy cell of the first line.

As a result of the camera scan stopping, the interface puts out no more TAKE pulses. The logger responds (after a while) by not sending any more clock pulses. In turn, after a few empty clock cycles have gone by, the retriggerable one-shot IC2 resets causing the EOF shift register to be cleared. The interface is now ready to accept another clock pulse. The entire process is very similar to an interrupted phone conversation: first the interface stops talking, then the logger hangs up, then the interface hangs up.

A few miscellaneous points: CLK width should be adjusted to maximize the analog output of the camera (~ 300 nsec). The test generator (IC's 4 and 8) provides a stream of clock pulses to simulate the logger if one is not using the entire system. The camera video output is buffered by an op amp to drive a decent length of cable. Finally, a

diagnostic technique: If in stand-alone mode (interface and camera only) everything seems to be hung up, try grounding 11/8 which will let clocks through despite any camera output levels. Then check the camera responses to see whether the camera or the interface is at fault.

B. Logger Module (Figures 11, 12, 13)

1. Overview (Figure 11)

The action of the logger is strictly sequential; that is, the states STANDBY, MEASURE, VIDEO and CAMAC are controlled by a four-bit shift register and are always executed in that sequence. When the module is in STANDBY (which it reaches either because of an ARM pulse or, in non-hold mode, upon the completion of the VIDEO step), it will go to MEASURE at the next delayed beam pulse. In MEASURE, it scans the array, pauses, then scans again. The scans are identical but of course the second overwrites the first in memory so the first is effectively a "clear" scan and the second, the "real" scan. The beam delay should be set so that a beam pulse arrives during the pause.

After MEASURE, the logger sets the VIDEO bit. In response to this, the display module will scan the logger memory at the next time convenient to it (that is, starting with the beginning of its next raster scan); thus the data for the most recent beam picture are transferred to the display memory.

After this, if the module is in the HOLD mode (which is caused by a previous CAMAC C function) the CAMAC bit will be set which lets through CAMAC clock pulses and allows the memory to be scanned by CAMAC. In non-HOLD (to which the module automatically reverts if CAMAC activity stops), the module will automatically go back to STANDBY. Since

it is assumed that whenever the computer is using the system it will want to select a definite beam pulse for processing, when the CAMAC transfer is completed in HOLD mode the module does not go back to STANDBY, but requires an ARM pulse.

To summarize: The module has two basic modes of operation, non-HOLD, the "normal" mode, in which the TV picture tracks the beam as rapidly as possible, and HOLD, which is invoked by CAMAC activity and causes the module to save the data for CAMAC, then wait for another ARM pulse.

The rest of the block diagram is more or less self explanatory. The memory can accept data from three sources: two, the 0/1 gates and the address gates, are used for test data only and the third is the ADC. The memory can put out data to two places: the display module and the CAMAC backplane. The scan sequence logic controls the camera interface, the ADC and the memory address counter in such a way as to store "real" cells and sluff dummy ones (that is, those for which the interface does not return a TAKE pulse). The memory is a RAM but is in fact always addressed sequentially. Figure 7 shows the arrangement of data in memory.

2. Main Shift Register (Figures 13b and 13c)

It is perhaps worth explaining how the main shift register moves from one state to the next. The shift register clock (21/8) is the OR of three pulses. When the module is in STANDBY, a clock occurs at the next delayed trigger output (2/13) moving it to MEASURE. In this state a clock occurs at the end of scan cycle 2 (13/12), changing the state to VIDEO. When in VIDEO or CAMAC, the shift register will be

clocked by the same clock pulse that increments the memory address scaler from full count to all zeros.

In more detail: Suppose we are in VIDEO and the memory address scaler reads (full count -1), addressing the next-to-last picture element. The trailing edge of the same write pulse (32/2) that copies this cell to display memory will also increment the logger memory address (by firing CMA). The memory address counter is now at full count and its carry output goes high. The trailing edge of CMA strobes this high into the LMA ff. Therefore on the next clock (the one resulting from copying the last cell) the memory address will be loaded with all zeros and the main shift register will be advanced. In general the ADC writes before incrementing the address and each external device (display or CAMAC) copies before incrementing the address. The logger starts each major state with its memory address at zero, which is compatible with the CAMAC requirement that the data for the first word be present before CAMAC issues the first clock pulse.

3. Digitize/Write Sequence (Figure 13c)

SETTLE, ADC and WRITE form a regenerative chain which, once triggered by a low on 50/9, keeps going and puts out a clock to the interface at each WRITE pulse. Note, however, that the ADC data are actually written (and the memory address incremented) only if the TAKE ff has been set by an interface TAKE response; otherwise the data are sluffed. The SCAN retrIGGERABLE one-shot is kept fired by the stream of TAKE pulses returning from the interface; the four-cycle lapses at the end of each line are not long enough to allow SCAN to reset, but the indefinite lapse when the interface reaches the end of the frame

is long enough, and SCAN resets, firing PAUSE. This causes a high at 50/9 stopping the digitize chain and therefore, the stream of clock pulses. However, the digitize chain will again be triggered if, when PAUSE times out, the logger is still in the MEASURE state (that is, it has only completed the first scan). The CY2 ff causes the logger to go from MEASURE to VIDEO when SCAN times out for the second time, that is at the end of the "real" scan.

4. Test Generator (Figure 13a)

Pushing the button sets the TEST ff (selecting one of the two non-ADC data sources), puts the module in HOLD, sets the main shift register to STANDBY, and starts a measurement by triggering the beam delay. (In this case "beam timing" does not matter because the data are not coming from the camera.) In addition the test select register (IC12) is incremented selecting the next test. Each push of the button will cause a new test, in the sequence zeros, ones, checkerboard and address. The tests may also be exercised via CAMAC as explained in Section II.

C. Display Module

The display is a CAMAC module only for packaging and power; it does not communicate with the CAMAC backplane. It communicates with the logger module via the upper set of contact fingers. Its purpose is to provide a real-time TV picture of the beam profile, and to permit certain studies of the distribution on a stand-alone (no computer) basis: iso-flux contours and measurement of the beam in the total frame as well as the beam in a region-of-interest (ROI).

Some understanding of the basic principles of black-and-white TV

is necessary; an excellent reference (despite its age) is Terman.³

1. Overview (Figure 14)

A raster generator section, which runs continuously, generates 10-bit addresses for the main and ROI memories in the desired sequence (see next section). The main memory has been loaded with 10-bit words representing the beam intensity in each of the 32 x 32 cells ("dummy" photodiodes having been edited out by the logger module). As the address changes, the words in main memory are continuously converted back into analog (0 to 5 volts) by a DAC. In the "gray" display mode the DAC output goes directly to a modulator which combines the DAC output with horizontal and vertical synch pulses from the raster generator to modulate the video oscillator. A picture can be obtained on any normal TV set tuned to channel 3.

The DAC output also drives a comparator which puts out a signal whenever the DAC is above an adjustable "slice" level. In the "BLACK/WHITE" display mode, this output (instead of the DAC) drives the modulator, and one obtains a picture with white zones wherever the beam intensity is above the slice level. If the display select is on B/W and SLICE the current white zones can be memorized by pushing "SET ROI". This allows one to explore the effect of focussing, steering, etc., in a fixed ROI. In the B/W mode either the current beam-above-slice or the memorized ROI may be displayed.

When the data on the main memory bus have the three most significant bits set, an overload warning oscillator is activated, cross-hatching the display as a warning that one is within 12.5% of full scale.

Finally, the sum of all ADC outputs in the entire frame

("TOTAL" region) and the sum of all counts in the ROI may be read using a supplementary decimal scaler. As the raster generator sweeps through the main memory, the data in each cell are added (once) to the counts in an accumulator, by a binary adder. When all cells have been added, the accumulator (which is also an up/down counter) is counted back down to zero, generating a clock pulse train equal to the total count. This pulse train, put out on the "COUNT" connector, is counted in the external scaler and latched for a decimal display of the total. The whole process is done twice, once for all cells and again for cells above the SLICE level (or listed in the ROI memory). The TTL signal on the "TOTAL" output is true during the TOTAL cycle and false during the ROI cycle, allowing external circuitry to steer the counts to one of two scalers.

2. Raster Generator (Figures 7 and 16a)

The TV signal departs from the black-and-white standard in a few respects. First, there is no interlace; this is done for simplicity and because⁴ interlace actually causes objectionable flicker in "digital" displays of this kind. Second, we use 256 lines per field instead of the ideal 262.5, again for simplicity.

For the desired picture (see Fig. 6d) the main memory must be scanned as shown in Fig. 7. This is done by the raster generator section (Fig. 16a) which is best thought of as two five-bit counters, a "column" counter (IC's 39, 30) and a "row" counter (31 and 3 with associated gates). In addition there is a six-state "lines per row" counter (IC 12). All these counters are synchronous, so that all address bits change simultaneously. The field will have 192 (32 x 6) active lines. The column circuitry will keep going during the inactive lines (to maintain horizontal

synch) but the lines-per-row and row counters will be shut off.

Suppose we are coming into the upper left-hand corner of the raster (Fig. 7). A negative signal from the horizontal oscillator (which is set at 65.1 μ sec so that 256 cycles take 1/60 sec) resets the horizontal blanking (HBLNK) flip-flop and, via the ± 256 counter, triggers the RESET (R) pulser which resets the column and row counters as well as VBLNK. Resetting HBLNK turns on the box width oscillator (IC 48) which after about 1.3 μ sec (the width of one cell) puts out a clock pulse incrementing the column address. This action continues until the column counter carries (during address 31) whereupon the next clock pulse will increment the lines-per-row counter and set HBLNK, shutting off the box width oscillator. We have finished the first line of the first row. A while later the horizontal oscillator again resets HBLNK starting the second line of the first row. After six lines (the number is chosen to make the display approximately square) the lines-per-row counter carries; on the next line it will be set back to 10 and the row counter will be incremented. When the row counter finally carries (2/6 goes low) we are on the last line of the last column of the last row. The next clock pulse will set VBLNK.

3. Synch and Modulator (Figure 16e)

The synch pulses are generated by one-shots triggered respectively by HBLNK and VBLNK. These are combined in the EX OR (IC 28) so that the horizontal synch pulses appear as notches during the vertical synch pulse (this helps maintain horizontal synch). A word about the raster adjustments: Overall synch is adjusted by adjusting the horizontal oscillator (SYNCH adjustment); the easiest way to do this is to

zero-beat the slowly moving pattern which invariably appears on the display due to residual 60 Hz effects. The width of the picture is adjusted by means of the basic cell size (H SIZE). The position is adjusted by varying the timing of the horizontal and vertical synch pulses in their respective blanking periods (H POS and V POS).

Returning to the modulator: The video oscillator is a Colpitts modulated on the principle that the oscillation amplitude is inversely proportional to base/emitter dynamic resistance which in turn is inversely proportional to standing current. (Hence amplitude is proportional to collector current.) The emitter current is changed by adding to or subtracting from the basic standing current using 4066 CMOS switches. The basic current represents black or about 75% of full amplitude; the synch pulses add current (and override any video input) while the video signal (which is either a quantized signal for black-and-white mode or an analog signal for grey mode) takes away emitter current.

4. Composite Output (Figure 16i)

In one application it was desired to drive a commercial video modulator allowing the TV signal to be put out on long "public" cables for remote viewing (instead of using a dedicated local TV set). Our oscillator signal has far too many sidebands to be used except locally at low power. Therefore one module was modified to provide a composite (synch plus video) signal with no carrier. This is done by killing the oscillator so that it acts only as a linear adder, then providing a little gain with a 733 amplifier. Unfortunately the module must be set up one way or the other; if the module is ever redesigned it would be nice to add enough circuitry to bring the signal out both ways.

5. Display Select (Figure 16d)

This page is fairly self-explanatory. The SLICE comparator is actually latched a short time after the DAC settles to ensure definite results for a given line. The ROI memory is write-enabled only if the button is pushed and B/W and SLICE are selected (that is, you must be looking at the new pattern in order to memorize it). The "quantized" video level comes either from the slice latch or the ROI memory depending on the switch setting. The overload oscillator puts glitches into both the gray and black/white gates so that the overload warning works on all displays.

6. Adder and Counter Control (Figures 8 and 16f)

This circuitry and the associated external scaler are useful for beam diagnostics if a computer and/or appropriate software are not available. Figure 8 is a timing diagram. Assume we are at the left side. Pin 27/8 is down ($\overline{\text{ADD} \cdot \text{COUNT} \cdot \text{WAIT}}$ is true) so the next R pulse from the raster generator (signifying the upper left corner of the picture) will set ADD. (Note that the ADD ff has inverted logic; that is, 45/6 is ADD, not 45/5.) In the ADD state, the accumulator/scaler (IC's on the right, Fig. 16c) will be loaded with the adder output (representing the accumulator itself plus the current cell) during the last line of each cell by an update (UPD) pulse. If TOT is true, this is done for all cells; if not, only for cells for which QUANT is true (this may be either the slice latch or the ROI memory depending on display mode). Using the last line assures that each cell will be counted just once. ADD is reset by the next R pulse. At this point the accumulator/scaler contains either the total counts in the picture (for TOT) or the counts in the selected

or memorized region (for $\overline{\text{TOT}}$).

For reasons having to do with the particular external scaler used (see Section III.D.) we must now wait about 100 msec before starting to put out a pulse train (WAIT adjustment). When WAIT times out, it sets the COUNT FF. This starts a countdown oscillator consisting of a TEST one-shot triggering a COUNT one-shot. The leading edge of TEST strobes the RCO (ripple carry out) level from the accumulator/scaler into an RCO FF; if RCO is false, the scaler is decremented and a pulse is put out on the COUNT connector to the external scaler; if true, the pulse is instead used to turn off COUNT. This arrangement ensures that if the accumulator/scaler is at zero at the start of the COUNT period, no counts (rather than one) will be put out.

In the external scaler the count train will (effectively) be steered to one of two scalers depending on the state of TOT. Thus one will display all counts, the other, counts in the region of interest (or above the slice level).

7. Video Transfer (Figure 16g)

Like many other operations, video transfer (from the logger) is done during the last line of each cell. When the VIDEO level (J2/12) is asserted by the logger, it means that the logger has paused with its memory address at zero (upper left corner). Nothing will happen until the display raster generator reaches the upper left corner at which time the XFER ff will be set by the R pulse. Thereafter, at the clock pulse heralding the last line of each cell, that cell will be written into the display memory and the logger memory address will be incremented selecting the next cell. (The logger circuitry ensures that this will

happen after the copy.) After one field the entire logger memory will have been copied. The next R pulse resets XFER. The logger already knows the copy is complete because 1024 WE pulses came through.

D. Scaler

The external scaler is optional and may be used to display the beam intensity in the total frame as well as the intensity in the region of interest (ROI). We use two Intersil counter evaluation kits³ mounted behind a 3 1/2" panel together with a 5 volt power supply. The PC boards in the kit are cut so as to provide a stand-up front panel display; otherwise the kits are assembled per instruction. The FUNCTION switch is set to RATIO A/B, RANGE is set to 0.01 Sec/1 cycle, and the DIP switch is set for external decimal point enable (but no external decimal point is supplied).

The purpose of the scalers is to count the pulse train coming from the display module and then display it. A small amount of additional circuitry (Fig. 17), which can be built in the breadboarding area, serves to (effectively) route the counts either to the TOTAL or ROI scalers, using the TOTAL signal from the display module.

At first it might seem more logical to use the scalers in UNIT mode where they function as simple counters. However in this mode the display is continuous so that one would see the numbers changing most of the time. In RATIO mode the display is updated only when the measurement is finished; therefore, we obtain a static display which changes only as the answer changes. In RATIO mode when the scale is set to one cycle, the scaler counts the A input for one cycle of the B input; in other words, all A pulses which occur between two successive B pulses.

The scaler control circuitry (Fig. 17) may be understood with the aid of Fig. 8. Suppose that we are at the instant where TOT goes high. This means that an ROI measurement has just ended. Note that the B input is supplied only for the ROI scaler; this "completes" the measurement and causes the result to be latched and displayed. The TOT scaler thinks it is still measuring. 100 millisec later a HOLD pulse is applied to both channels. This has no effect on ROI which is already latched, but in the case of the TOT scaler, it resets the count and does not display it; effectively, it flushes the counts which were accumulated in the TOT channel.

Important: HOLD must be delayed at least 100 msec after the completion of a measurement, specifically, after the scaler STORE pulse ends. This allows the chip to do some internal housekeeping. This feature is not at all clear from the Intersil data sheet. To save some circuitry, we use a fixed delay rather than the STORE signal itself.

After the HOLD pulse, both channels receive a B input which starts the next measurement. In this cycle the roles will be reversed; TOT will receive another B pulse (when the TOT level goes low) before the next HOLD, but ROI will not; therefore the TOT scaler will be latched and displayed and the ROI scaler will be flushed. In Fig. 8, the arrows flag complete measurements.

We mention in passing that the evaluation kit sells for about \$80 and is a very powerful bit of electronics for the money. Because of the many things this chip can do, the data sheet is not always totally clear, but it repays study.

E. Aperture Control (Figure 18)

During a test program the beam intensity is apt to vary a great deal due to changes in focussing, etc. Because of the limited dynamic range ($\sim 100/1$) of the Reticon it is essential to have a remote aperture control. This is done using a small DC motor driving an O ring which is used as a belt drive; at the end of travel it slips, eliminating the need for limit switches. The OPEN and CLOSE switches are interconnected so that nothing bad will happen if both are pushed (some wag is bound to try this sooner or later). The LEDs indicate current not voltage so they will light only if the circuit is complete.

F. Glossary of Acronyms

1. Interface

RETR	retrigger (on incoming clocks)
EOC	end of clocks
CLK	clock
TAKE	a negative pulse back to the logger which will cause it to store the data
EOF	end-of-frame
EOL	end-of-line

2. Logger

T1, T2	bits of test select register
RT1	reset T1
ST1	set T1
CS2	CAMAC S2 gated with function C
ISR	initialize shift register
TRIG	trigger (used synonymously with BEAM)
TRD1	trigger delay 1
DELT	delayed trigger
CSR	clock (advance) shift register

Q	CAMAC Q response
CY2	flip-flop which is true during second scan cycle
NFØS2	CAMAC FØ function gated with N and S2 (also, at pin 32/1, with CAMAC ff)
CNA	clock (increment or load) memory address
LNA	load memory address
WE	write enable
MAF	memory address full
Ø/1	a data source which is all zeros or all ones
DØ	data bit zero (least significant)
RI	read line 1 (least significant)
W3	write line 3

3. Display

VBLNK	vertical blank
HELNK	horizontal blank
LL	last line (of a row)
C	clock (cell to cell)
R	reset (upper left corner of raster)
ROI	region of interest
CE	Chip enable
QUANT	quantized version of the half-tone image (that is, either black or white)
VSD	vertical synch delay
VSX	vertical synch
VBL	same as VBLNK
TV	television
UPD	update (accumulator)
RCO	ripple carry out (when scaler is full or zero depending on up/down)

Miscellaneous Notes:

1. Except for the 18 pin memory chips, 16 pin sockets were used throughout in the first production models; the spare pins (if any) are useful as tie points for resistors, etc.; 14 pin devices are always

loaded at the top of the socket; 8 pin devices in the top or bottom halves or both.

2. In the writeup, 31/2 denotes pin 2 of IC 31. The IC number corresponds to the location on the board as viewed from the pin side (example: Fig. 12).

3. R, L denote right and left if the chip splits that way (example: LS74) and U, L denote upper and lower for chips like the LS221, or where two 8 pin chips are socketed.

4. Chips are drawn according to their positive-logic function (example: an LS00 is drawn as a NAND even if used as a negative NOR).

IV. OPERATING EXPERIENCE

Three monitor systems have been used for several months of linac tests so we can say that overall performance is reliable. However both instantaneous and (because of the great variety of linac operations) integrated beam dosimetry are difficult at the injector end of the linac where the device was used, so we have embarrassingly little quantitative data at this time. However it is probably useful to state what little we do know about sensitivity and radiation damage at this writing.

A. Sensitivity

This appears to be no problem at all with the 1 mm CsI scintillator. With the camera wide open (f 1.8) at about 12" from the scintillator one could obtain signals of a few tenths of a volt (which would already allow a profile measurement if background were subtracted) using a reasonably well focussed beam of the order of 10^7 electrons. In fact the actual beam (much more intense) eventually put a brown spot in the scintillator so it

would probably be good to design the scintillator mechanism so that fresh scintillator could be used after a while.

B. Radiation Damage

This is a very important question since the diode array alone costs over \$700. Cameras were installed in two locations in Sector 1. The downstream monitor functioned through several months of tests alternating with routine linac operations with little or no deterioration. Two cameras each failed in the upstream location within a week or so. It is known (from activation of slits, etc.) that there are large beam losses near this point. Total failure (which was traced to the logic portion of the array, not the photodiodes themselves) was preceded by gradual baseline shifts, then a large odd/even effect in the scan. The cameras were shielded by 1/8" of lead all around but this would only make matters worse if high-energy radiation is responsible.

A program is now underway to obtain more quantitative results by taping appropriate dosimeters to each fresh camera, and to improve camera lifetime by better shielding and/or greater distance from the accelerator.

V. ACKNOWLEDGEMENT

I would like to thank Bob Melen for suggesting the project; Ray Stiening for early advice (it was he who suggested the Reticon); Ev Ferrell, Bill Roster and Ray Ortiz for general help and for providing a pleasant working atmosphere; and Ted Constant, for taking over (good luck!). As always, some of the best ideas in this system came from conversations with Dave Gustavson.

REFERENCES

1. EG & G RETICON, 345 Potrero Ave., Sunnyvale, CA 94086
(408) 738-4266. We use the MC510A matrix camera which uses the RA-32x32A image sensor array. It is not necessary to buy the camera power supply, but the multiconductor cable (and female connector for same) are required for the camera interface.
2. Terman and Helliwell, "Electronic and Radio Engineering," McGraw-Hill (1955).
3. Intersil Inc., 10710 N. Tantau Ave., Cupertino, CA 95014.
We use ICM7226AEV/Kit which is an evaluation kit (including display, etc.) for the ICM7226A 10 MHz Universal Counter chip. (Kit includes the chip.) The PC board furnished with the kit can be strategically cut to arrange for a front-panel display. Otherwise, it is best to start by assembling the kit according to instructions.
4. D. Gustavson, private communication.

FIGURE CAPTIONS

1. Computer-generated three-dimensional representation of a profile of the SLAC beam, obtained with the monitor during linac tests.
2. Block diagram of the monitor system.
3. Timing diagram for the logger module.
4. Timing waveforms obtained with an LED array acting as object.

(a) Upper trace: video monitor output at 5 V/div; lower trace, timing monitor output at 0.1 V/div; sweep speed 2 msec/div. Each scan takes 7 msec and "start delay" has been set so that the beam occurs during the pause between the "clear" and "real" scans.

(b) The same at 0.1 msec/div. showing the first few lines of the "clear" scan. (c) The same using a delayed sweep at 2 μ sec/div; this shows that the cycle time is 6 μ sec and that the settling-time adjustment is correct: the voltage steps are flat for at least 2 μ sec before the "write" pulse starts. (d) Video picture corresponding to these waveforms. LED spacing was 0.2" on centers; only three LED's are visible, and the image has been deliberately defocused to mimic beam. The gray areas near the center of each spot (which in a better photograph would show as cross-hatched) warn of a near-overload condition there.
5. Graph to aid in camera setup: object field width versus object distance (measured from front of camera box) for a 50 mm lens with various extender rings.
6. Three memory tests and the LED pattern: (a) all ones; (b) checkerboard (alternating all ones and all zeros); (c) address test (each cell contains its own address); (d) the LED pattern. The "all zeros"

test has been left out since it would be a totally black frame). The bottom of the address test is gray because of the overload warning. The LED picture shows an odd/even effect in the background, symptomatic of camera misadjustment or possibly, slight radiation damage.

7. How the raster is generated by the display module.
8. Timing waveforms connected with the external scaler (see text).
9. Camera interface, IC layout.
10. Camera interface circuits:
 - a. main board
 - b. power supplies and video buffer amplifier
 - c. interconnect cable
11. Logger module, block diagram.
12. Logger module, IC layout.
13. Logger module, circuits:
 - a. test and arm
 - b. trigger delay, main shift register
 - c. digitize, write, increment memory address
 - d. memory address bus
 - e. data bus
 - f. CAMAC-associated circuits
 - g. voltage regulators
14. Display module, block diagram.
15. Display module, IC layout.
16. Display module, circuits:
 - a. raster generator
 - b. address bus

- c. data bus
 - d. display mode select
 - e. synch generator and modulator
 - f. adder and counter control
 - g. video transfer
 - h. voltage regulators
 - i. alternative output (video/synch composite signal)
- 17. Scaler control.
 - 18. Aperture control.

FIG. 1. Computer-generated three-dimensional representation of a profile of the SLAC beam, obtained with the monitor during linac tests.

FIG. 2. Block diagram of the monitor system.

FIG. 3. Timing diagram for the logger module.

(a)

(b)

(c)

(d)

8-81

4169A5

FIG. 4

8-81

4169A4

FIG. 5. Graph to aid in camera setup: object field width versus object distance (measured from front of camera box) for a 50 mm lens with various extender rings.

(a)

(b)

(c)

(d)

8-81

4169A8

FIG. 6

FIG. 7. How the raster is generated by the display module.

8-81
4169A9

FIG. 8. Timing waveforms connected with the external scaler (see text).

1 710	2 LS123 RETR EOC	3 LS221 CLK TEST DEL	4 555 TEST 0 CLK 0 TEST
5	6 LS221 "TAKE" TEST	7 LS74 EOL 1 EOL 2	8 LS221 TEST GEN
9	10 LS00 RETR TAKE EOF EOL	11 LS74 EOF 2 EOF 1	12
13 AD579	14 CAMERA I/O	15 4011 (4001) CLOCK DRIVER	16 -15 +15 +12 +5 -6

(PIN VIEW)

FIGURE 9 : IC LAYOUT

CAMERA INT'FACE
DG 12/15/80

FIGURE 10 B : VOLTAGE REGULATORS , VIDEO BUFFER

CAMERA CONNECTOR :
(LOOKING AT FRONT OF CONN.)

SOCKET 14, CAMERA I/O :

16	+15	1	EXT START Y
15	TO CAM	2	" " X
14	-15	3	NC
13	TO CAM	4	EOL
12	-7 FROM CAM	5	EXT ϕ
11	CLOCK	6	EOF
10	INIT	7	CLK MODE
9	EXT CLK TO CAM	8	GROUND

FIGURE 10 C

CAMERA INT'FACE

DG 12/15/80

FIG. 11. Logger module, block diagram.

BOTTOM (PIN) VIEW

FIGURE 12 : IC LAYOUT

LOGGER
326 1/26/81

FIGURE 13 A: TEST & ARM

FIGURE 13 C : DIGITIZE, WRITE, COUNT

FIGURE 13 E : DATA

LOGGER
BxG 2/24/81

(LOWER
 CARD-EDGE
 CONNECTOR)

C19-20, R33-34

FIGURE 13 F : CAMAC

LOGGER
 Bx6 3/25/81

C21-27, R35-36

FIGURE 13G: VOLTAGE REGULATORS

LOGGER
DxG 3/27/81

FIG. 14. Display module, block diagram.

(LOOKING AT PINS)

FIGURE 15 : IC LAYOUT

DISPLAY
TBXG 5/6/81

FIGURE 16 B : ADDRESS BUS

DISPLAY
B-6 5/13/81

FIGURE 16D: DISPLAY SELECT

DISPLAY
Bx6 5/12/81

* : AS NEEDED FOR CHAN. 3

L1 : 4 TURNS BUS WIRE,
1/2" LONG ON 1/4" FORM

FIGURE 16E: SYNC. & MODULATOR

DISPLAY
DIG 5/14/81

	1	1	
GROUND	16	1	15
	14	1	13
VIDEO	12	1	11
	10	1	9
D9	8	1	7
D7	6	1	5
D5	4	1	3
D3	2	1	1
D1			

DISPLAY
BKG 5/13/81

78xx : (TAB = COMMON) OUT
COMMON
IN

79xx : (TAB = IN) OUT
IN
COMMON

FIGURE 16H: REGULATORS

DISPLAY
13x6 5/13/81

THIS CIRCUIT MAY REPLACE THE VIDEO
OSCILLATOR TO BRING OUT A COMPOSITE
(VIDEO + SYNC) SIGNAL FOR USE
WITH AN EXTERNAL MODULATOR.

FIGURE 16 I : COMPOSITE OUTPUT

DISPLAY
T3xG 8/14/81

ALL ~ 10 μ SEC EXCEPT
WAIT1 ~ 100 MILLISEC

FIGURE 17: SCALER CONTROL

PROFILE
BXG 8/14/81

TRIAD F91-X

CAMERA 1
CHANNEL IS SHOWN ;
CAMERA 2
CHANNEL IS
IDENTICAL.

CAMERA 1

USE 24 V/120 mA
DC MOTOR. CONNECT
SO THAT + ON BMC
CENTER CONDUCTOR
OPENS APERTURE.

FIGURE 18 : APERTURE DRIVE SUPPLY & CONTROL