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FASTBUS REVIEW 1985*

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ABSTRACT

The progress of developments based on the FASTBUS Specification DOE/ER-0189 for modular high-speed data acquisition and control systems is reviewed.[1] Available hardware components and efforts in standardized FASTBUS software are summarized. The status of FASTBUS applications at research laboratories in North America is reported.

FASTBUS work in Europe and Japan is presented in other papers at this conference.[2,3] Due to the highly condensed nature of this review, background information and references from reports at the 1983 and 1984 Nuclear Science Symposia may be useful.[4]

1. STATUS OF FASTBUS SPECIFICATION

The FASTBUS Specification DOE/ER-0189 has been updated by a Supplement (April 1985) and Addenda and Errata dated 28 June 1985 and 21 August 1985.

Highlights of these updates are:

- Added broadcast case 3a for "Device Available Scan" and case 6 for CSR#0 (05) scan (SR asserted).
- Recommended front panel mounting holes on module printed circuit board.
- Recommended grounding area for static charge control on module printed circuit board.
- Mandatory crate contacts for static charge control.
- Revision of table of recommended module connectors for crate segment.

Printing of the FASTBUS Specifications as ANSI/IEEE STD 960-1985 is in progress. Distribution by IEEE is expected by the end of 1985. This document will incorporate all updates published to-date.

Preparation of the FASTBUS Specification as a standard of the International Electrotechnical Commission (IEC) is underway.

A tutorial short course on FASTBUS has been presented again by members of the U.S. NIM Committee as part of this Conference.

2. HARDWARE NEWS

The FASTBUS hardware commercial market has exploded in the past two years. In 1983 a crate, power supply, and blower combination from J. White Company and a two-layer kluge card from Scientific Systems International/Kinetic Systems Inc. were the only pieces of FASTBUS hardware commercially available in the United States. Table 1 depicts a list of U.S. manufacturers offering FASTBUS hardware today.

TABLE 1

1. Astro Dynamics, Inc.	Fan Units
2. BiRa Systems	Segment Display Modules Crate Segment Ancillary Logic
3. Integrated Networks	Cable Segment Drivers
4. Interface Standards, Inc.	Crates, Power Supplies, and Blowers Crate Segment Ancillary Logic
5. Kinetic Systems, Inc.	Crates and Power Supplies Crate and Cable Segment Ancillary Logic Segment Interconnects VAX/PDP-11 Computer Interface (UPI) Active and Passive Extenders Kluge Cards Block Mover* and Fast Sequencer* Three-Crate Air/Water Exchanger-Cooled Rack
6. LeCroy Research Systems Corp.	96 Channel 12 and 15 Bit ADCs 96 Channel 8 and 9 Bit TDCs Image Chamber Analyzer Module Segment Manager/Interface (SM/I) CAMAC Register Interface, Active Extender
7. McLean Midwest	Air/Water Heat Exchanger
8. NYCB Real-Time Computing, Inc.	VAX-DDI Interface FASTBUS Microvax Master* Image Processing Systems
9. Valtronic, Inc.	Slave Control Logic Hybrid

*Planned Or Under Development.

A FASTBUS Hardware Compendium[5] has been assembled which details all European, Japanese, and American manufacturers, their products and addresses. It also contains a partial list of laboratory or university FASTBUS hardware projects finished or under development which are of general interest to the FASTBUS community along with contacts for these projects.

Figure 1 shows one of the most significant hardware developments in FASTBUS. Nine European, Japanese and American institutions and companies have combined for a joint prototype development effort and production quantity purchase[6] of a VLSI integrated circuit for interfacing via ECL/TTL converters to the Address/Data lines of the FASTBUS segment bus. The IC, called the ADI, was manufactured by Fujitsu in Japan. 110 prototypes have been made thus far and are presently being tested at Fermilab. Another 3,000 production ADI ICs are on order with an expected February/March 1986 delivery time. The ADI is a 1100 equivalent gate, 88 lead pin-grid gate-array IC utilizing LSTTL technology. It interfaces 16 of the 32 address/data lines; thus two are needed per module.

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Fig. 1. 16-Bit ADI Gate-Array Integrated Circuit.

A hybrid IC, called the SCL, consisting of three TTL PALs and a few SSI ICs has been fabricated and is now under test. This hybrid implements much of the control circuitry necessary in a FASTBUS interface such that with two ADI ICs, an SCL and ECL/ TTL translators, a user has an almost complete Slave interface to FASTBUS.[7] After experience has been gained using ADI and SCL devices to implement module designs, a gate-array realization of the SCL functions is planned.

3. STATUS OF FASTBUS SOFTWARE

The Software Working Group has put its main efforts into a revision of the draft Standard Subroutines for FASTBUS. The revised draft is more comprehensive in its scope, providing better support for large multi-user environments and increased software portability, and reflects experience gained with the earlier draft standard. Consensus is evident on the main features of the document, but work continues on questions such as which features should be mandatory, and what subsets or levels of implementation should be permitted.

The software problem is complicated by the existence of a wide variety of hardware interfaces, some of which have limitations or peculiarities which are not appropriate for support by a standard. Eventually, the existence of a software standard should clarify what hardware interface behavior is desireable, and thus encourage the production of good supporting hardware. Meanwhile, software emulation of missing features may make some interfaces run rather slowly in certain modes of operation. Portability of programs from one installation to another may be possible, using the Standard Subroutines interface, but local optimizations will be needed in some cases to get the desired performance on the local hardware.

The Software Working Group is responsible for the allocation of standard Control/Status Registers, and has recently added a set of timer duration controls, at addresses 1C through 1F, corresponding to the timers controlled by bits 4 through 7 in CSR# 9.

Projects which will be undertaken soon include re-thinking of the FASTBUS interrupt handling scheme, particularly in connection with the Standard Subroutines, and consideration of the software interface to Buffered Interconnect devices.

The FASTBUS User's Handbook, which was prepared by the Software Working Group several years ago, has become rather outdated, and the SWG is cooperating with the new FASTBUS User's Guide Working Group in transferring useful material to the new Guide, and updating and creating new material as needed.

Software implementations supporting FASTBUS have grown considerably in the past year. Rather than trying to list all the activity in that area here, we suggest interested parties contact labs using similar equipment to get the current status and availability of support software.

4. REVIEW OF FASTBUS APPLICATIONS

Activities in FASTBUS applications have ranged from operation of several small data acquisition systems, installation and testing of major portions of the CDF system at FNAL and the Mark II/SLC system at SLAC, to planning and development of several new FASTBUS systems. It should be emphasized that the laboratories listed in this review are the host facilities for these experiments and that a significant FASTBUS development effort is also taking place at collaborating institutions.

1. BNL - Brookhaven National Laboratory. A single crate system for MPSII is in operation; E787 is planning a small system of ADCs and TDCs for late 1986.
   (a) Experiment E802. Data acquisition system for single - arm magnetic spectrometer for relativistic nuclei collisions will include one or two FASTBUS crates with pipeline TDCs. Main parts of DAQ system will utilize CAMAC and VME. First operation expected early next year.[8]
   (b) Experiment NA36 (Later E810). Data acquisition system for a heavy ion experiment at SPS at CERN in October 1986. Very high speed data collection and recording implemented with 5 crate segments. E810 will employ a similar system one year later at AGS at BNL.[9]
2. FNAL-Fermi National Accelerator Laboratory. The year 1985 was a milestone for FASTBUS at FNAL. Four experiments (E636, 653, 665 and 687) with approximately 19 crates of FASTBUS equipment became operational. Two additional experiments, E706 Direct Photon Production Experiment and E740 DO Collider Detector, are planning or considering FASTBUS usage. Installation and testing of the CDF system is proceeding.[10]
   (a) CDF - Collider Detector Facility. Detector with 75K signal channels; FASTBUS data acquisition system with 60 crate segments, 4 cable segments, 32 SIs; approximately 30% of system is installed and being tested; completion of system scheduled by October 1986. Figure 2 shows the installation of the detector at the BO interaction region of the p^+p^- collider at FNAL.
3. LANL - Los Alamos National Laboratory. Prototype development and testing of FASTBUS hardware for multiple single crate front-end data acquisition systems for the Weapons Neutron Facility is continuing.[11]
4. LBL - Lawrence Berkeley Laboratory. The data acquisition system for the Di-Lepton Spectrometer includes one crate of commercial FASTBUS TDCs and ADCs interfaced with a LeCroy 1821 SM/I to CAMAC.[12]
5. SLAC - Stanford Linear Accelerator Center. Construction of the Stanford Linear Collider (SLC) is progressing toward the October 1986 completion date.[13] Accelerator improvements and additions such as damping rings, electron and positron sources, 50 MW klystrons are well underway. The Arc tunnels are being outfitted with the beam transport components, the Collider Experimental Hall is scheduled for completion by March 1986 (Fig. 3). FASTBUS

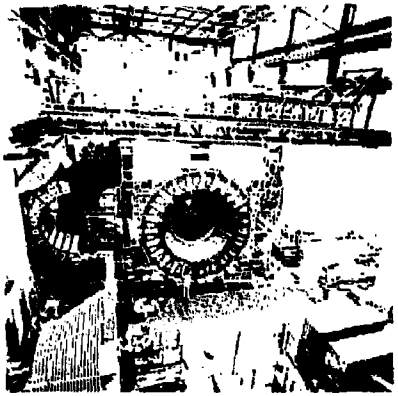

Fig. 2. Collider Detector Facility at FNAL.

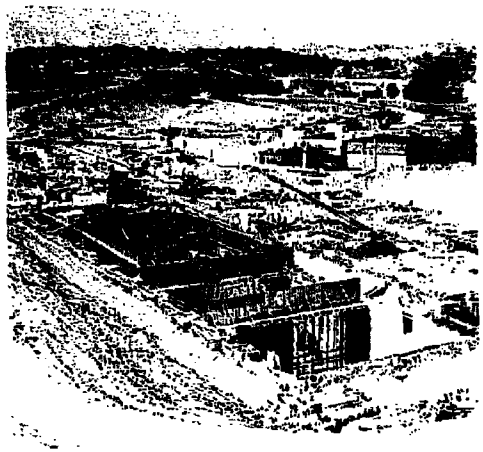

Fig. 3. SLAC Collider Experimental Hall.

data acquisition systems for SLC detectors Mark II/SLC and SLD are in preparation.[14]

(a) Mark II/SLC Upgrade Data Acquisition System. A FASTBUS system for 20K signal channels with 23 crates and 6 cable segments is being assembled. Parts of this system have been installed and are being tested at the PEP storage ring.

(b) SLD Detector. The data acquisition system will be implemented entirely with FASTBUS including front-end electronics at the detector. The 200K signal channels will be heavily multiplexed and will require a system of only 20 crates and 8 cable segments. Completion is expected by late 1988. A significant R & D effort of front-end analog circuitry utilizing custom monolithic integrated circuits and hybrid packaging technology is being carried out.[15]

5. SUMMARY

During 1985 FASTBUS utilization world wide moved from planning to realization with impressive growth. The estimated number of FASTBUS crates installed for data acquisition increased from approximately 5 in 1983 to 10 in 1984 to 50 in 1985. Based on present plans and schedules, FASTBUS usage is expected to expand to 200 to 250 crates during 1986 and to approximately 1000 crates by 1987/88. Spurred by this growth in FASTBUS application the interest by commercial industry is increasing, promising better availability of FASTBUS hardware.

The year 1985 also brought significant progress in custom interface "chip" developments to reduce overhead cost of FASTBUS. Prototypes or production units became available of two types of ADI gate-array chips, a Slave Control Logic (SCL) hybrid, two cable segment driver hybrids, and a cable segment transceiver hybrid.[16] (Fig. 4).

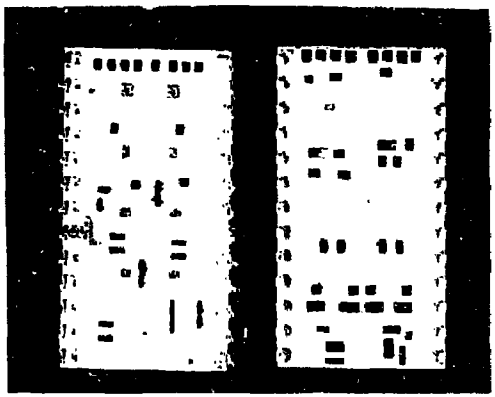

Fig. 4. Transceiver Hybrid for Cable Segment. Right: Top Substrate 4 Channel Driver; Left: Bottom Substrate 4 Channel Receiver.

During 1985 FASTBUS system complexity has increased to the level of 10 to 15 crates and FASTBUS implementation problems have moved from the crate to the system level. To help users cope with hardware, software and system design problems, a new working group was formed by the Fast System Design Group of the U.S. NIM Committee with the assignment of producing a FASTBUS User's Guide.[17]

The outlook for 1986 is exciting: we will start out with the brand-new ANSI/IEEE-STD 960 publication; next we expect the basic completion of large FASTBUS systems for CDF, Mark II/ SLC, and KEK detectors TOPAZ, VENUS and AMY; finally, FASTBUS development work for the next generation of large detectors (ALEPH, DELPHI, L3, OPAL at CERN and SLD at SLAC) will become a primary laboratory effort.

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