242
4 12-79

DR. 2466

DOE/JPL/954356-7

SILICON ON CERAMIC PROCESS

Silicon Sheet Growth and Device Development for the Large-Area Silicon Sheet and Cell Development Tasks of the Low-Cost Solar Array Project, 3#

Annual Report No. 3, September 20, 1977–September 29, 1978

By

P. W. Chapman

J. D. Zook

J. D. Heaps

R. B. Maciolek

B. Koepke

B. L. Grung

C. D. Butter

S. B. Schuldt

October 31, 1978

Date Published

Work Performed Under Contract No. NAS-7-100-954356

Honeywell Corporate Material Sciences Center
Bloomington, Minnesota

MASTER

U.S. Department of Energy

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

Solar Energy

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency Thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Department of Energy, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

This report has been reproduced directly from the best available copy.

Available from the National Technical Information Service, U. S. Department of Commerce, Springfield, Virginia 22161.

Price: Paper Copy \$6.50
Microfiche \$3.00

SILICON ON CERAMIC PROCESS

Silicon Sheet Growth and Device Development for the
Large-Area Silicon Sheet and Cell Development Tasks
of the Low-Cost Solar Array Project

Annual Report No. 3

by

P. W. Chapman

J. D. Zook, J. D. Heaps

R. B. Maciolek, B. Koepke, B. L. Grung

C. D. Butter and S. B. Schuldt

Period Covered: 9/20/77 - 9/29/78

Published 31 October, 1978

Honeywell Corporate Material Sciences Center
10701 Lyndale Ave. South
Bloomington, Minnesota 55420

NOTICE

This report was prepared as an account of work sponsored by the United States Government. Neither the United States nor the United States Department of Energy, nor any of their employees, nor any of their contractors, subcontractors, or their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness or usefulness of any information, apparatus, product or process disclosed, or represents that its use would not infringe privately owned rights.

MASTER

The JPL Low-Cost Silicon Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initiate a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Institute of Technology, by agreement between NASA and DOE.

DISTRIBUTION OF THIS DOCUMENT IS UNLIMITED

THIS PAGE
WAS INTENTIONALLY
LEFT BLANK

TABLE OF CONTENTS

	<u>Page</u>
SUMMARY	1
INTRODUCTION	3
TECHNICAL DISCUSSION	5
Substrates	5
Substrate Properties	5
Slotted Substrate Development and Large Substrates	16
Dip Coating	17
Experimental Dip Coater	23
Continuous Coating	23
Initial Testing and System Modifications	24
Temperature Profiling	28
SCIM Coating Results	34
Analysis of Growth	41
The Performance of SOC Cells - Task II and Task VI	45
The Potential for Improvement	48
Series Resistance Measurements	49
Summary of Progress in SOC Cell Fabrication	52
Novel Device Development - Task VI	56
Device Modelling - Task II and Task VI	56
Slotted Contacts	56
Circular Contacts	59
Economic Analysis	61
Conductive Interface	63
BSF Metallization	65
Effect of Melt Temperature on SOC Growth	67
PROCESSING EFFORTS	74
PROJECTION OF FUTURE ACTIVITIES	75
NEW TECHNOLOGY	76
SUMMARY OF ANALYSIS AND CHARACTERIZATION DATA	77
PROGRAM STATUS UPDATE	79
REFERENCES	82
APPENDIX A - ANALYSIS OF CONDITIONS FOR HIGH-SPEED GROWTH OF SILICON SHEET	

LIST OF FIGURES

<u>Figure</u>		<u>Page</u>
1	The Alumina - Silica Phase Diagram According to Askay and Pask	7
2	Optical Micrograph (325x) of Coors S1SI Mullite	7
3	Room Temperature Fracture Strength of MV20 Mullite Plotted as a Function of Quench Temperature	10
4	Schematic Showing Specimen and Loading Arrangement Used in the Constant-Moment Test	11
5	Photomicrographs of Various Mullite Bodies (Magnification 150x)	14
6	Thermal Expansion of S1SI Mullite Containing Excess Silica	15
7	Dimensions of Slotted Substrates Produced at Coors	17
8	Vertically Slotted Substrates	20
9	Horizontally Slotted Substrate	20
10	SOC Layer Thickness, t , as a Function of Growth Speed, v , for a Number of Dip-Coating Runs Under Different Conditions	21
11	Photograph of SCIM Coater During Operational Run	25
12	Photograph of SCIM Coater Showing Buss Bars From Remotely Located Power Supplies	25
13	Original Heating-Element Arrangement in Coating Chamber of SCIM Coater	26
14	Modified Heating-Element Arrangement in Coating Chamber of SCIM Coater	27
15	Temperature Profile of First Half of Belt Furnace	30
16	Original Temperature Profile of SCIM Coater	30
17	Preheater Longitudinal Thermal Profiles	31
18	Cross-Sectional View Looking into the Preheater Compartment as Viewed From the Coating Chamber	32
19	Postheater Longitudinal Thermal Profile	33
20	Preheater Isotherms Prior to Reducing Temperature of the Lower Substrate Heater	35
21	Most-Recent Preheater Isotherms	36
22	Most-Recent Postheater Isotherms	37
23	Coating Compartment Profile Goal	39
24	Growth Chamber Cross Section Showing Adjustable Substrate Guide and Substrate Cooling Gas Ports	40

LIST OF FIGURES (CONCLUDED)

<u>Figure</u>		<u>Page</u>
25	Growth Chamber Cross Section Showing Proposed Trough Holder and Heating Element	42
26	Growth Chamber Cross Section Showing Proposed Revised Trough Holder With Molten Silicon Bath	43
27	Slotted Substrate SOC Solar Cell	47
28	Calculated Contours of Constant Power (Efficiency) Loss as a Function of Slot Spacing (Basic Unit Width), b , and Base Sheet Resistance, $R_{\square}$	48
29	Slotted-Cell Calculation of the Series Resistance	50
30	Single-Crystal Cell Calculated of the Series Resistance	51
31	Basic Design of Integral Optical Coupler	57
32	The 2x Cell	57
33	The 2x Cell Single-Crystal Substrate Without IOC	58
34	The 2x Cell Single-Crystal Substrate With IOC	58
35	Partial Lattice of Electrodes With Square Basic Units (Left)	60
36	Holes at the Intersection of Perpendicular Sets of Troughs in the Front and Back Ceramic Surfaces	60
37	RA/R_s from Equation (1) for the Circular Base Field Geometry	61
38	Meniscus Shape and Convection in SOC Growth	67
39	Temperature Profile in Silicon Near the Ceramic Boundary	68
40	Change in Melt Temperature at Fixed Velocity	69
41	Velocity/Thickness Relationship Using Equation (13)	72
42	Updated Program Plan	79
43	Updated Program Labor Summary	80
44	Updated Program Cost Summary	81

LIST OF TABLES

<u>Table</u>		<u>Page</u>
1	Initial Batch of Experimental Substrate Compositions	6
2	Semiquantitative Emission Spectrochemical Analysis of Mullite Substrates in Wt. Percent	8
3	Room Temperature Fracture Strength and Critical Quench Temperature for Mullite Refractory Substrates	9
4	Fracture Toughness Measurements on Mullite Substrate Materials	12
5	Compositions of the Second Series of Coors Experimental Substrates	13
6	Slotted SOC Cell Efficiencies	45
7	Performance of Slotted SOC Cells	46
8	Gas Flow Rate (cc/min.)	52
9	Performance of Single-Crystal Cells	54
10	Performance of Non-Slotted SOC Cells	55
11	Cost Predictions Based on Various Production Scenarios	62
12	Sheet Resistivity of Silicon Coatings (First Dip Run)	63
13	Sheet Resistivity of Silicon Coatings (Second Dip Run)	64
14	Summary of SOC with Glassy Carbon	64
15	Single-Crystal Diodes with Aluminum Back Contacts	66
16	Slotted SOC Diodes with Sintered Aluminum Paste Back Contacts	66

SUMMARY

The objective of this research program is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating one surface of carbonized ceramic substrates with a thin layer of large-grain polycrystalline silicon from the melt. During the past year, the cell development task (Task VI) of the low-cost solar array project has also sponsored work leading to the solution of solar-cell-oriented problems unique to silicon-on-ceramic material. This work is contained within this report and identified in the proper headings. In the past year, significant progress was made in all areas of the program.

Fracture toughness and thermal shock measurements were made on various mullite compositions obtained from Coors Porcelain Inc. and the Honeywell Ceramics Center. This was done to provide quality control guidelines for substrate procurement. New substrate compositions were formulated in slotted patterns that closely match the thermal expansion coefficient of silicon, thus minimizing substrate cracking. Large (10-cm x 1-m) substrates were also developed for use in our continuous coater.

The dip-coater experimentation involved using a variety of crucible positions and gas flow rates to improve coating speeds. Various slotted-substrate patterns were coated, with horizontal slots seeming to perturb the coating the least. Improvements in the purity of the coatings were correlated to the lack of impurities in the carbon parts of the dipper. Investigations indicate that the growth of silicon-on-ceramic (SOC) material is similar to EFG material, with the added advantages of no width instability or SiC particles forming on the surface.

The construction of our continuous coating facility was completed. Many modifications to the original design have been made to obtain better control of the temperature profile of the coater. Thermal conditions have been improved to the point where 1-m x 10-cm ceramic substrates will pass through the coater without breaking. Incomplete control of the thermal gradient at the solidification zone of the coater has prevented the successful continuous coating of large substrates. Spotty coatings have been obtained (150 to 250 μm thick) at growth speeds of 0.15 to 0.23 cm/sec.

An experimental dip-coater has been completed. The goal of this effort is to increase coating speeds to from 0.15 to 0.3 cm/sec without sacrificing material quality. The best slotted SOC cell fabricated to date has a 7.5 percent conversion efficiency (antireflective-coated, AM1, total area 4.1 cm^2). The pattern used contains a wide buss-bar (total pattern area 20 percent). The performance limit at this time is due

to series resistance in the top contact, not due to any fundamental limit imposed by the cell design. A standardized cell fabrication process was developed for slotted and un-slotted SOC solar cells. Series resistance in the top contact remains an unsolved problem. A satisfactory antireflective (AR) coating system was developed.

Modeling activities have concentrated on three major areas: silicon growth, device design, and economic analysis. The relationship between silicon growth speed and film thickness for dip coating is given by the expression $v^2t = \text{constant}$. This has been verified experimentally. The shape of the liquid-solid interface has been calculated in detail. Further modeling indicates that the slotted-substrate approach would not unduly penalize cell performance if the silicon was not allowed to fill the slots. An economic projection was made using standard SAMICS procedures which indicated the target cost of \$18/m² for silicon sheet could be met for certain SOC manufacturing conditions.

Glassy- carbon layers have been demonstrated to act as wetting agents and diffusion sources for doping silicon layers. No way has been developed as yet to prevent erosion of these films by the melt. This work has been temporarily discontinued.

A Back-Surface Field study was initiated using aluminum paste and sputtered aluminum as the contact. Results to date have been negative but work will continue.

INTRODUCTION

This research program started 21 October 1975. Its purpose is to investigate the technical and economic feasibility of producing solar-cell-quality sheet silicon by coating inexpensive ceramic substrates with a thin layer of polycrystalline silicon. The coating methods to be developed are directed toward a minimum-cost process for producing solar cells with a terrestrial conversion efficiency of 12 percent or greater.

By applying a graphite coating to one face of a ceramic substrate, molten silicon can be caused to wet only that graphite-coated face and produce uniform thin layers of large-grain polycrystalline silicon; thus, only a minimal quantity of silicon is consumed. A dip-coating method for putting silicon on ceramic has been shown to produce solar-cell-quality sheet silicon. This method and a continuous coating process also being investigated have excellent scale-up potential which offers an outstanding cost-effective way to manufacture large-area solar cells. The dip-coating investigation has shown that, as the substrate is pulled from the molten silicon, crystallization continues to occur from previously grown silicon. Therefore, as the substrate length is increased (as would be the case in a scaled-up process), the expectancy for larger crystallites increases.

A variety of ceramic materials have been dip coated with silicon. The investigation has shown that mullite substrates containing an excess of SiO_2 best match the thermal expansion coefficient of silicon and hence produce the best SOC layers. With such substrates, smooth and uniform silicon layers 25 cm^2 in area have been achieved with single-crystal grains as large as 4 mm in width and several cm in length. Crystal length is limited by the length of the substrate. The thickness of the coating and the size of the crystalline grains are controlled by the temperature of the melt and rate at which the substrate is withdrawn from the melt.

The solar cell potential of this (SOC) sheet silicon is promising. To date, 4.1- cm^2 solar cells have been fabricated, with the benefit of an AR coating but without minimized series resistance, that have conversion efficiencies in the 7.5 percent region. Such cells typically have open-circuit voltages and short-circuit current densities of 0.55 V and 20 mA/cm^2 , respectively. Minimization of series resistance within these cells would improve their efficiency in the direction of the program's ultimate 12 percent goal.

Development efforts are continuing in such areas as improvement in growth rate, optimization of cell performance, and novel device development. A new dip-coating facility has been fabricated with the express purpose of determining how coating speeds can be maintained without sacrificing thickness and grain size. A continuous silicon coating facility has been constructed which is designed to coat large (10-cm x 100-cm) substrates in a continuous manner. It is expected that this facility will not only improve the growth rate, but also minimize the silicon melt's contact with the substrate. This should reduce the rate at which the melt becomes contaminated. This new facility will also permit a study of possible continued grain growth by accommodating the use of longer substrates. It should also reveal problems that are likely to be encountered in a scale-up process.

TECHNICAL DISCUSSION

SUBSTRATES (B. Koepke)

In this section we discuss the development of ceramic substrates for the SOC process. Early in the program it was found that mullite-based aluminosilicate refractories (i. e., fire clay refractories) were quite suitable for the application. Subsequently, all of the work on substrates has been with this class of ceramics. The main goals of the effort this year were to:

- Optimize substrate properties.
- Develop substrates with slots in them to allow back contact to the silicon coating.
- Develop techniques to produce large, 10-cm-wide substrates by a continuous process.

Significant progress was made toward each one of these goals; the results are discussed in the subsections that follow.

Substrate Properties

Early in the program it was realized that fire clay refractories were extremely suitable for use as SOC substrates. They could withstand high temperatures, were resistant to thermal shock, were inexpensive, and had thermal-expansion coefficients close to that of silicon. Thus, fireclay, or mullite refractories as they are also commonly called, have been used exclusively as substrates for the SOC process.

At the beginning of this year, most of our work had been carried out on McDanel MV20 mullite substrates produced at the Honeywell Ceramic Center by rolling, drying, and firing a premixed extrudable composition and on Coors S1SI mullite substrates produced at Coors Porcelain Co. by cold-pressing and firing. At that time, the results on the mullite substrates were promising enough to warrant an effort to optimize the substrate properties with respect to the SOC process. Coors was asked to supply us with a number of experimental substrate compositions based on their standard S1SI material. These substrates were produced, and their compositions and properties were discussed in Annual Report No. 2. At that time, none had been dipped.

Before discussing these and more-recent compositions, the reader is reminded that a fireclay (or mullite) refractory is an aluminosilicate ceramic and can be described in terms of the SiO_2 - Al_2O_3 binary phase diagram shown in Figure 1. At firing temperatures of approximately 1650°C , these materials consist of mullite (i.e., $3\text{Al}_2\text{O}_3 \cdot 2\text{SiO}_2$) crystallites in a high SiO_2 liquid matrix. When the refractory is cooled from the firing temperature, the liquid transforms to a glass, leaving a two-phase material consisting of mullite crystallites in a glass matrix. A typical microstructure of a mullite-based refractory is shown in Figure 2. With the above in mind, the initial experimental compositions from Coors included those listed in Table 1.

Table 1. Initial Batch of Experimental Substrate Compositions

Code	Material	Composition (wt/o Al_2O_3)	$\text{Al}_2\text{O}_3/\text{SiO}_2$ Ratio
A	S1SI	57.6	1.48
B	S1SI plus excess mullite	67.2	2.14
C	S1SI plus 10 wt/o excess SiO_2	52.2	1.17
D	S1SI plus boric acid to dope glass phase	57.6	1.48
E	S1SI fired to produce a porous body	57.6	1.48
F	S1SI produced from high-purity starting materials	57.6	1.48
G	Ground electrically-fused mullite and ground-fused SiO_2 mixed and fired	77.5	3.54
H	S1SI fired in a reducing atmosphere	57.6	1.48
X	McDanel MV20	54.0	1.25

Note that the McDanel MV20 material contains about as much Al_2O_3 as the Coors C Mod material (i.e., S1SI + 10 wt/o SiO_2). The boric acid additions were to produce a low-expansion glass to lower the thermal expansion coefficient to a value closer to that of silicon. This was not found to be the case. This problem has since been resolved with other composition modifications as discussed later. The porous body was produced to improve the thermal shock resistance and to allow more penetration of silicon into the ceramic. The results were marginal. The material fired in a reducing atmosphere contained a high porosity and a carbonaceous residue from unoxidized binder. Both were to enhance silicon penetration into the ceramic. Again the results were marginal.

Figure 1. The Alumina - Silica Phase Diagram According to Askay and Pask

Figure 2. Optical Micrograph (325x) of Coors S1SI Mullite

Modifications B through F and H survived the dip-coating operation but too few were dipped to make a valid comparison of the effects of the compositional modifications. In fact, only one solar cell was fabricated on one of these substrates. The efficiency was only 3.41 percent. The G Mod material was the only substrate to not survive dip coating. This is attributed to the higher total mullite contact in the body. The thermal expansions of these materials are discussed in more detail later.

Semiquantitative analyses of the impurity contents of a number of these materials have been run and are given in Table 2.

Table 2. Semiquantitative Emission Spectrochemical Analysis of Mullite Substrates in Wt. Percent

Sample	Ti	Cu	Mg	Fe	Ca	V	Ni	Cr	Mn
MV20	0.78	<0.01	0.20	0.89	0.11	0.031	---	---	0.041
S1SI	1.1	0.071	0.29	0.68	0.070	0.051	<0.03	0.030	<0.03
Open-porosity modification	1.45	0.038	0.29	0.57	0.062	0.036	<0.03	0.026	<0.03
Reducing-fire modification	1.0	0.27	0.27	0.52	0.062	0.042	<0.03	0.28	<0.03
High-purity modification	0.27	0.047	0.14	0.45	0.080	<0.03	<0.03	N.D.	<0.03

Notable differences include the lower impurity content in the F Mod material and the higher Ti and Cu and lower Fe in S1SI compared with MV20. As noted above, there have not been enough solar cells made on the B through H modifications to evaluate the impurity effects. The mechanical properties and thermal shock resistance of S1SI and of the Coors substrate materials A through H have been extensively characterized during the past year and are discussed in what follows.

The fracture strength and thermal shock resistance of these materials are listed in Table 3. The fracture strengths were measured in four-point bending at room temperature on bars with a nominal cross section of 0.1 x 0.1 inch over a span of 1 inch. The fracture strengths of the Coors C Mod and McDanel MV20 material were about the same. As noted in Table 1, the Al_2O_3/SiO_2 ratios and presumably, the glass contents, were also similar. With the exception of the open-porosity and electrically-fused mullite substrates, the fracture strengths of the rest of the Coors materials were about 20K psi.

Table 3. Room Temperature Fracture Strength and Critical Quench Temperature for Mullite Refractory Substrates

Code	Material	Strength (Kpsi)	Critical Quench Temperature (°C)
7-50	MV20	15.0 ± 2.7	340
7-300	MV20	13.8 ± 2.3	340
A	S1SI	21.7 ± 1.4	*
B	High-mullite	21.0 ± 1.6	300
C	High-glass	13.8 ± 0.8	360
D	Glass-property modification	21.1 ± 1.4	325
E	Open-porosity	16.6 ± 1.8	325
F	High-purity	19.4 ± 0.9	325
G	Electrically-fused	16.2 ± 6.5	315
H	Reducing-fire	22.3 ± 1.5	315

* Not measured to date.

The critical quench temperature refers to a thermal shock resistance measurement attributed to Hasselman [D. P. H. Hasselman, J. Am. Ceram. Soc., **52**, 600 (1969)]. In this technique the room temperature fracture strength (usually in bending) of samples quenched from elevated temperatures is measured as a function of the quench temperature. When the quenching stresses are sufficient to propagate localized surface flaws in the ceramic, the room temperature strength decreases abruptly. The quench temperature causing the decrease in strength is an indication of how much thermal shock the material can withstand. Higher critical quench temperatures imply greater thermal shock resistance. The data listed in Table 3 were obtained on bars with a nominal cross section of 0.08 x 0.08 inch tested in four-point bending over a span 0.75 inch. Tests were run on S1SI samples but the bars were larger in cross section. Since there is a size effect in thermal shock testing, these data need to be repeated on smaller specimens. The critical quenching temperature increases for smaller cross sections. Representative data showing the fracture strength as a function of quench temperature for MV20 mullite are shown in Figure 3. With the exception of the MV20 and C Mod material, the critical quenching temperature is around 325°C. It is slightly less for materials with higher mullite contents (B and G Mod) and for the material fired in a reducing atmosphere. It is slightly higher for materials containing more glass, presumably as a result of their slightly lower thermal expansion. The thermal expansion data will be reported later in this section.

Figure 3. Room Temperature Fracture Strength of MV20 Mullite Plotted as a Function of Quench Temperature. The critical quench temperature is 340°C.

Fracture toughness measurements have been made on MV20 and on the Coors material A through H, excluding the C Mod material. Briefly, the fracture toughness is an indication of the resistance of a material to fast, catastrophic crack propagation and is usually denoted by the critical stress intensity factor, K_{IC} . K_{IC} is a measure of the stress at a crack tip during fast fracture in terms of the crack tip and loading geometry, the crack size, and the remote applied stress according to $K_{IC} = Y \sigma_F a$, where Y is a geometrical constant, σ_F is the fracture stress, and a is the crack length. K_{IC} is a material property and is determined by measuring the load required to fracture pre-cracked specimens with known loading and crack geometries.

In this work the constant-moment modification of the double-cantilever beam technique, devised by Freiman et al. [S. W. Freiman, D. R. Mulville, and P. W. Mast, *J. Mater. Sci.* 8, 1527 (1973)], is being used to measure K_{IC} . An advantage of this technique is that the stress intensity factor is independent of crack length. Thus, the fracture toughness measurement can be made by simply loading a precracked specimen to failure.

Crack length measurements are not necessary. A schematic of the specimen and loading geometry is shown in Figure 4. A side groove is cut into the specimen, as shown in Figure 4, to guide the crack.

Figure 4. Schematic Showing Specimen and Loading Arrangement Used in the Constant-Moment Test. δ is the deflection of the point of load application during the test.

K_{IC} is calculated from

$$K_{IC} = \frac{P_c L}{(It)^{1/2}}$$

where I is the moment of inertia of one-half of the specimen, L is the moment arm, and t is the thickness at the base of the crack-guiding notch shown in the cross-section diagram in Figure 4. Neglecting the effect of the reduced cross section at the crack, $I = wh^3/12$. Note that the general form of both these expressions is $K_{IC} = AP_c$, where A is a geometrical term and P_c is the applied load at fracture. In this test, K_I is independent of the crack length, a , and the measurements are correspondingly simplified, as noted above.

Fracture toughness data taken to date are summarized in Table 4.

Table 4. Fracture Toughness Measurements on Mullite Substrate Materials

Code	Material	K_{IC} (MNm ^{-3/2})
MV20	MV20	1.98 ± 0.23
A	S1SI	2.39 ± 0.34
B	High-mullite	2.22 ± 0.06
D	Glass property modification	2.37 ± 0.29
E	Open-porosity	2.16 ± 0.25
F	High-purity	2.23 ± 0.25
G	Electrically-fused	2.10 ± 0.31
H	Reducing-fire	2.30 ± 0.34

The fracture toughness of the mullite refractories listed in Table 4 are about the same. The lowest of the Coors materials is the electrically-fused mullite fired with fused silica. To put the numbers in Table 4 in perspective, values of the fracture toughness of ceramics range from 0.75 MNm^{-3/2} for soda lime glass to greater than 6 MNm^{-3/2} for hot-pressed silicon nitride. Fine-grained aluminum oxide has a fracture toughness of about 5 MNm^{-3/2}. The fracture toughness of metals is typically an order of magnitude higher.

An estimate of the flaw size initiating fracture in these materials may be obtained from $K_{IC} = \sigma_F Y A^{1/2}$, where σ_F is the fracture strength and Y is a constant depending on the flaw and loading geometry. For penny-shaped surface flaws, $Y = 1.26$ [G.R. Irwin and P.C. Paris, pp. 1-46 in Fracture, Vol. III, H. Liebowitz ed., Academic Press, New York (1971)].

Flaw sizes calculated from K_{IC} and σ_F measurements on S1SI and MV20 materials are 160 and 230 μ m, respectively. These are relatively large flaws and may indicate most failures in these ceramics originate from pores or pore clusters.

Before the thermal expansion data are presented, some recent work on new mullite compositions should be pointed out. One of the goals of the work on the first series of Coors substrates (i.e., B through H Mod) was to see if the thermal expansion of mullite-based refractories could be altered by compositional control. This was the reason that boric acid was added to S1SI to form the D Mod substrates. The resulting borosilicate glass was expected to lower the thermal-expansion coefficient of the material. As noted in the Annual Report No. 2, this was not the case and the expansion of the D Mod substrates was actually slightly higher than that of S1SI. It was also realized at that time that

substrates with thermal expansions closer to that of silicon would probably have to be developed when slotted substrates were used. The stress concentrations in the substrates due to the slots might initiate fractures in the substrates and coatings. This, as we later found out, turned out to be true.

Since fused silica has a lower thermal expansion than silicon and mullite has a higher thermal expansion, in principal the thermal expansion of the two-phase refractory should be a function of the relative amounts of each phase. These are controlled by the $\text{Al}_2\text{O}_3/\text{SiO}_2$ ratio according to the phase diagrams shown in Figure 1. With this in mind, J. Sibold and D. Wirth at Coors started formulating another experimental series of mullite compositions by adding excess silica to the S1SI composition. This had already been done in the first series of compositions (i.e., the B and C Mod materials), but in the "high-silica" modification, only enough silica was added to S1SI to bring the $\text{Al}_2\text{O}_3/\text{SiO}_2$ ratio down to that of MV20. In the next series, even more SiO_2 was added. The compositions of the second series of Coors experimental substrates are given in Table 5.

Table 5. Compositions of The Second Series of Coors Experimental Substrates

Code	Material	Composition wt/o Al_2O_3	$\text{Al}_2\text{O}_3/\text{SiO}_2$ Ratio
A	S1SI	57.6	1.48
C	"High-silica mod" S1SI + 10 wt/o excess SiO_2	52.2	1.17
I	S1SI + 18 wt/o excess SiO_2	48.8	1.01
J	S1SI + 25 wt/o excess SiO_2	45.8	0.89
K	S1SI + 38 wt/o excess SiO_2	41.4	0.74

We will see in what follows that the material with the highest silica content (i.e., K Mod) has properties that make it much more applicable as a substrate for SOC than any others tested to date.

The microstructures of the A, I, and K Mod materials are shown in Figure 5. The darker phase is the continuous glass phase. The amount of glass phase is seen to increase as the $\text{Al}_2\text{O}_3/\text{SiO}_2$ ratio decreases. The pore size also appears to increase with increasing silica additions. Measurements have not been made of the densities at this time. The mechanical properties and thermal shock resistance of these materials have also not been determined. Thermal expansion data have been provided by Coors and are discussed below.

(a) S1SI

(b) S1SI + 18 wt/o Excess SiO_2

(c) S1SI + 38 wt/o Excess SiO_2

Figure 5. Photomicrographs of Various Mullite Bodies
(Magnification 150x)

The thermal expansions of the substrate materials produced by adding excess silica to the S1SI composition are shown in Figure 6. The data are plotted as the linear thermal expansion from room temperature to 700°C as a function of the $\text{Al}_2\text{O}_3/\text{SiO}_2$ ratio. The residual stresses between the silicon layer and the substrate are presumed to be negligible above 700°C. The data corresponding to the S1SI, I and K modifications are indicated as such on the figure. The thermal expansion of silicon is also included in the figure. Note that as the silica content increases, the thermal expansion decreases in the manner expected and that the thermal expansion of a mullite refractory with an $\text{Al}_2\text{O}_3/\text{SiO}_2$ of approximately 0.45 should be equal to that of silicon. A silicon-coated substrate with this composition should not show any residual stresses between the coating and the substrate. The residual stresses in the silicon coating can be estimated by $\sigma = E\Delta T (\alpha_{\text{Si}} - \alpha_{\text{ceramic}})$, where Youngs modulus, E , is assumed to be equal in the substrate and the coating. ΔT is the temperature difference the composite cools below its stress-free state and α_{Si} and α_{ceramic} are the linear thermal expansion coefficients of silicon and the substrate, respectively. If we assume E is 15×10^6 psi, α_{Si} (RT - 700°C) = $3.7 \times 10^{-6} \text{ } ^\circ\text{C}^{-1}$, and a stress-free state at 700°C (i. e., $\Delta T \sim 675^\circ\text{C}$), the residual stresses in the silicon layers on S1SI and the K Mod substrates are:

Material	α (RT - 700°C) ($^\circ\text{C}^{-1}$)	σ (psi)
S1SI	4.7×10^{-6}	10,000
K Mod	4.0×10^{-6}	3,040

Figure 6. Thermal Expansion of S1SI Mullite Containing Excess Silica

Note that with even a small thermal mismatch, significant thermal stresses can develop. These stresses can cause the slow growth of flaws. When subcritical flaws reach critical size under a constant applied stress, large-scale fracture may occur.

Slotted Substrate Development and Large Substrates

The ceramic substrates used in SOC solar cells will presumably have to be produced by a continuous process in order to meet the economic goals of the program. To this end, J. Sibold and D. Wirth at Coors have been adapting their roll compaction process to the manufacture of mullite substrates for the SOC process. This effort has been quite successful. Large, 10-cm by 1-m S1SI substrates have been produced from roll-compacted tape and have been used in the SCIM coater. These substrates are 1.0 mm thick and are some of the largest single substrates produced by a tape process.

Roll-compacted tape has also been used to produce slotted substrates for back-contacted SOC solar cells. In this process, slotted substrates with dimensions shown in Figure 7 have been produced by both cutting the slots in bisque-fired tape with small abrasive wheels and by punching the slot patterns in green, unfired tape with plastic die sets. The properties of silicon coatings put down on slotted substrates are discussed elsewhere in this report.

A last comment should be made pertaining to the mechanical integrity of slotted substrates. It has been noted that slotted substrates have more of a tendency to crack after dipping and during subsequent processing than unslotted substrates. This is expected and results from the tendency for subcritical crack growth to occur in ceramics and from the stress concentrations associated with a slot. Since the thermal expansion of the substrate is greater than silicon, the substrate is in tension at room temperature. The stress concentration at the end of a slot can raise the local stress to values larger than those listed above. The fracture stress of a ceramic depends on the fracture toughness and the flaw size. If flaws in the substrate can slowly grow under a constant residual stress, they may grow to a size where they become critical and initiate fast fracture. This is the origin of delayed failure in glasses and other ceramic materials and has been observed by us in silicon-coated mullite. This problem has been minimized by using the K Mod substrate material but is still occasionally observed. As a result, some new, even lower-expansion, substrate compositions are being developed at Coors.

Figure 7. Dimensions of Slotted Substrates Produced at Coors. Taken from September 15, 1978, Monthly Report from Coors. All dimensions in inches.

DIP COATING (D. Zook, D. Heaps, D. Sauve, R. Maciolek, and K. Wuori)

During the past year, significant progress has been made in improving the control and the quality of dip-coated layers, as well as in the basic understanding of the growth process and definition of the parameters controlling growth. Rather than repeat the details which for the most part have been described in previous quarterly reports, we will list here some of the experiments performed:

- 1) A variety of crucible positions and gas flow rates have been investigated. Both He and Ar gas have been used. The gas flow in the vicinity of the melt has been laminar at low velocities up to this point.
- 2) A variety of mullite substrates have been investigated. Substrate development and the physical properties of the substrates are described elsewhere in this report. It is significant that a wide range of substrate thicknesses have been coated successfully (0.20 inch to 0.200 inch). Generally, we find a tendency for the thinner substrates to have thicker coatings, although below 0.080 inch there is not a large difference. The thinner substrates warp and may crack upon cooling unless the thermal expansion is well matched to that of silicon.
- 3) A variety of carbons have been investigated, including a glassy-carbon coating that was developed in-house. Vitregraf coatings made by Tylan Corporation were also dip coated. All graphite-coated substrates have dip coated very well. Doped-carbon experiments to date have resulted in doping the melt as well as the SOC layer.
- 4) Seeded growth was performed during the past year. The most successful seeding was done by using EFG ribbon material as seeds. This again demonstrates that the SOC growth and structure is very similar to that of EFG ribbon.
- 5) We believe the purity of the graphite used in the crucible holder and lifter has significant impact on the purity of the films.
- 6) Slotted and grooved substrates have been successfully dipped. Originally the intent was to have the silicon fill the slots, but it was then realized that this would lead to additional series resistance when the base contact is made through the slots. Although Dag (colloidal) carbon coatings were used quite successfully on non-slotted substrates, the Dag tends to enter the slots, causing the silicon to work into them. Therefore, hand-rubbed carbon has usually been used with slotted substrates.

Horizontal slots have been found to be more easily bridged by the silicon than the vertical slots. This was first observed with grooved substrates. Horizontal and vertical slots that cover 50 percent of the area can be successfully and routinely dip coated. Figure 8 is a photograph of a vertically-slotted substrate in which the slots are over 1 mm wide

and the ribs are less than 1 mm wide. These layers were grown at a speed of 0.6 cm/sec. The slots were cut with a saw. Figure 9 shows the latest substrate configuration in which the horizontal slots were cut with a punch. We observe that there is less perturbation of the surface with the horizontal slots.

Part of the SiO in our system is due to oxygen leaks from the atmosphere, since the system is not vacuum tight. We believe that the flushing action with clean gas minimizes the detrimental effects of gas leaks in the system.

At this point it is perhaps appropriate to summarize our observations and understanding of the growth process. This understanding has been greatly enhanced by discussions with two consultants: Prof. L. E. Scriven of the University of Minnesota and Prof. J. Verhoeven of Iowa State University.

- 7) Velocity thickness data are summarized in Figure 10. The straight lines denote constant values of the v^2t product. We observe that at a given crucible position, the maximum thickness at a given velocity tends to a constant v^2t relationship. When the crucible is low with respect to the heater, the v^2t product also is lower.
- 8) An annoying problem with the dip-coating operation is the generation of SiO. We have established that the SiO is due to dissolution of the quartz crucible, because a growth run (No. 144) with a POCO graphite crucible did not produce SiO vapors, and the samples and windows remained clear during the run. In a practical sense the SiO formation can be eliminated by introducing the clean gas to the system through a quartz tube in the vicinity of the melt surface and sample. This provides a continuous flushing action of the growing surface.

At the beginning of this year we were not sure where solidification occurs along the SOC layer. Now, however, we believe that solidification occurs at the top of the meniscus. Direct evidence of this is a bright line right at the upper edge of the meniscus. The increased brightness is due to the higher emissivity of the solid. The narrowness of the line is because of the steep temperature gradient in the solid. Our observations can be summarized as follows:

- 1) Solidification takes place at the edge of the meniscus. This is the same as in Czochralski growth and ribbon growth.

Figure 8. Vertically Slotted Substrates

Figure 9. Horizontally Slotted Substrate. The back has been coated with solder for a back contact. The lower part of the front surface has been AR coated.

Figure 10. SOC Layer Thickness, t , as a Function of Growth Speed, v , for a Number of Dip-Coating Runs Under Different Conditions. Triangles and circles are used to indicate series of coating runs in which attempts were made to hold the conditions constant.

- 2) The meniscus height is constant over the range of velocities normally used - 0.04 to 0.1 cm/sec.
- 3) The contact angle between the liquid and solid is 11 deg as in other types of growth from the melt except the ribbon-to-ribbon case. This is inferred. Precise observations are not possible in the present system.
- 4) Starting from good conditions of growth, an increase in the melt temperature, T_m , always causes a decrease in thickness. Films can be grown in a melt temperature range of at least 20 to 30°K.
- 5) At a given velocity, T_m can be decreased to a minimum value, T_{mo} , corresponding to maximum thickness. Under these conditions, a few dendrites form at the top of the layer, but these decay within a few millimeters growth.
- 6) If T_m is further decreased below T_{mo} , dendrites will form and will not decay. The entire range of melt temperatures between dendritic growth to complete disappearance of dendrites is on the order of 3°K. The center of this range we consider to be the optimum growth temperature at that velocity.
- 7) If the velocity is increased, the optimum growth temperature, T_{mo} , is increased. Thus, to obtain maximum thickness at a given velocity, the melt temperature must be increased as the velocity is increased to prevent dendrite formation.
- 8) Width instability has not been observed in SOC growth. This contrasts with the case of EFG growth where careful design and control are needed to maintain the width.
- 9) SiC particle formation on the surface of SOC layers has not been observed. Sometimes protuberances on the surface are observed, but these have been always found to be dendrites, formed under conditions where T_m was just below T_{mo} . Again, this contrasts with the case of EFG ribbon growth, where care must be taken to avoid SiC particle formation.

The above observations, coupled with the results of our thermal analysis (Appendix A), indicate that SOC growth is very similar to EFG growth, but has some important advantages. The thermal analysis, which applies equally to SOC and ribbon growth, shows that the v^2t relationship is very general. However, one restriction is that the heat

current density (or temperature gradient) on the liquid edge of the liquid-solid interface must be negligible compared with $v\rho L$, the velocity times the latent heat per unit volume.

The condition of nearly zero temperature gradient in the liquid is consistent with the observations listed regarding the optimum melt temperature, T_{mo} . Thus, the analyses and the experimental results lend credulity to each other. In fact, the value of the v^2t product can be calculated quite simply, and agrees with the experimental results.

The theory basically states that the v^2t product is determined completely by the coating function. Thus, we can confidently predict that additional radiative and convective cooling will enable us to increase the v^2t product by a significant factor.

Experimental Dip Coater (B. G. Koepke and D. J. Sauve)

An experimental dip-coating facility has been designed and constructed to study the supported growth of SOC substrates. The major goal of the effort is to define the optimum conditions necessary to grow reasonably thick (i.e., 100- μ m) films at high rates (i.e., 0.15 to 0.3 cm/sec). The design of the experimental dip coater closely resembles that of the existing coater, with a few major exceptions. The new coater is larger to allow more access to the vicinity of the liquid-solid interface and to allow afterheaters to be used. Our initial attempts to improve the growth rate while maintaining a film of reasonable thickness will involve the use of cold fingers to increase the temperature gradient at the liquid-solid interface. Early runs indicate material quality as good if not superior to that obtained from the already existing dip coater.

CONTINUOUS COATING (J. D. Heaps, L. Nelson, C. D. Butter, and H. Burke)

During this reporting period, construction of the continuous coating facility was completed. This facility is referred to as the SCIM coater, an acronym based on its principle of operation (Silicon Coating by an Inverted Meniscus). Details of this principle along with a description of the coater were given in Annual report No. 2 (Sept. 30, 1977). The SCIM coater was constructed to investigate what is believed to be a superior method for coating large (10-cm x 100-cm) ceramic substrates with a thin layer of silicon. When fully operational, this coating technique promises to have the following advantages over the present dip coating method:

- Its coating principle reduces the area of, and the time that the substrate is in contact with the silicon melt. This feature lessens the possibility of the melt being progressively contaminated by the substrate.

- The method permits the use of much larger substrates which should allow individual crystalline grains to develop larger in size.
- The coating through-put of this technique is potentially superior because it eliminates the dipping and soaking time required with the dip-coating method.
- The thermal stability of this coating method should also be superior to dip coating because its melt temperature will not be constantly upset by the immersion of unheated substrates.

Figures 11 and 12 are photographs of the coater. Note the large buss bars emerging from the floor in Figure 12. These electrodes supply the facility with output power from three supplies located in a room directly below the facility. The supplies were moved to this remote location because of their excessive audible noise. A fourth power supply is shown in Figure 12.

Constructing a facility capable of coating silicon on large ceramic substrates in a continuous manner proved to be an ambitious undertaking. Most challenging is the fact that the equipment must function where environmental temperatures often exceed 1500°C.

Testing of this coater was initially handicapped by a 4-month late arrival of the facility's major power supplies. This delay was partially offset, however, by operational tests which were conducted using smaller power supplies of lower power than those for which the coater was designed. These tests followed by several full-power tests, performed after receipt of the specified power units revealed that numerous system modifications were needed to ensure satisfactory performance of the coater. This section of the report documents the rationale for these changes and reports the progress made to date in coating SOC after these modifications were completed.

Initial Testing and System Modifications

Originally, the coater was designed with one graphite heating element which supplied power to a melt crucible and quartz trough both containing molten silicon. Early tests revealed that heating these individual containers with a single power source resulted in a nonuniform temperature along the trough. As shown in Figure 13, the upper surface of the graphite trough holder radiates energy to a heating element directly above it, whereas the surface of the silicon melt radiates to colder parts within the coating chamber. This condition unfortunately allowed the molten silicon in the trough to reach a much higher temperature than the silicon melt. Separate heating elements for the melt and the trough were installed to correct this situation, and, by doing so, the temperature of the molten silicon in each of these containers could now be individually controlled (see Figure 14).

Figure 11. Photograph of SCIM Coater During Operational Run

Figure 12. Photograph of SCIM Coater Showing Buss Bars From Remotely Located Power Supplies

Figure 13. Original Heating-Element Arrangement in Coating Chamber of SCIM Coater

Figure 14. Modified Heating-Element Arrangement in Coating Chamber of SCIM Coater. (Substrate upper heater and afterheater not shown in plan view.)

Initially, stainless-steel bolts were used to attach all graphite heating elements to their respective water-cooled electrodes. Due to the poor thermal conductivity of stainless steel, these bolts during operation were constantly melting. This problem eventually required us to substitute larger-diameter graphite bolts. To form a silicon meniscus over which the substrates to be coated must pass, it is necessary to displace molten silicon from the melt into the trough. Early attempts to do this proved troublesome. Because molten silicon has a large surface tension, it does not flow readily along narrow (1-cm-wide) channels as is the case with the quartz trough. To enhance this flow, carbon films were applied to the trough, but this proved to be unsatisfactory because of their inadequate adherence to the trough. One method used for improving the flow was to fill the trough with solid silicon prior to an operational run. By doing so, molten silicon not only flows down the trough, but also assures the operator that the trough is up to temperature before he displaces the silicon in the melt. In later operational runs, a wider (1.5-cm) trough was used, giving the silicon more freedom to flow. Once the trough is filled with molten silicon, a meniscus of substantial height (up to 6 mm) can be observed through a viewing port and this height can be conveniently varied by adjusting the displacer level.

An additional problem related to silicon displacement was also encountered. As experienced with the dip coater, after a prolonged period of operating time, a crust of SiO_2 condenses around the periphery of the silicon melt crucible. In the SCIM coater, this crust also forms a ring around the quartz displacer. If the diameter of the displacer is too large, the crust on the crucible after a period of time combines with the crust on the displacer and the mobility of the displacer is lost; a smaller displacer solved this problem.

Temperature Profiling

Early attempts to silicon-coat large (100-cm x 10-cm x 0.1-cm) mullite substrates furnished by Coors were unsuccessful. This was primarily due to substrate breakage resulting from the large thermal gradients along the substrates path. To gain insight regarding the acceptable thermal gradient that Coors' large substrates would endure, a substrate was passed through a heated (910°C) belt furnace. It was first passed through at a very slow rate and then at the furnace's maximum rate. The substrate endured both passes. At temperatures above 800 to 900°C, mullite is judged to be sufficiently plastic to accommodate larger thermal gradients; therefore, our main interest was to modify the SCIM coater's thermal profile below this temperature.

A thermal profile of the belt furnace is shown in Figure 15. Also shown is the maximum temperature gradient (dT/dx) and thermal shock (dT/dt) the substrate encountered. By

way of comparison, a temperature profile was then made of the path along which the substrate at that time passed through the silicon coating furnace. Data for this profile were taken using three side-by-side thermocouples (TC) traveling longitudinally along the substrate's path. These TC's were arranged to monitor the outer edges as well as the center of this path. By doing so, the transverse gradient along the path could also be plotted. The results of this profile data are plotted in Figure 16. To reduce the large thermal gradient shown here, the coater was modified as described next.

A dual-walled insulated preheated compartment was nonthermally attached to the water-cooled heat baffle which surrounds the coating chamber. A long rectangular graphite tube or tunnel was then attached to this compartment. This tube extends from the entrance of the preheater to the quartz trough in the coating chamber (see Figure 17). This two-piece graphite tube can be easily separated to rearrange guides for various substrate widths. One end of this tube is heated by the upper and lower substrate heaters. Midway in the preheater compartment the upper half of this tube passes by a temperature- and position-adjustable resistance heating element (see Figure 18). The function of this additional heater was to trim the temperature profile. In practice, however, this resistance heater was not needed to achieve the desired profile goal. The long graphite tube served the purpose of providing a longer, more gradual temperature gradient. Because it completely surrounds the substrate, as shown in Figure 18, the edges of the substrate could no longer radiate their energy to the cold walls of the system. To accommodate this modification, the substrate conveyor chain was relocated 4 inches further from the coating compartment. By doing so, this stainless-steel mechanism never experiences a temperature greater than 600°C. A postheater similar in design was also added to the exit port of the coating chamber (see Figure 19).

Following installation of the pre- and postheaters, additional temperature profiles of the system were made. Figure 19 includes the longitudinal plots of all profiles made to date. The dotted curve is a plot of the thermal profile within the coating chamber prior to the addition of pre- and postheaters to the system. The steep thermal gradient shown by this curve was of course, responsible for the substrate breakage. The broken curve is a plot of the thermal profile after the preheater had been added. Note in this profile that the substrate would reach a maximum temperature about 2.5 inches before it passed over the silicon meniscus, and that this maximum temperature is about 120°C above the melting point of silicon. The solid curve is the profile after measures were taken to shift the peak temperature downstream. This shift was accomplished by reducing the temperature of the lower substrate heater.

The upper and lower substrate heaters originally were electrically series-connected and powered by a single source. They are now individually powered by separate supplies. Within limits, the longitudinal position of this peak temperature can now be

Figure 15. Temperature Profile of First Half of Belt Furnace

Figure 16. Original Temperature Profile of SCIM Coater

Figure 17. Preheater Longitudinal Thermal Profiles

Figure 18. Cross-Sectional View Looking Into The Preheater Compartment as Viewed From The Coating Chamber

Figure 19. Postheater Longitudinal Thermal Profile

shifted by varying the temperature of the lower substrate heater. Reducing this temperature also improved the transverse temperature gradient along the substrate path. Prior to electrically separating these heaters, isotherms were plotted for the substrate path as shown in Figure 20. Note the hot spot at the exit of the preheater graphite tunnel. Figures 21 and 22 show that some improvement was made in the transverse temperature uniformity after the heaters were individually powered. Unfortunately, serious non-uniformity still existed in the region of the trough. This nonuniformity has since been improved by altering the resistance of the trough heater in such a way as to add power to the colder end of the trough. To date, updated thermal profiles have not been made. Coating runs following the above equipment changes demonstrate that the thermal gradient along the substrates path has been correctively modified and no longer contributes to substrate breakage.

SCIM Coating Results

Initial attempts to SCIM coat the large Coors' substrates produced spotty, nonuniform layers. These poor coatings were probably a result of the following problems:

- 1) The first and probably most serious problem is the fact that solidification of the silicon coating originally did not occur until 3 or 4 cm downstream from the meniscus. Thus, the coating would often build up in thickness as though silicon were being drawn out of the trough by the motion of the substrate. If, however, the substrate's motion were stopped, this buildup nevertheless continued as though the weight of the coating were siphoning silicon from the trough. On the other hand, when the substrates rate of travel was increased, this buildup appeared to diminish.
- 2) The spotty coatings can be attributed, at least in part, to the problem of temperature nonuniformity along the trough. This causes the substrate to warp in such a way that it makes only spotty contact with the silicon meniscus.
- 3) Another problem is lack of operator experience. In all runs to date, the temperature of the melt and the meniscus have probably been higher than desirable for optimum coating conditions. One reason for the higher temperatures was to prevent the displacer from solidifying in the melt. Efforts in the past to free it have resulted in fracturing its shaft and subsequently ending the run. Another reason was that on occasions portions of the meniscus solidified to the moving substrate.

Figure 20. Preheater Isotherms Prior to Reducing Temperature of the Lower Substrate Heater

Figure 21. Most-Recent Preheater Isotherms

Figure 22. Most-Recent Postheater Isotherms

Then, during the remelt period, the carbon coating on the substrate would become contaminated with SiO and render it unwettable for further coating.

In an effort to overcome the above problems, further system modifications were made. They included the following:

- 1) To attain a temperature gradient in the solidification zone similar to that shown by the dotted line in Figure 23, a modified quartz crucible/trough piece was fabricated which had the trough attached to the crucible in a manner which located it further downstream and closer to the edge of the coating furnace assembly (see Figure 23).
- 2) With the trough moved downstream, the peak temperature had to also be shifted downstream. This was, in part, done by increasing the resistance and hence the temperature of the downstream end of the upper substrate heater. This change is also shown in Figure 23.
- 3) The unheated graphite post tunnel was then moved upstream, bringing it closer to the trough. An additional gas inlet was plumbed into its fore end allowing the gas to pass through a manifold and be exhausted upward to the coated side of the substrate (see Figures 23 and 24). The flow rate of this gas is adjustable and is monitored by a separate flow-meter.
- 4) To correct the problem of spotty coatings, an adjustable graphite guide was constructed which steers the full width of the substrate uniformly over the meniscus. The substrate height over the meniscus can now be trimmed by an adjustment knob which is located near the meniscus viewing port (see Figure 24). The shape, and hence the resistance, of the trough heater was then further altered to supply even more heat to the cold end of the meniscus.
- 4) Only time and repeated coating runs can contribute to SCIM coating experience, but this task is made easier by improved temperature control. Therefore, automatic temperature controllers were added to the system and made operational. This added control reduces the thermal interaction between heating elements when a change of temperature is desired for one element only.

Coating runs following the above changes demonstrate that progress has been made, but that the temperature profile in the solidification zone is still less than desirable.

Figure 23. Coating Compartment Profile Goal

Figure 24. Growth Chamber Cross Section Showing Adjustable Substrate Guide and Substrate Cooling Gas Ports

The SCIM coater has, however, produced thick (150 to 250 micron) dendritic layers at growth velocities of 0.15 to 0.23 cm/sec. The nature of the solidification is not known, but it does differ from the unidirectional growth associated with dip coating. The latest runs indicate that the previously discussed buildup of molten silicon is in part related to the height at which the substrate contacts the meniscus. In all cases where this height was small allowing broad area contact with the meniscus, the molten layer progressively thickened until it eventually made contact with the graphite trough holder below. The only runs to date where there was no evidence of this thickening effect were those where only minimal contact was made with the meniscus.

Further changes are yet needed to provide a steeper temperature gradient in the solidification zone. Consideration has been given to a proposed redesign of the trough holder and its heating element. This redesign would allow the trough to be on the extreme downstream edge of the furnace assembly (see Figure 25). With such a change, however, there is a possibility that in order to maintain molten silicon in the trough, the temperature upstream may be higher than desirable. Another possible redesign being considered would add a second molten silicon reservoir to the trough assembly as shown in Figure 26. This reservoir would be mounted in the trough holder block directly below the meniscus trough. A predetermined quantity of solid silicon would be placed in this reservoir prior to a coating run and, as this silicon melted, it would contact the base of the meniscus trough. It would not, however, have liquid contact with the silicon in the trough. Such a reservoir of silicon would act as a thermal bath, giving both longitudinal and transverse temperature uniformity to this region of the furnace. This, of course, would tend to flatten the peak temperature upstream of the trough. It would also catch any molten silicon which was inadvertently spilled over the sides of the trough. Such spillages have to date been costly in terms of time and ruined furnace parts. Lastly, this bath of molten silicon would visually aid the operator in achieving and maintaining the proper trough temperature.

As reported above, innumerable changes in the facility have been made to solve the many problems related to coating large ceramic substrates with molten silicon. Now that the coater is operational, we anticipate that our future progress toward the ultimate goal of producing large area silicon coatings will be rapid.

ANALYSIS OF GROWTH (D. Zook and S. Schuldt)

During the past 6-months we have made significant progress in modeling the thermal conditions required for steady-state stable growth. In many cases, the analysis and the observations have been closely interrelated with questions raised by one being answered by the other.

Figure 25. Growth Chamber Cross Section Showing Proposed Trough Holder and Heating Element

Figure 26. Growth Chamber Cross Section Showing Proposed Revised Trough Holder with Molten Silicon Bath

The theoretical analyses have had two objectives: (1) to define the parameters which would enable us to increase growth speed, and (2) to define the shape of the liquid-solid interface. One assumption that initially was made for convenience was that the temperature gradient in the liquid was zero. This stimulated observations and a conclusion is that the zero gradient condition can be defined experimentally. Further, the corresponding minimum melt temperature, T_{mo} , for a given velocity can be determined within 1 or 2 degrees Celsius (at least on a relative scale, the thermocouple reading in the crucible lifter can be determined within that accuracy).

The details of our analyses are presented in Appendix A, and will be submitted to the Journal of Crystal Growth for publication. The main conclusions are as follows:

- 1) Under given cooling conditions (i.e., radiative, with given solid angles, emissivities, and environmental temperatures, and/or convective with a given gas), the maximum thickness, t_m , at a given velocity is such that $v^2 t_m = \text{constant}$. The value of the constant depends on the latent heat, L , the heat capacity, C , the density, ρ , the thermal conductivity, K , and the surface cooling functions at the front and back surface of the silicon. Of these parameters, only the cooling can be varied to increase the $v^2 t$ product.

Our results are strictly valid only for the case of ribbon growth, or for growth on an insulating substrate in which case the thickness is exactly half of that of the ribbon case. However, real SOC growth must be between these two limits, and actually closer to the ribbon case when the substrates are thin. This has been verified by two-dimensional numerical modeling of the substrated case. The results of this analysis are not yet complete and ready for inclusion in the present report.

- 2) The shape of the freezing isotherm (the liquid-solid interface) has been calculated in detail. Simple expressions have been derived for the corner angle that the isotherms make with the silicon surfaces and for the radius of curvature of the isotherm. A detailed numerical analysis was performed for a "worst case" example to obtain an exact shape of the isotherm, which showed that the approximate formulas work quite well for the usual cases of practical interest.

The results of the analysis show that the curvature of the isotherm is probably too small to measure accurately, and that therefore the calculations are probably more useful than experiments. The experimental verification will be somewhat indirect and will involve correlating the observed crystalline structure with the calculated interface shape.

THE PERFORMANCE OF SOC CELLS - TASK II AND TASK VI
(B. Grung, T. Heisler, and S. Znameroski)

The best SOC cell fabricated so far has a total-area conversion efficiency of 7.5 percent (AM1, with AR). This cell used the slotted-substrate approach for a back contact to the base region. The AR coating was an approximate 800Å-thick SiO layer. The total area was 4.08 cm² and the top contact metallization covered about 20 percent of the surface area of the cell. A new mask is being designed to reduce the metallization area. The substrate material was mullite with silica added to improve the thermal expansion properties.

The total-area efficiencies of the most recent slotted cells are listed in Table 6. Additional information concerning these cells is given in Table 7. It is important to note that Table 6 uses total-area efficiencies and Table 7 uses active-area efficiencies.

Table 6. Slotted SOC Cell Efficiencies

Cell Number	Total Area (cm ²)	Metal Coverage (%)	Total-Area Efficiency	
			Before AR Coating (%)	After AR Coating (%)
135-11	2.25	16	5.6	x
135-13	2.25	16	4.3	x
136-9	2.25	16	2.7	x
140-8	4.08	20	5.0	6.7
140-9L	4.08	20	5.7	7.2
140-9T	2.25	16	4.7	6.9
140-10T	2.25	16	4.5	5.7
140-10L	4.08	20	4.8	6.7
140-10R	4.08	20	5.9	7.5
140-11T	2.25	16	4.8	x
140-11L	4.08	20	4.9	6.5
140-11R	4.08	20	4.9	6.5
Average	---	---	4.6	6.5

Table 7. Performance of Slotted SOC Cells

Item	Slotted Cell Number	Diffusion Number	Active Area (cm ²)	Emitter $\rho \square$ ($\Omega/\square$)	V _{oc} (V)	J _{sc} (mA/cm ²)	Fill Factor	Active-Area Conversion Efficiency
1	105-4-	P27	5.07	58	0.47	17.8	0.506	4.3
2	108-12-	P28	8.9	57	0.36	13.8	0.291	1.5
3	108-13-	P28	10.38	48	0.45	13.2	0.374	2.2
4	109-10-	P29	12.22	43	0.48	18.8	0.381	3.4
5	109-11-M7HT		8.5	51	0.44	14.1	0.377	2.4
6	109-12-	P29	13.06	31	0.34	15.3	0.262	1.3
7	118-5-MAH		13.64	44	0.48	16.7	0.333	2.6
8	121-9-3	Q21A	1.9	44	0.5	18.5	0.522	4.9
9	121-9-4A	Q21A	1.9	44	0.52	20.7	0.591	6.4
10	121-9-4C	Q21A	1.9	44	0.47	20.2	0.493	4.7
11	122-2-1	000	2.64	44	0.48	21.2	0.87	4.9
12	122-2-2	000	2.84	44	0.48	21.9	0.516	5.5
13	122-3-1	P12	2.64	46	0.5	16.8	0.493	4.1
14	122-3-2	P12	2.84	46	0.5	19.4	0.549	5.4
15	122-5-1	000	2.64	43	0.48	20.1	0.553	5.4
16	122-6-1	P13	2.64	48	0.5	18.3	0.544	5
17	128-3-1	Q21A	2.26	55	0.48	16.5	0.415	3.3
18	128-3-2	Q21A	2.41	55	0.5	17.6	0.443	3.8
19	128-3-3	Q21A	1.9	55	0.48	20.9	0.481	4.8
20	128-4-3	Q21A	1.9	54	0.46	22.1	0.438	4.5
21	128-4-4A	Q21A	1.9	54	0.46	20.4	0.493	4.6
22	128-4-4B	Q21A	1.9	54	0.46	20.4	0.467	4.2
23	130-14-3	Q20B	1.9	66	0.42	17.1	0.391	2.8
24	130-14-4	Q20B	1.9	66	0.42	18.5	0.399	3.1
25	135-11-	Q34	1.9	50	0.52	19.6	0.663	6.7
26	135-13-	Q34	1.9	60	0.49	20.2	0.517	5.2
27	136-9-	Q36	1.9	56	0.42	18.5	0.41	3.2
28	140-8-R	Q39	3.26	42	0.53	18.5	0.585	5.7
	After AR coating		---	---	0.54	30.1	0.521	8.4
20	140-0-L	Q38	3.26	47	0.54	19.3	0.625	6.5
	After AR coating		---	---	0.55	30.9	0.541	9.2
30	140-9-T	Q38	1.9	47	0.49	20.4	0.551	5.6
	After AR coating		---	---	0.51	28.2	0.564	8.2
31	140-10-L	Q39	3.26	46	0.53	20.3	0.554	5.9
	After AR coating		---	---	0.54	29.1	0.537	8.4
32	140-10-R	Q39	3.26	46	0.54	22.2	0.624	7.5
	After AR coating		---	---	0.55	29.5	0.582	9.4
33	140-10-T	Q39	1.9	46	0.48	19.7	0.555	5.3
	After AR coating		---	---	0.49	26.7	0.518	6.8
34	140-11-L	Q38	3.26	42	0.52	20.0	0.592	6.2
	After AR coating		---	---	0.54	28.1	0.539	8.2
35	140-11-R	Q38	3.26	42	0.53	21.0	0.558	6.2
	After AR coating		---	---	0.54	29.4	0.518	8.2
36	140-11-T	Q38	1.9	42	0.49	19.6	0.589	5.7

Table 6 shows that the average efficiency of recent slotted SOC cells is about 4.6 percent without an AR coating and about 6.5 percent with. The I-V characteristics for the best cell - cell number 140-10R - are given in Figure 27. After the AR coating, this cell had a total-area efficiency of 7.5 percent, a total-area current density (J_{sc}) of 23.7 mA/cm^2 , an open-circuit voltage (V_{oc}) of 0.55 V and a fill factor (F.F.) of 0.58. The high values of J_{sc} and V_{oc} indicate that the basic SOS process has considerable potential for producing solar cells with efficiencies greater than 10 percent. Note that the given value of J_{sc} is calculated by dividing the short-circuit current by the total area rather than the active area. The low value (0.58) for the fill factor indicates that the performance of SOC cells can be significantly improved by reducing the effects of series resistance. The important question is: Can this improvement be achieved?

Figure 27. Slotted Substrate SOC Solar Cell

The Potential for Improvement

For conventional solar cells, series resistance effects are associated primarily with fabrication techniques. For example, high series resistance can result from poor ohmic contact to the base region or to the emitter region of a cell. For SOC cells using slotted substrates, series resistance effects are associated not only with fabrication techniques but also with the fact that base contact is made through slots in the ceramic substrate. Computer calculations (Annual Report No. 2) indicate that the series resistance of a slotted SOC cell should be only slightly greater than the series resistance of a structurally similar single-crystal cell if the slot pattern is spaced ≈ 0.5 cm apart.

It is important to note here that we are assuming that the single-crystal cell has a base contact which covers the entire back side of the cell. It is also important to note here that we have fabricated slotted SOC cells with slot dimensions that are typical of those used in the computer calculations. For example, the best cell has slots that are 0.1 cm wide by 1.5 cm long. The center of the slots are spaced 0.25 cm apart. Figure 28 is a calculated contour plot of constant power loss versus slot spacing (from S. Schuldt, Annual Report No. 2). The point is experimental.

Figure 28. Calculated Contours of Constant Power (Efficiency) Loss as a Function of Slot Spacing (Basic Unit Width), b , and Base Sheet Resistance, $R_{\square}$

Experimentally, we have found that the resistance-area product of a recent slotted SOC cell is about $2.8 \Omega\text{-cm}^2$ and the corresponding product of a single-crystal cell is about $1.8 \Omega\text{-cm}^2$ (see the next section). For comparison of different area cells, the resistance-area product is more significant than the series resistance itself. Experimentally, the resistance-area product of a slotted SOC cell is about 50 percent larger than that of a structurally similar single-crystal cell. The important fact to note here is the following: The single-crystal cell has a resistance-area product that is over three times larger than the corresponding product for a typical commercial solar cell, which is usually less than $0.5 \Omega\text{-cm}^2$. This indicates that we have a serious fabrication problem that limits unnecessarily the performance of our single crystal cells - as well as the performance of our slotted SOC cells. The fabrication problem is certainly not unique to the slotted substrate approach.

The most probable cause for the fabrication problem is our unconventional method for making the top surface contact to the emitter region. This method is as follows: Photoresist is applied to the top surface. The emitter pattern is exposed and photoresist is removed from the contact regions. The top surface is sputter cleaned and a thin, $2000\text{\AA}$ layer of Ni is deposited over the entire surface. The photoresist is removed. This lifts off the Ni from the active area of the cell. Solder contacts are then made by dipping the cell into molten In at approximately 170°C . The Ni is not sintered. This method for making the emitter contact can certainly be improved or replaced with a more conventional technique.

In summary, we have a basic fabrication problem that is not unique to the slotted-substrate approach. This problem may be associated with our unconventional emitter-contact method. It is certain that we can substantially improve the performance of our single-crystal cells by identifying and solving this fabrication problem. It is just as certain that we can simultaneously improve the performance of our slotted SOC cells.

Series Resistance Measurements

The I-V characteristics of slotted cell number 135-11 are shown in Figure 29. Three curves are shown. One is for the standard AM1 light condition; the second for a reduced light condition; and the third for the dark condition. The latter curve is inverted. From the three curves, the specific series resistance, or resistance-area (RA) product, can be determined by two methods. The first method involves different illumination levels and yields an RA product of $\sim 2.4 \Omega\text{-cm}^2$. The second method uses the dark curve and yields an RA product of $\sim 3.0 \Omega\text{-cm}^2$. The corresponding I-V characteristics of single-crystal cell number Q21A are shown in Figure 30. The RA product is $2.0 \Omega\text{-cm}^2$ for the first method and $1.5 \Omega\text{-cm}^2$ for the second.

Figure 29. Slotted-Cell Calculation of the Series Resistance

Figure 30. Single-Crystal Cell Calculation of the Series Resistance

Summary of Progress in SOC Cell Fabrication

During the last year, we reported several improvements in our processing techniques for SOC cells. The major improvements are summarized here:

- 1) The diffusion process was modified. First, quartz wool was packed around the ends of the diffusion tube. This produced a more uniform temperature profile inside the tube. Second, the baffle was removed from the source end of the tube. A baffle often improves the uniformity of results; however, it proved to be unnecessary. It should be noted here that it is usually better to set up the diffusion furnace without using a baffle and then to add it later if necessary. Third, the various flow rates were changed as shown in Table 8.

Table 8. Gas Flow Rate (cc/min.)

Gas	Old	New
N ₂	2700	3500
O ₂	124	35
N ₂ + 1% PH ₃	1160	525

After these improvements were incorporated, five 3-inch-diameter single-crystal test wafers were processed. The average sheet resistance of each wafer was within the range from 37 to 39 $\Omega/\square$. This result represents exceptional uniformity for our system. In subsequent processing, the average sheet resistance of an SOC cell was within the range from 43 to 52 $\Omega/\square$. Thus, for the same diffusion conditions, the sheet resistance of an SOC cell is about 10 $\Omega/\square$ greater than that of a single-crystal cell. This is due primarily to the polycrystalline nature of the SOC material.

- 2) An AR coating system was developed. The system is a diffusion-pumped evaporation system with a silicon-oxide evaporation source from Vacuum Atmospheres Company. This is a design with which we had good experience in coating manganese-bismuth films. The thickness is monitored with an Inficon thickness monitor. The nominal thickness we have used is 800Å, which gives the desired deep blue color. The AR coating improves the cell efficiency by approximately 33 percent.

- 3) Mullite substrates with added silica were used. In the first slotted cells a serious cracking problem was observed. This problem has apparently been eliminated by modifying the substrate material so that the thermal expansion coefficient of the substrate matches more closely that of the silicon layer. The high silica substrate material does not seem to have detrimental effects on the performance of SOC cells.
- 4) The doping concentration in the base region was increased. The boron concentration is presently about 3×10^{16} atoms/cm³. This concentration produces a slight increase in the open-circuit voltage.
- 5) The fabrication procedure was improved. The present procedure is to:
 - a) Perform phosphorus diffusion for 20 minutes at 850°C. This diffusion forms the n⁺ emitter region of the completed solar cell. After the phosphorus diffusion, the resulting heavily-doped SiO₂ layer is then removed by hydrofluoric (HF) etch.
 - b) Sputter-deposit platinum on the back surface. The platinum is used to form an ohmic contact to the lightly-doped base region.
 - c) Bake for 2 hours at 100°C. This bake removes any residual liquids (i. e. , water) that remain in the porous ceramic substrate after the previous process steps. Without this bake, the silicon may spall off the substrate during the subsequent high-temperature process, as was demonstrated during our first attempt to fabricate solar cells on slotted substrates.
 - d) Sinter for 30 minutes at 600°C. This forms a platinum-silicide ohmic contact to the base region.
 - e) Sputter-deposit nickel on both the top and bottom surfaces. On the top surface, the nickel is selectively etched to form the contact grid to the n⁺ emitter region. On the bottom surface, the nickel provides a good electrical connection to the thin platinum-silicide layer.
 - f) Indium solder the deposited nickel. This completes the ohmic contacts to the emitter and base regions of the solar cell.

- g) Plasma-etch the outer regions of the solar cell. This defines the total area of the solar cell, which was between 5 to 10 cm² for the preliminary cells on slotted substrates.

Other cell performance data are presented in Tables 9 and 10.

Table 9. Performance of Single-Crystal Cells

Item	Single-Crystal Number	Active Area (cm)	Emitter $\rho \square$ ($\Omega / \square$)	V _{oc} (V)	J _{sc} (mA/cm ²)	Fill Factor	Active-Area Conversion Efficiency
1	P1	1.05	0	0.54	23.6	0.673	8.5
2	P3	1.05	43	0.53	23.8	0.623	7.8
3	P4	4	0	0.53	22.3	0.676	8
4	P6B	7.2	0	0.54	22.3	0.642	7.7
5	P7B	7.56	51	0.55	23.4	0.662	8.5
6	P8B	13.65	0	0.56	21	0.622	7.3
7	P12	2.84	0	0.27	23.6	0.389	2.5
8	P12B	5.52	0	0.54	23.9	0.564	7
9	P13B	2.97	0	0.54	23.9	0.68	8.8
10	P26	1.05	0	0.54	23.6	0.613	7.9
11	P28	1.05	0	0.54	24.9	0.595	8
12	P31+C	1.05	43	0.55	22.4	0.68	8.4
13	P31+D	1.05	43	0.55	21.5	0.612	7.2
14	P31B	1.05	51	0.54	25.5	0.66	8.7
15	P31E	1.05	45	0.55	25.1	0.687	9
16	P32	1.05	0	0.55	24.6	0.657	8.8
17	Q11A	1.05	0	0.54	27.1	0.596	8.8
18	Q11B	1.05	0	0.54	26.9	0.529	7.7
19	Q20B	1.9	0	0.56	25	0.692	9.7
20	Q21A	2.64	0	0.57	27.2	0.702	10.8
21	Q23	2.64	42	0.57	27.2	0.7	10.8
22	Q23A	2.77	0	0.55	26.1	0.638	9.2
23	Q24	1.9	44	0.55	26.1	0.643	9.2
24	Q27	1.05	43	0.52	25.1	0.564	7.4
25	Q27	1.05	58	0.54	27	0.596	8.6
26	Q29A	1.05	43	0.54	25.7	0.663	9.1
27	Q29B	1.05	60	0.54	27.9	0.583	8.8
28	Q30	1.05	44	0.54	25	0.685	9.2
29	Q31	1.05	43	0.54	25	0.685	9.2
30	Q34	3.26	42	0.55	26.1	0.693	10
31	Q36	1.9	42	0.56	25.4	0.741	10.5
32	Q38	5.43	42	0.56	23.9	0.691	9.2
33	Q38	5.43	47	0.46	24.6	0.633	7.1
34	Q39	5.43	41	0.55	24.1	0.686	9.2
35	Q39	5.43	45	0.45	24	0.621	6.7

Table 10. Performance of Non-Slotted SOC Cells

Item	Non-Slotted Cell Number	Diffusion Number	Active Area (cm ²)	Emitter $\rho \square$ ($\Omega/\square$)	V _{oc} (V)	J _{sc} (mA/cm ²)	Fill Factor	Active-Area Conversion Efficiency	Comments
1	104-2-A	P25	1.05	---	0.47	14.8	0.463	3.2	Silicon spalled off
2	104-7-A	P26	3.08	---	0.51	22.7	0.509	5.8	
3	104-7-B	P26	1.05	---	0.51	22.4	0.651	7.4	
4	104-9-A	P25	2.47	---	0.5	21	0.435	4.5	
5	104-18-A1	P30	1.05	66	0.5	17.5	0.626	5.5	
6	104-18-C	P30	1.05	66	0.49	18.4	0.635	5.7	
7	105-2-A0	P26	2.77	---	0.5	19.3	0.541	5.2	
8	105-2-B	P26	1.05	---	0.5	18.7	0.654	6.1	
9	105-7-A	P26	2.77	---	0.47	15.7	0.541	4.1	
10	105-7-B	P26	1.05	---	0.47	14.8	0.463	3.2	
11	106-1-A	P26	1.05	---	0.5	17.6	0.59	5.2	Silicon spalled off
12	106-1-C	P26	2.11	---	0.5	20.4	0.615	6.3	
13	106-2-B	P25	1.05	---	0.5	18.3	0.607	5.5	
14	106-6-A	P30	2.77	72	0.51	20.9	0.607	6.5	
15	106-6-B	P30	1.05	72	0.5	19.5	0.619	6	
16	106-9-A	P25	1.05	---	0.46	17	0.445	3.5	
17	107-4-A	P28	2.77	58	0.51	30.9	0.607	6.5	
18	107-7-A	P28	2.77	68	0.48	15.7	0.506	3.8	
19	107-9-A	P30	2.77	67	0.51	17.8	0.65	5.9	
20	107-9-B	P30	1.05	67	0.47	17	0.624	5	
21	108-15-A	P27	2.77	60	0.47	21.2	0.36	3.6	Glassy carbon Defective cell Vitreous carbon
22	108-15-B	P27	1.05	60	0.4	18.5	0.322	2.4	
23	112-1-A	P31	2.77	58	0.46	22.2	0.283	2.9	
24	112-1-B	P31	1	58	0.46	21.8	0.365	3.6	
25	112-3-A	P31	2.77	59	0.48	19.4	0.486	4.6	
26	112-3-B	P31	1	59	0.49	19.5	0.619	6	
27	112-5-A	P2	2.77	48	0.49	17.4	0.656	6	
28	112-5-B	P2	1.05	48	0.5	17.8	0.664	5.9	
29	112-7-A	P31	1.38	54	0.5	19.9	0.579	6	
30	112-7-B	P31	1.05	54	0.5	17.1	0.588	5	
31	112-10-A	P2	2.77	44	0.51	17	0.659	5.7	Sintering furnace problem
32	112-10-B	P2	1	44	0.51	15.6	0.72	5.7	
33	112-12-A	P31	2.77	61	0.51	18.1	0.566	5.2	
34	112-12-C	P31	1.05	61	0.46	15.8	0.528	3.9	
35	112-14-A	P2	2.77	48	0.51	16.1	0.661	5.5	
36	112-14-B	P3	1.05	48	0.51	16.7	0.705	6	
37	114-1-A	P32	1.05	71	0.48	19.2	0.614	5.7	
38	114-2-A	P32	1.05	69	0	0	0	0	
39	120-3-A	Q11	1.05	47	0.5	19.5	0.619	6	
40	130-10-A	Q23A	1.05	54	0.22	17	0.25	0.9	Metallization problem
41	130-10-B	Q23A	1.05	54	0.49	17.1	0.465	3.9	
42	130-11-A	Q23A	1.05	49	0.48	17.9	0.363	3.1	
43	130-11-B	Q23A	1.05	49	0.46	15.8	0.329	2.4	
44	131-8-A	Q24A	1.9	48	0.33	15.3	0.306	1.5	
45	131-8-B	Q24A	1.9	48	0.51	18.4	0.627	5.9	
46	131-9-	Q20B	1.9	0	0.52	20	0.557	5.7	
47	131-12-A	Q24A	1.9	51	0.41	14.8	0.319	1.9	
48	131-12-B	Q24A	1.9	51	0.4	16.2	0.506	3.3	
49	131-13-A	Q24A	1.9	54	0.48	17.2	0.544	4.5	
50	131-13-B	Q24A	1.9	54	0.49	16.4	0.499	4	Sintering furnace problem
51	131-13-C	Q24A	1.9	54	0.5	16.7	0.578	4.8	
52	132-3-L	Q30	1.05	47	0.49	19.1	0.608	5.7	
53	132-3-R	Q30	1.05	47	0.47	17.9	0.549	4.6	
54	132-6-L	Q30	1.05	54	0.51	18.9	0.629	6.1	
55	132-6-R	Q30	1.05	54	0.51	18.6	0.604	5.7	
56	132-17-A	Q23A	2.77	53	0.5	14.5	0.475	3.4	
57	132-17-B	Q23A	1.05	53	0.48	15.5	0.341	2.6	
58	134-3-B	Q31	1.05	50	0.51	23.4	0.581	6.9	
59	134-3-T	Q31	1.05	50	0.48	23.2	0.434	4.8	9 percent silica
60	134-4-B	Q27	1.05	56	0.51	19.7	0.65	6.5	
61	134-4-T	Q27	1.05	56	0.52	19.6	0.7	7.1	
62	134-7-L	Q31	1.05	46	0.51	18.9	0.561	5.3	
63	134-7-R	Q31	1.05	46	0.52	17.9	0.667	6.2	
64	134-9-A	Q29A	1.05	56	0.52	20.1	0.696	7.3	
65	134-9-B	Q29A	1.05	56	0.52	19.1	0.691	6.8	
66	134-14-B	Q27	1.05	49	0.49	17.2	0.56	4.8	
67	134-14-T	Q27	1.05	49	0.51	17.3	0.667	5.9	
68	135-7-A	Q29A	1.05	50	0.51	17.5	0.681	6.1	15 percent silica
69	135-7-B	Q29A	1.05	50	0.49	17.2	0.48	4.1	
70	135-8-A	Q29A	1.05	60	0.52	19.9	0.698	7.2	
71	135-8-B	Q29A	1.05	60	0.51	15.2	0.681	5.3	

NOVEL DEVICE DEVELOPMENT - TASK VI (B. Grung, T. Heisler, S. Znameroski)

The integral optical coupler (IOC) device was designed by Honeywell and has been fabricated by Plastic Tooling Aids Laboratory of Skokie, Illinois. The IOC resembles the dielectric compound parabolic concentrators developed by Winston, et al.⁵ A scale drawing of the basic configuration is shown in Figure 31. The concentration ratio is approximately 2.

The IOC is designed to operate with an interdigital SOC solar cell - called here the 2x cell. The basic structure of this cell is shown in Figure 32. The first 2x cell was fabricated using a single-crystal silicon wafer rather than an SOC cell. Figure 33 shows the I-V characteristics of the single-crystal 2x cell without the IOC device. The fill-factor and efficiency values are rather low because the starting material had a resistivity of approximately 4 Ω -cm. Both these values can be significantly increased by using lower-resistivity material.

Figure 34 shows the I-V characteristics of the single-crystal 2x cell with the IOC device. Comparison of Figures 33 and 34 shows that the IOC produces the following results: 1) the open-circuit voltage, V_{oc} , increases slightly from 0.55 V to 0.56 V; 2) the fill-factor (F.F.) decreases from 0.63 to 0.54; 3) the total area current density, J_{sc} , increases from 11.8 mA/cm² to 24.0 mA/cm²; and 4) the total-area conversion efficiency increases from 4.1 percent to 7.3 percent. These preliminary results are encouraging. It is important to note that the total-area current density increased by about a factor of two. The IOC was designed to produce this result.

DEVICE MODELLING - TASK II AND TASK VI (S. B. Schuldt)

Slotted Contacts

An extensive analysis of the series resistance problem for slotted contact SOC solar cells was included in Annual Report No. 2. Our main concern in this area has been the unusually high series resistance inherent in our approach, since the bonded structure appears to limit electrical contacting to relatively small areas of the base region. In particular it was found that, if base contacts are made to the silicon through parallel slots in the ceramic, any silicon partially filling the slots would contribute significantly to the RA product of the solar cell. Assuming the silicon completely filled the slots, as was supposed, an RA product of 4.0 Ω -cm² could be expected if the slots were spaced 3.0 mm apart, and if effective silicon sheet resistance were 50 Ω /□. This did not compare favorably with the minimum RA of 1.66 for a tolerable (10 percent) tax on the solar cell efficiency due to parasitic resistance.

Figure 31. Basic Design of Integral Optical Coupler

Figure 32. The 2x Cell

Figure 33. The 2x Cell Single-Crystal Substrate Without IOC

Figure 34. The 2x Cell Single-Crystal Substrate With IOC

It was found since then that it is entirely possible to coat the slotted substrates with minimal filling of the slots, since the silicon tends to bridge the gap if the carbon is kept out of the slots in the substrate precoating treatment. Based on this observation, the RA products were recalculated and the results appeared in Quarterly Report No. 7 (December 30, 1977). For the 3.0-mm spacing case, the RA product would be reduced to a much more acceptable $1.48 \Omega\text{-cm}^2$.

Circular Contacts

A possible alternative to striped electrodes is a two-dimensional square lattice of small circular electrodes as shown in Figure 35. Various methods might be used to produce such a pattern. One method of making small roughly circular holes in the ceramic, while at the same time creating troughs in the back ceramic surface through which contacts to the holes can be made, is illustrated in Figure 36.

Neglecting variation in the thickness of the silicon layer that might result from such a geometry, we have approximated the square fields of Figure 35 as roughly equivalent circular fields in order to estimate the series resistance. If d_o and d_1 are the diameters of contacts and circular fields, respectively, it can be shown that the RA product for an effective sheet resistance, R_s , is:

$$RA = R_s (d_1^2/8) [\ln(d_1/d_o) - 1/4 (1 - d_1^2/d_o^2) (1 - 3d_1^2/d_o^2)] \quad (1)$$

and this equation is plotted in Figure 37. One may note, for example, that $RA = 1.5 \Omega\text{-cm}^2$ if $d_o = 0.3 \text{ mm}$, $d_1 = 3 \text{ mm}$, and $R_s = 50 \Omega/\square$.

An extra contribution to RA due to contact resistance can be shown to be comparatively small. For this term we use the transmission line model ¹ for circular geometries:

$$(RA)_{\text{contact}} = (\pi d_1^2/4) (\sqrt{R_s \rho_c}/d_o) J_0(j\alpha d_o/2) / [-j J_1(j\alpha d_o/2)] \quad (2)$$

where ρ_c is the specific contact resistivity and $\alpha = \sqrt{R_s/\rho_c}$. For $R_s = 50 \Omega/\square$ and $\rho_c = 0.0005 \Omega\text{-cm}^2$, one finds $(RA)_{\text{contact}} \approx 0.2 \Omega\text{-cm}^2$.

The RA product, including contact resistance, is therefore approximately $1.7 \Omega\text{-cm}^2$, comparing favorably with the striped geometry of equivalent (0.3-cm) spacing. For both types of geometry, the RA product will fall rapidly as the spacing is reduced.

Figure 35. Partial Lattice of Electrodes With Square Basic Units (Left). In the derivation of Equation (1), the square units are approximated in circles (right).

Figure 36. Holes at the Intersection of Perpendicular Sets of Troughs in the Front and Back Ceramic Surfaces

Figure 37. RA/R_s from Equation (1) for the Circular Base Field Geometry

Economic Analysis

A cost analysis was presented in Quarterly Report No. 7 (December 30, 1977) to cover three hypothetical production scenarios: 1) a 1977 "baseline" set of parameters, 2) a "conservative" projection corresponding roughly to the year 1982, and 3) an "optimistic" projection corresponding to 1986. The analysis applies to a factory which produces inspection-approved silicon film on ceramic panels. Subsequent steps in the manufacture of solar cell arrays are excluded from the operation - namely diffusion, electroding, assembly, and packaging. In this particular factory, the important input parameters are the raw materials, utilities, labor rates, and unit productivity (pulling speed). Based on a fixed assumed output of 5 million m^2 of silicon-coated ceramic per year, the economic model predicts delivered price per m^2 of coated panel, including the silicon, and added value, excluding silicon. Included in the model is an estimate of

the labor force and capital investment necessary to achieve the production goal. Since this goal is fixed, it follows that the factory size must scale in some inverse fashion with the unit productivity. These scaling relationships are presented in some detail in the earlier reports. The conclusions extracted from the three scenarios are summarized in Table 11.

Table 11. Cost Predictions Based on Various Production Scenarios

Input/Output Summary	Scenario		
	Baseline	Conservative	Optimistic
Input:			
Production units at	\$100,000	\$100,000	\$100,000
Silicon (\$ /kg)	55.00	25.00	10.00
Ceramic (\$ /m ²)	5.00	5.00	2.00
Argon (\$ /100 ft ³)	3.75	3.00	3.00
Pull speed (mm/sec)	0.5	1.0	10.0
Si thickness (microns)	200	150	100
Substrate thickness (cm)	0.25	0.25	0.25
Electric rate (\$ /kWh)	0.04	0.04	0.04
Output:			
Added value (\$ /m ²)	37.15	20.90	7.19
Price (\$ /m ²)	75.06	33.82	10.64

A conclusion from the cost breakdown (not indicated in Table 11) is that direct material and labor costs contribute roughly equally to the added value of the product, whereas both capital and utility costs are relatively unimportant on a per-unit-area basis. If the target added value is not to exceed \$18/m², the optimistic projection is well within range, and the conservative projection is slightly too high. In the latter case, it was shown in Quarterly Report No. 7 that a doubling of the pull rate from 1 to 2 mm/sec would reduce the added value to about \$15/m².

CONDUCTIVE INTERFACE (T. Schuller and D. Zook)

We have previously reported observations and measurements of the silicon-carbon interface. The primary goal of this task is to improve the conductance (increase the thickness) of the carbon layer used to wet the ceramic and to obtain ohmic contact between the carbon and the p-type silicon so that the carbon contributes significantly to decreasing the series resistance of the solar cells. Two additional goals are: 1) to investigate the use of doped carbons as diffusion sources for doping of the back surface of silicon to provide a BSF effect, and 2) to investigate the use of the glassy carbon as a protective barrier against unwanted impurity diffusions from the substrate into the silicon layer.

An important part of this effort is to have control of the carbon layer. For this reason, we have begun development of a method of producing doped glassy-carbon (GC) layers. We had previously demonstrated that "Vitregraph" glassy-carbon coatings made by Tylan Corporation showed very little erosion by the molten silicon. This is important if the vitreous carbon is to be used as a protective barrier.

In Table 12, silicon-to-carbon contacting is indicated in the dipped GC-coated substrates by a lower ρ_s measurement of 8 to 40 $\Omega/\square$. In contrast, the hand-rubbed Ultra-Carbon control sample is 200 $\Omega/\square$. On some of the dipped samples the silicon was etched off with CP4 etch and considerable erosion of the vitreous carbon layer was observed. High-temperature firing of the carbon layers may reduce this degree of erosion. There is evidence of the boron-doped carbon doping the melt. This is indicated by contrasting the ρ_s of the silicon layer on the doped-carbon samples and the ρ_s of the silicon on a hand-rubbed Ultra-Carbon sample dipped after the doped-carbon samples.

Table 12. Sheet Resistivity of Silicon Coatings
(First Dip Run)

Substrate	Silicon Layer ρ_s ($\Omega/\square$)
Hand-rubbed Ultra-Carbon control before	200
900° fired GC (4 samples)	8 to 40
900° fired boron-doped GC (dipped) near end of run	4.2, 4.4
Hand-rubbed Ultra-Carbon dipped after boron-doped samples	17

In the second dip run, eight GC-coated substrates with thinner carbon coatings (average $\rho_s = 52 \Omega/\square$) were dipped. The silicon coated all of the substrates very well. Sheet resistivity measurements for the sequence are summarized in Table 13. All samples were dipped with the same pull-rate, resulting in similar silicon coating thicknesses.

Table 13. Sheet Resistivity of Silicon Coatings
(Second Dip Run)

Substrate	Silicon Layer $\rho_s (\Omega/\square)$
Hand-rubbed Ultra-Carbon control before	120
Unheat-treated GC (3 samples)	avg. = 130
Boron-doped GC (5 samples)	avg. = 3.4
Hand-rubbed Ultra-Carbon control after GC samples	2.1

Comparison of the first two lines of Table 13 shows no evidence of electrical contact between the silicon and carbon. This is possibly due to the high erosion of the thinner carbon layer by silicon. The bottom two lines indicate boron doping of the melt by the GC for the same reasons as previously mentioned.

Diodes were made from this dip run and results are listed in Table 14.

The cell measurements show that the GC coatings can produce performance at least as good as that produced with hand-rubbed carbon.

Table 14. Summary of SOC with Glassy Carbon

Diode	No. of Diodes	Avg. Active Area (cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	Fill Factor	Avg. Eff. (%)	Max. Eff. (%)	Comments
120-1A-Q11	5	0.048	0.47	22.2	0.668	7.2	8.2	Hand-rubbed carbon control
120-3B-Q11A	6	0.070	0.50	21.6	0.679	7.25	8.4	GC
120-3B-Q11B	6	0.085	0.50	22.0	0.672	7.4	7.7	GC
120-3A-Q11	1	1.05	0.50	19.5	0.619	6.0	6.0	GC

It is expected that the erosion resistance and the impermeability of the GC layers will be increased by high-temperature firing. For this purpose, an induction furnace for high-temperature heat treatment of vitreous carbon coatings has been set up. Some problems arose with the first few samples which were fired. The first coating fired successfully but succeeding coatings tended to flake off. This problem was later rectified by thinning the polymer and laying down a much thinner coat for the second and succeeding coatings.

In summary, GC layers have been demonstrated to act effectively as wetting agents and as diffusion sources for doping silicon layers. Firing at 900°C does not appear to give adequate erosion resistance and impermeability, although such films are adequate to produce good cell performance. High-temperature firing is needed to reduce the erosion effect of the molten silicon.

At this point the work with glassy-carbon coatings has been temporarily stopped in order to work on the formation of a Back Surface Field with aluminum or boron.

BSF Metallization (Task VI)

Different materials are being evaluated as back-contact materials that will produce the BSF effect when used with the slotted SOC material.

The first of these new materials is an aluminum paste formulation. The use of such for BSF contacts was described in a paper by J. S. Thornhill of Spectrolab.¹ We prepared two paste mixtures which are very similar to the in-house mixture described by Thornhill, one with an average particle size of 9 microns and the other with an average particle size of 6 microns. The second material is also aluminum, but is sputtered on the back surface rather than applied as a paste. Contact resistivity measurements and diodes were made on both paste and sputtered aluminum. The contact resistivity of the fired paste was 0.16 Ω -cm, while the sputtered aluminum was 0.010 Ω -cm. The value for the paste was higher than expected. This may be due to process conditions.

Diodes were made on both single-crystal and SOC silicon. The results for single-crystal silicon are listed in Table 15 and for the SOC diodes in Table 16. All samples were sintered in an oxygen/argon atmosphere and all the aluminum paste samples were air-baked at 210 to 250°C for 15 minutes prior to sintering. This paste was made with Reynolds Aluminum 1-131 with an average particle size of 6 microns.

Table 15. Single-Crystal Diodes With Aluminum Back Contacts

Wafer No.	Type of Aluminum	Furnace Temp. (°C)	Furnace Time	Max. V_{oc} (V)	Comments
6	Paste	903	60 sec	0.56	Shown shunt and series resistance.
10	Paste	916	40 sec	0.55	Shown shunt and series resistance.
11	Paste	~900	25 sec	0.56	Shown shunt and series resistance.
12	Sputtered	876	30 sec	0.54	Shown shunt and series resistance.
13	Sputtered	825	15 min	0.54	Shown series resistance, but the shunt resistance was much better than observed on the other samples.

Table 16. Slotted SOC Diodes With Sintered Aluminum Paste Back Contacts

Diode No.	Furnace Temp. (°C)	Furnace Time	V_{oc} (V)	Fill Factor	Comments
139-13A-2	823	5 min	0.515	0.740	Diode located at the edge of the mullite.
139-13A-4	823	5 min	0.507	0.711	
139-13A-1	823	5 min	0.321	---	
139-13A-3	823	5 min	0.445	---	Crack in the silicon extending toward the diode.

The improved shunt and series resistance on the SOC diodes in contrast to the shunting effect and high series resistance of the single-crystal diodes may be the result of lower temperature firing. Temperatures in the range of 800 to 825°C were used.

The work on the formation of a BSF back contact to slotted SOC material will continue using the aluminum paste and sputtered aluminum. Another method which will also be evaluated is the use of a borosilica film as a boron diffusant source for BSF formation.

EFFECT OF MELT TEMPERATURE ON SOC GROWTH (J. D. Zook)

Existing theory is consistent with our observations that the meniscus height in SOC growth is independent of velocity. The theory of the meniscus height and shape, as discussed by Surek,² and by other authors,³ also is consistent with observations of EFG ribbon and dendritic web growth. The meniscus shape for the SOC case should be the same as that for the dendritic web case, and is plotted in Figure 6 of Harrill, et al.,⁴ which is included below as Figure 38.

Figure 38. Meniscus Shape and Convection in SOC Growth

The arrows in Figure 38 have been added to show the effect of convection in the liquid silicon. Because of the convection within the wide part of the meniscus, the temperature gradients in the liquid next to the ceramic should be small except within a region, δ , of the liquid-solid interface. Thus, the temperature profile within the silicon near the ceramic boundary should be as shown in Figure 39.

Figure 39. Temperature Profile in Silicon Near the Ceramic Boundary

The boundary condition at the liquid-solid interface is

$$J_F = J_O + \rho v L \quad (3)$$

where J is the heat current density

$$J = -K \frac{dT}{dy}, \quad (4)$$

J_O is the current in the liquid at the liquid-solid interface, and J_F is the current in the solid.

The curvature of the thermal profile is due to the surface heat loss in the δ region:

$$-\frac{dJ}{dy} = \frac{f_L}{t} \quad (5)$$

where f_L is the surface heat transfer function (W/cm^2) for the liquid. For example, $f_L = \epsilon_L \delta (T^4 - T_O^4)$ for radiative transfer. Integrating once,

$$-K \frac{dT}{dy} = J = \frac{-f_L}{t} y + J_O \quad (6)$$

since f_L is essentially independent of y . Integrating again from $T = T_M$ to T_F and from $Y = -\delta$ to 0,

$$T_M - T_F = \frac{1}{2} \frac{f_L}{K_L t} \delta^2 + \frac{J_o}{K} \delta \quad (7)$$

The condition for maximum thickness is that $J_o = 0$, giving the relationship:

$$T_{M_o} - T_F = \frac{1}{2} \frac{f_L}{K_L t_m} \delta^2 = \frac{1}{2} \frac{f_L \delta^2}{K_L (v^2 t_m)} v^2 \quad (8)$$

From our analyses of heat flow in the solid and from experiment we know that $v^2 t_m$ is a constant. Thus, Equation (8) is a relationship that would enable us to deduce a value for δ from the observed increase in temperature needed to produce maximum thickness when the velocity is increased.

Qualitatively the effect of a change in melt temperature at a fixed velocity is shown in Figure 40.

Figure 40. Change in Melt Temperature at Fixed Velocity

Curves 1, 2, and 3 illustrate three decreasing values of T_M . Curve 1 results in a positive value of J_o . Because of Equation (3), the value of J_F is increased by the amount J_o . The thermal analysis in the Appendix shows that

$$J_F = \frac{c}{t^{1/2}} \quad (9)$$

where c is a constant which depends on the surface heat transfer function for the solid:

$$c^2 = 2 \int_{T_o}^{T_m} KfdT. \quad (10)$$

Since J_F is higher than the minimum value, $\rho v L$, the thickness, t , will be less than the maximum thickness, t_m .

Lowering the melt temperature, T_M , to reduce J_o to zero, gives curve 2 in Figure 40 and yields the maximum thickness, t_m , which is given by

$$t_m = \frac{c^2}{\rho^2 v^2 L^2} \quad (11)$$

A further reduction in t_m produces curve 3 which indicates supercooling in the melt ahead of the freezing interface and a negative value of J_o . This is an unstable condition, because freezing at this point would result in a lowering of the meniscus height from the stable value, h_o , determined by surface tension. The result is growth of dendrites and nonuniform thickness, nonuniform heat flow in the solid, and a nonuniform meniscus height.

Consider growth under conditions of curve 2. When the growth of a layer first begins, the silicon is not present to conduct the heat of fusion away. Thus, the gradient in the freezing solid is small (like curve 3), and that in the liquid may be negative (curve 3). As the length of solid builds up, it can conduct away the heat, and the temperature profile shifts to that of curve 2. Thus, experimentally the conditions of growth under optimum conditions can be established by requiring that dendrites form at the top of the layer and decay within a few mm. Our observations show that only a degree or two increase in T_M from this condition will eliminate the dendrites, and a decrease in T_M by a degree or so will produce dendritic growth.

The value of J_o is obtained from Equations (3), (9), and (11):

$$J_o = \rho v L \left(\sqrt{\frac{t_m}{t}} - 1 \right) \quad (12)$$

Thus, Equations (7) and (12) give a relationship:

$$T_M - T_F = \frac{1}{2} \frac{f_L \delta^2}{K_L t} + \frac{\rho L \delta}{K_L} \left(\sqrt{\frac{(v^2 t)_m}{t}} - v \right) \quad (13)$$

All parameters are known except δ , which can be determined from the change in minimum melt temperature, T_{Mo} , with change in velocity as given by Equation (8):

$$\delta^2 = \frac{2K_L (v^2 t_m)}{f_L} \frac{\Delta T_{Mo}}{\Delta (v^2)} \quad (14)$$

A rough examination of some of our data shows that $\delta = 1$ mm should be in the ball park. For the purposes of plotting it is convenient to choose $T_M - T_F$ as a parameter and plot the velocity/thickness relationship using Equation (13). This is done in Figure 41 for reasonable choices of parameters. The value of $T_M - T_F$ can be expressed in terms of the thickness, t_m :

$$T_M - T_F = \frac{1}{2} \frac{f_L \delta^2}{K_L t} \quad (15)$$

and then Equation (13) can be rewritten for convenience in plotting:

$$v = \sqrt{\frac{(v^2 t)_m}{t}} - \frac{1}{2} \frac{f_L \delta}{L} \left(\frac{1}{t} - \frac{1}{t_m} \right) \quad (16)$$

Equation (16) shows that one parameter, f_L/L , determines the shape of the curves and (15) shows that $f_L \delta^2/K_L$ determines the value of $T_M - T_F$ for each curve.

In summary:

- 1) The melt temperature for maximum velocity at a given thickness is given by zero temperature gradient in the liquid ($J_o = 0$). It may be observed and reproduced experimentally by requiring that dendrites form at the top of a layer and decay within a few mm after forming.
- 2) Under conditions of optimum growth, the product $v^2 t_m$ is constant, as discussed previously.

Figure 41. Velocity/Thickness Relationship
Using Equation (13)

- 3) As the velocity is increased, the temperature of the melt must be increased to maintain optimum growth, according to Equation (8) which has an adjustable parameter, δ .
- 4) The same parameter, δ , may be used to predict the decrease in thickness as T_M is increased for a fixed velocity above the value for optimum growth.

In conclusion, observations should be made to determine if the meniscus height is indeed independent of v , and measurements of the change in thickness produced for a given increase in melt temperature should be interpreted in terms of the present theory.

It would help our understanding considerably if a simple theory with one parameter could be used in lieu of a detailed understanding of the convective and heat transfer effects taking place in the molten silicon. Plans are underway to perform a series of runs to test the validity of the simple model presented here.

PROCESSING EFFORTS

The following processing efforts were performed during this reporting period:

- A procedure was developed for making fracture toughness and thermal shock measurements in mullite substrates.
- A process was developed for making mullite substrates of various excess silica concentrations to closely match the thermal expansion coefficient of silicon. (Coors Inc.)
- A process was developed for making mullite substrates using a roll-compacted tape process. (Coors Inc.)
- The gas used for the silicon coating environment was changed to argon.
- A new experimental dip coater was constructed.
- A process for seeding the grain growth of the silicon coating was developed.
- A process for in-house glassy-carbon coatings was developed.
- A process was developed to practically eliminate the SiO formation during dip coating by introducing a clean gas at the surface of the melt.
- A process was developed which provides more-uniform N^+ diffusion sheet resistance on the SOC material.
- An antireflection coating process was developed which increases solar cell performance by an average of 33 percent.
- A process was developed which improved the overall performance of unslotted SOC photocells.
- A process was developed for making various slot, hole, and groove patterns in mullite substrates.
- A process was developed to provide glassy-carbon layers doped with boron on SOC substrates.

PROJECTION OF FUTURE ACTIVITIES

The work necessary to successfully determine the technical and economic feasibility of our SOC technology can be divided into three major areas:

- Cell performance optimization
- Coating speed optimization
- Continuous-coating technology development

Specifically, we will continue to determine the mullite modifications necessary to obtain ceramic slotted substrates which will withstand cracking (with Coors Inc.), Coating properties as a function of substrate thickness will be investigated.

Work will also continue in the area of understanding the role of boron doping from glassy-carbon coatings in order to provide improved cell performance.

The continuation of processing refinement will occur. We will concentrate on obtaining complete cell processing techniques which will eliminate the high series resistance in the top contact.

We will continue to establish a capability to evaluate various novel device structures. We will initially concentrate on the stripe cell geometry with an integral optical coupler.

Slotted-substrate cell processing will continue. Back-Surface Field activity will be incorporated in this cell processing activity to determine its potential for increased cell performance.

Work will continue in an effort to increase the linear coating speed of our dip coater without sacrificing material quality. This will be done by adding cooling shoes to our experimental dip coater.

We will continue our continuous-coating technology development by performing coating experiments in our Silicon Coating by Inverted Meniscus (SCIM) coater. Work here will concentrate on temperature gradient control near the solidification zone.

Device modeling activities will continue primarily in the area of analyzing novel device structures. Further modeling activities will concentrate on understanding the various growth parameters and their effect on grain size and coating thickness.

NEW TECHNOLOGY

Recent results indicate that slotted-substrate SOC solar cells can approach the conversion efficiency necessary to provide a cost-effective device. We have demonstrated the ability to coat slotted mullite substrates which have a 50 percent slot/ceramic ratio. This ratio is well within the limits set by an analytical model of this device configuration necessary to minimize series resistance.

We have also demonstrated the feasibility of using a striped cell geometry in conjunction with an integral optical coupler. This device is particularly useful in that it may provide the necessary performance without the need of making electrical contact through the back of the substrate material.

SUMMARY OF ANALYSIS AND CHARACTERIZATION DATA

The analysis and characterization data are presented in detail in the appropriate sections of the report. These analyses are summarized in the following brief statements:

- Mullite-based refractories can be produced with varying excess silica concentrations without impairing their coatability.
- Fracture toughness and thermal shock resistance measurements were carried out on various mullite compositions as a means of providing quality control information.
- Microstructure evaluation of excess silica mullite compositions indicates an increase in the glass phase and pore size.
- Elevation of the crucible with respect to the heater in the dip coater allows thicker coatings to be obtained at the same growth speed.
- In general, there is a tendency for thinner ceramic substrates to have thicker silicon coatings. This effect seems to disappear if the substrates are 0.080 inch thick or less.
- Thinner substrates warp/crack upon cooling unless the thermal expansion is well matched to that of silicon.
- All graphite-coated substrates, including glassy carbon, have dip coated very well.
- Doped-carbon experiments have resulted in doping of the melt as well as the SOC layer.
- The purity of the graphite in the crucible holder directly impacts the purity of the SOC layer.
- Slotted and grooved substrates have been successfully dipped. We can control whether the slots are filled with silicon or not. Horizontal slots seem more coatable than vertical slots.
- The thickness of the SOC layer is proportional to the inverse of the pulling speed squared.

- Solidification of the dip-coated layer takes place at the edge of the meniscus similar to Cz and ribbon growth. The meniscus height is constant over a velocity range of 0.04 to 0.1 cm/sec.
- An increase in the melt temperature always causes a decrease in silicon film thickness.
- For a given desired layer thickness, the melt temperature must be increased as the pulling speed increases, to prevent dendrite formation.
- Width instability and SiC particle formation have not been observed in SOC material.
- Electrical contact studies reveal the limitation of slotted-cell performance is due to the high series resistance in the top contact, not due to the slotted cell design.

PROGRAM STATUS UPDATE

Updated versions of the Program Plan, Program Labor Summary, and Program Cost Summary are presented in Figures 42, 43, and 44, respectively.

NOTE: IN ADDITION TO THE ABOVE PROGRAM PLAN, THE HONEYWELL CORPORATE TECHNOLOGY CENTER WILL PROVIDE THE REQUIRED DOCUMENTATION, ATTEND THE REQUIRED MEETINGS AND DELIVER THE REQUIRED SAMPLES AS PER CONTRACT AGREEMENT.

△ PLANNED
▲ ACCOMPLISHED GOALS

Figure 42. Updated Program Plan

Figure 43. Updated Program Labor Summary

Figure 44. Updated Program Cost Summary

REFERENCES

1. "Automated fabrication of BSF silicon solar cells with screen-printed wraparound contacts," J. A. Thornhill, Spectro Lab, NASA Contract NA53-20029, Final Report, pp. 11-15 (August 1977).
2. "The EFG process applied to the growth of silicon ribbons," J. G. Swartz, T. Surek, and B. Chalmers, J. Electronic Materials, 4, 255-279 (1975).
3. "The growth of crystals from liquids," J. C. Brice, North Holland Press (1973).
4. "Thermal analysis of solidification in web-dendritic ribbon growth," M. D. Harrill, G. A. Rhodes, J. W. Faust, and R. B. Hilborn, J. Crystal Growth, 44, 34-44 (1978).
5. "Solid dielectric compound parabolic concentrator; on their use with photovoltaic devices," N. B. Goodman, R. Ignatius, L. Wharton, and R. Winston, Appl. Optics, 15, p. 2434 (1976).

APPENDIX A
ANALYSIS OF CONDITIONS FOR HIGH-SPEED
GROWTH OF SILICON SHEET*
(S. G. Schuldt and J. D. Zook)

INTRODUCTION

The vertical growth of sheet silicon from the melt is common to several approaches¹⁻⁸ to low-cost silicon solar cells. The rate of growth and the thickness of the silicon are of key importance in cost analyses. Also, it is well known that excessive curvature of the steady-state freezing front can aggravate the problem of undesirable grain boundaries in the sheet silicon, leading to lower cell efficiency. It is therefore important from the standpoint of cost and efficiency to have a thorough understanding of the parameters which control the growth rate, thickness, and the shape of the liquid-solid interface.

This analysis consists of two parts. In the first part the heat transport in the solid and at the radiating boundaries is linearized and the gradients in the liquid are neglected. The "convective" term in the heat transport and the nonlinear boundary condition are taken into account and the problem is solved by numerical analysis. The speed-thickness tradeoff and the shape of the liquid-solid interface are calculated, assuming, of course, that freezing and the liberation of the latent heat take place along an isotherm.

In the second part, analytic expressions for the speed-thickness tradeoff and the slope and curvature of the liquid-solid interface are derived. The temperature dependence of the thermal conductivity and nonlinear surface heat transfer are taken into account exactly. Based on the results of the first part, it is argued that the approximations involved in the analytic expressions are quite good. The two parts are complementary in the sense that each deals more exactly with an aspect of the problem that is treated approximately in the other part. The agreement of the two approaches in a specific "worst case" example gives credibility to the validity of both.

The model used in this analysis is directly applicable to symmetrically grown unsupported ribbon (Figure A-1a). Supported growth on a substrate, (Figure A-1b) such as ceramic⁸ (SOC or Silicon-on-Ceramic) or on graphite⁹⁻¹¹ (RAD or Ribbon-Against-Drop), is more complex. In the limit that the substrate is a thermal insulator, this analysis is again

*Based on paper to be submitted for publication to the Journal of Crystal Growth.

(a)

(b)

Figure A-1. Vertical growth of sheet silicon. (a) Unsupported growth. (b) Supported growth. In the present discussion, the effect of a die to stabilize the unsupported growth is neglected.

applicable. In this case, the isotherms in the silicon must be perpendicular to the substrate. Due to symmetry, this is also true at the middle plane ($x = 0$) of the unsupported ribbon. Thus, the insulating substrate case is equivalent to the left half ($-t \leq x \leq 0$) or the right half ($0 \leq x \leq t$) of the unsupported ribbon case.

This analysis does not treat the heat transfer in the liquid, which can be quite complex, and may vary considerably among the different sheet growth methods. A general feature of all growth from the melt, however, is that the liquid-solid interface will not be stable if the heat flow in the liquid is away from the interface. A condition for the maximum stable growth rate is that the temperature gradient on the liquid side of the interface approach is zero. As discussed by Brice,¹² this condition can be approached by increasing the velocity and/or by decreasing the melt temperature almost to the point where the interface becomes unstable and dendritic growth develops.

In any case, the choice of zero gradient in the liquid is very convenient mathematical modeling, since the heat transfer in the liquid is then irrelevant. A limitation of such a model is that it cannot predict how changes in the melt temperature will affect the growth rate or sheet thickness. However, the purpose of this analysis is to discuss the growth at maximum velocity (for a given thickness) and thus the assumption of zero gradient in the liquid is quite appropriate. The analytic expressions in the second part of the analysis include the gradient in the formal expression. However, the purpose of including it is only to indicate its effect, since the relationship between J_0 and the melt temperature is not specified.

LINEARIZED TWO-DIMENSIONAL PROBLEM

Heat transport in the moving solid is governed by the equation¹³

$$\bar{\nabla} \cdot (K \bar{\nabla} T) - \rho C (\bar{\nabla} T) \cdot \bar{\nabla} = \rho C \frac{\partial T}{\partial \tau} \quad (A-1)$$

where K is the thermal conductivity, ρ is the density, C is the specific heat, T is the temperature, τ is the time, $\bar{\nabla}$ is the ribbon velocity, and the position coordinates are stationary with respect to the crucible.

Of interest here are ribbons with a high width-to-thickness ratio so that a two-dimensional analysis (x, y) is appropriate. The velocity is just the pull speed, v , in the positive y direction, and the process is assumed to be in the steady state, $\frac{\partial T}{\partial \tau} = 0$. The range of temperatures in the solid ribbon must be restricted to a relatively narrow band between

the silicon freezing temperature, T_F , and the radiation temperature, $T_O < T_F$, of the environment seen by the ribbon as it proceeds upward. Assuming constant K , we have

$$K \left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} \right) - \rho C v \frac{\partial T}{\partial y} = 0 \quad (A-2)$$

Auxiliary conditions are to be satisfied at the ribbon faces, $x = \pm t$, and at the unknown freezing front, $y = y_F(x)$, where $T[x, y_F(x)] = T_F$. Heat carried to ribbon faces is assumed to be radiated to the environment, according to

$$|K \partial T(\pm t, y) / \partial x| = \epsilon \sigma \{ [T(\pm t, y)]^4 - T_O^4 \}, \quad 0 \leq y < \infty, \quad (A-3)$$

where σ is the Stephen-Boltzmann constant and ϵ is the blackbody emissivity. The total rate of radiation transfer, per unit width, must balance the convection rate plus the rate of latent heat release at the freezing front; i. e.,

$$\int_0^\infty \epsilon \sigma \{ [T(-t, y)]^4 - T_O^4 \} dy + \int_0^\infty \epsilon \sigma \{ [T(t, y)]^4 - T_O^4 \} dy = 2t\rho v [C(T_F - T_O) + L] \quad (A-4)$$

where L is the latent heat of fusion. We will restrict our analysis to the symmetrical ribbon case, so that the two integrals on the left of (A-4) are equal.

One may linearize the radiation law by replacing $\epsilon \sigma (T^4 - T_O^4)$ with $\epsilon \sigma (T_F^3 + T_F^2 T_O + T_F T_O^2 + T_O^3) (T - T_O)$. If $\epsilon \sigma (T_F^3 + T_F^2 T_O + T_F T_O^2 + T_O^3)$ is denoted by H , conditions A-3 and A-4 become

$$|K \partial T(\pm t, y) / \partial x| = H [T(\pm t, y) - T_O] \quad (A-3a)$$

and

$$\int_0^\infty H [T(\pm t, y) - T_O] dy = t\rho v [C(T_F - T_O) + L] \quad (A-4a)$$

The condition to be satisfied at the freezing front, assuming it is the isothermal $T = T_F$, is

$$K |\bar{\nabla} T| - K_L |\bar{\nabla} T_L| = \rho L (\bar{\nabla} \cdot \bar{\nabla} T) / |\bar{\nabla} T| \quad (A-5)$$

where K and K_L are the thermal conductivities in the solid and liquid phases, and $\bar{\nabla} T$ and $\bar{\nabla} T_L$ are the temperature gradients in the solid and liquid phases,

Method of Solution

The solution of (A-2), subject to conditions (A-3a), (A-4a), and (A-5) is complicated by not knowing a priori the location of the freezing front. Another complication arises from a lack of information about the temperature gradients in the liquid. As for the latter, it is supposed, as in the introductory remarks, that the term $K_L |\nabla T_L|$ can be reduced to a negligible value. The procedure adopted here is to express the solution as a series of eigenfunctions which satisfies all conditions of the problem except (A-5). The coefficients of the expansion are then adjusted to minimize some measure of the imbalance of condition (A-5) along the freezing isotherm. This is simply the root mean square of the residuals at 21 points $[x_i, y_F(x_i)]$, with the x_i 's equally spaced on the interval $0 \leq x_i \leq t$. The coefficient search is done automatically by means of a Davidon-Fletcher-Powell minimization procedure.¹⁴ Further details of this search are given below.

The Eigenfunction Expansion

The following may be readily verified to satisfy (A-2), (A-3a), and (A-4a), in the solid silicon:

$$\frac{T(x, y) - T_o}{T_F - T_o} = \sum_{i=1}^{\infty} a_i e^{-v_i y} \cos \mu_i x / \cos \mu_i t \quad (\text{A-6})$$

with the μ_i 's satisfying the transcendental equations

$$\tan \mu_i t = H / \mu_i K, \quad i = 1, \dots \quad (\text{A-7})$$

where the roots occur in the positive odd-numbered quadrants, 1, 3, 5,

The v_i 's satisfy

$$K (v_i^2 - \mu_i^2) + \rho C v_i = 0, \quad i = 1, \dots \quad (\text{A-8})$$

The condition that $T(\pm t, 0) = T_F$ requires that

$$\sum_{i=1}^{\infty} a_i = 1 \quad (\text{A-9})$$

Also, condition (A-4a) requires that

$$\sum_{i=1}^{\infty} a_i / v_i = t \rho v [C(T_F - T_o) + L] / H(T_F - T_o) \quad (\text{A-10})$$

The eigenfunctions in (A-6) form a complete basis on $-t \leq x \leq t$.¹⁵ By Fourier analysis, one could ordinarily expect to complete the solution by selecting the coefficients to match a known temperature profile or gradient on a known curve, $y_F(x)$. As we have indicated, the main complication in determining a self-consistent solution is the fact that not only is $y_F(x)$ unknown, but the boundary condition (A-5) there is nonlinear. Before returning to the relaxation method for finding the a_i 's, we pause to point out some physical features of the solution.

Relationship of Thickness to Pull Speed

Since the effective environment radiation temperature is fixed by the design of the apparatus, the only independent variables in the process are the pulling speed and the melt temperature. If the latter is adjusted to keep $\nabla \cdot T_L$ at or near zero, the thickness, t , is minimized for any given pulling speed. All other quantities are the physical constants, which are enumerated in Table A-1. From a casual inspection of the equations, it might appear that the relationship between v and t is very implicit, particularly with respect to Equations (A-8) and (A-10). The situation becomes simpler when it is noted that only the first term of the summation in (A-10) is of any consequence: it is found, as documented in the later example, that a_1 is very close to 1.0 while none of the other coefficients can ever exceed 0.0025 for ribbon thicknesses below 0.5 cm. Furthermore, it can be easily verified that $\mu_1 t \ll 1$ for the given values of H and K , and for reasonable values of t . Then Equation (A-7) may be replaced by

$$\mu_1^2 = H/Kt \quad (A-7a)$$

Table A-1. Physical Constants Used in the Calculations

Constant	Value of Constant
T_F	1685°K
ρ	2.33 g/cm ³
$C_F = C_S(T_F)$	1.04 J/g - °K
L	1810 J/g
$K_F = K(T_F)$	0.216 W/cm - °K
K_L	0.6 W/cm - °K
ϵ	0.5
σ	5.669×10^{-12} W/cm ² - °K ⁴
$T_F - T_O$	300°K
H	$\epsilon \sigma (T_F^3 + T_F^2 T_O + T_F T_O^2 + T_O^3) = 0.0414$ W/cm ² - °K

With a little algebraic manipulation of (A-7a), (A-8), and (A-10), taking $i = 1$ only, it is possible to eliminate μ_1 and v_1 to obtain the following relationship:

$$v^2 t = K H (T_F - T_O)^2 / \rho^2 L [L + C(T_F - T_O)] \quad (A-11)$$

For the parameters of Table A-1, the right-hand side of Equation (A-11) has the numerical value $3.9 \times 10^{-5} \text{ cm}^3/\text{sec}^2$ (see Figure A-2).

Figure A-2. Relationship between total silicon thickness, $2t$, and growth velocity, v . Both curves obey a constant $v^2 t$ relationship. The lower curve is derived for the linear case with $T_F - T_O = 300^\circ\text{K}$. The upper curve shows the relationship for the non-linear case assuming parameters used by Bell.²

Angle of Freezing Front at Ribbon Surfaces

The angle of the freezing front with respect to the normal at the ribbon surface is given, according to Equation (A-6), by

$$\tan \theta = [\partial T(t, o) / \partial x] / [\partial T(t, o) / \partial y]$$

$$= \left(\sum_{i=1}^{\infty} a_i \mu_i \tan \mu_i t \right) / \left(\sum_{i=1}^{\infty} a_i v_i \right) \quad (\text{A-12})$$

Since $\mu_i \tan \mu_i t = H/K$ and $\sum a_i = 1$ by Equations (A-7) and (A-9), this becomes

$$\tan \theta = (H/K) / \left[\sum a_i v_i \right] \quad (\text{A-13})$$

Again using the approximation $a_1 = 1$, $a_i = 0$ for $i > 1$, we have

$$\tan \theta = (H/K) / v_1 = \rho v [C(T_F - T_O) + L] / K(T_F - T_O) \quad (\text{A-14})$$

from (A-13) and (A-10). Equation (A-11) can be used to eliminate t from (A-14), giving

$$\tan \theta = H(T_F - T_O) / \rho L v \quad (\text{A-14a})$$

For an extremely slow rate, $v = 0.01$ cm, (A-14a) gives $\tan \theta = 0.295$ or $\theta = 16.5$ degrees. For more reasonable pulling speeds (thinner ribbons), the angle would be smaller.

Determination of the Correct Freezing Isotherm

The approximation $a_1 = 1$ and $a_i = 0$ for $i > 1$ is excellent for determining v versus t and the corner angle of the freezing isotherm, but the heat balance (A-5) at the freezing isotherm is not satisfied. However, when the coefficients are properly adjusted, it is found that five terms in the expansion (A-6) are adequate to balance Equation (A-5) over $-t \leq x \leq t$ very precisely. Letting $U(\bar{a}, x, y) = U(a_1, a_2, a_3, a_4, a_5, x, y)$ denote the five-term approximation to $T(x, y)$, we have

$$\frac{U(\bar{a}, x, y) - T_O}{T_F - T_O} = \sum_{i=1}^5 a_i e^{-v_i y} \cos \mu_i x / \cos \mu_i t \quad (\text{A-15})$$

The problem then is to adjust $\bar{a}$ until some measure of the error in (A-5) is minimized, where the freezing front, $y_F(\bar{a}, x)$, must be redetermined each time $\bar{a}$ is changed. For the error measure, we use

$$E(\bar{a}) = 100 \left[\sum_{j=1}^{21} (r_j)^2 / 20 \right]^{1/2} \quad (\text{A-16})$$

in which the residuals [see Equation (A-5)]

$$r_j = 1 - (\rho LV/K) \left| \partial U / \partial y \right| / \left| \nabla U \right|^2 \quad (\text{A-17})$$

are evaluated at 21 points on the freezing front:

$$y_F(\bar{a}, x_j); x_j = (j - 1)t/20, j = 1, \dots, 21 \quad (\text{A-18})$$

Since the coefficients are constrained by $\sum_{i=1}^5 a_i = 1$, the minimization of $E(\bar{a})$ may be viewed as a sequential search over the four-dimensional coefficient space a_2, a_3, a_4, a_5 , with $a_1 = 1 - a_2 - a_3 - a_4 - a_5$. The Davidon-Fletcher-Powell algorithm works very well for this purpose. This uses a sequence of subsearches (line searches) along different specified directions in the four-dimensional space, each of which yields a further reduction in $E(\bar{a})$. The sequence terminates when at some $\bar{a} = \bar{a}^*$, the partial derivatives of E with respect to the coefficients are all equal to zero.

The example selected was $2t = 0.5$ cm. Initial values for the coefficients were $a_1 = 1$, $a_2 = a_3 = a_4 = a_5 = 0$. The quantities $K |\nabla U|$ and $\rho L(\bar{v} \cdot \nabla U) / |\nabla U|$ on the freezing front are plotted in Figure A-3 (solid traces), along with the same quantities for the optimum set of coefficients (dashed trace):

$$\begin{aligned} a_1 &= 1.002418 \\ a_2 &= -2.329 \times 10^{-3} \\ a_3 &= -5.766 \times 10^{-5} \\ a_4 &= -2.005 \times 10^{-5} \\ a_5 &= -1.135 \times 10^{-5} \end{aligned}$$

The corresponding freezing fronts are plotted in Figure A-4. The rms balance error (A-16) was reduced from 2.6 percent initially to 0.014 percent.

Figure A-3. The coefficients of the expansion (A-15) are adjusted until the condition $K|\nabla U| = \rho L (\nabla \cdot \nabla U)/|\nabla U|$ is satisfied along the freezing front. Solid curves (corresponding to $a_1 = 1$; $a_2 = a_3 = a_4 = a_5 = 0$) show large error. After minimization of the error, the two curves virtually coincide (dashed trace).

Figure A-4. Freezing front contours before and after adjusting the coefficients of the expansion (A-15). Note the 5:1 scale difference between x and y .

It is clear from Figure A-4 that the initial value of the corner angle, θ , as given by (A-14), was unchanged in the final solution, but that the isotherm is more curved in the final solution. This rather unrealistic example was chosen to exaggerate the balance errors. For more reasonable ribbon-pulling conditions, and hence thinner ribbons, the freezing front would be more planar, and the balance corrections in a_2 , a_3 , a_4 , and a_5 would also be smaller.

ONE-DIMENSIONAL ANALYSIS

One result of the previous analyses is that the transverse temperature gradients within the silicon are quite small. This suggests that a one-dimensional heat flow analysis can be useful. The present section presents such an analysis, includes the effects of the temperature-dependent thermal conductivity, and allows for nonlinear heat transfer at the surfaces of the silicon.

The basic one-dimensional heat flow equation follows from conservation of energy:

$$(t_1 + t_2) \left[\frac{d}{dy} \left(K \frac{dT}{dy} \right) - \rho C v \frac{dT}{dy} \right] = f_1(T) + f_2(T) \quad (A-19)$$

where the functions f_1 and f_2 represent the surface heat transfer functions, or cooling functions, and have units of watts/cm², for example. The main assumption here is that the functions f_1 and f_2 are functions of temperature only, and do not depend explicitly on y . The Stefan-Boltzmann law [the left-hand side of (A-3) above], or Newton's law of cooling [the left-hand side of (A-3a) above] are examples of such heat transfer functions.

It is convenient to let $t_1 + t_2 = 2t$ and $f_1 + f_2 = 2f$ to facilitate comparison with the symmetrical case above, so that (A-19) becomes

$$\frac{d}{dy} \left(K \frac{dT}{dy} \right) - C \frac{dT}{dy} = \frac{f}{t} \quad (A-19a)$$

Since only the ratio f/t enters into the problem, the partial thickness t_1 and t_2 can always be chosen so that $t_1/t_2 = f_1/f_2$. We show below that t_1 and t_2 in general are the thicknesses measured from the maximum point in the freezing isotherm.

The boundary conditions on Equation (A-19) are at $y = 0$, the liquid-solid interface, and at $y = \infty$. At $y = 0$, we have the conditions $T(0) = T_F$, and

$$J_F = -K \left[\frac{dT(0)}{dy} \right]_F = -K_L \left[\frac{dT(0)}{dy} \right]_L + v\rho L = J_O + v\rho L \quad (A-20)$$

where J_O is the heat current density in the liquid at the interface. This is equivalent to Equation (A-5) above, but is simpler because it is not necessary in this case, to deal with an unknown liquid-solid interface. The boundary condition at infinity is simply $T = T_a$.

Specifying the temperatures at both ends and the gradient at $y = 0$ over-determines the solution, since only two boundary conditions may be specified in a one-dimensional second-order differential equation. Thus, a solution satisfying the boundary conditions generally does not exist for arbitrary combinations of J_O , v and t . Our model is intended to deal with an experimental situation in which there are really only two independent variables, namely v and the melt temperature. These determine both J_O and t for given cooling conditions (i. e., given $f(T)$). The precise relationships depend upon meniscus height and shape, the liquid transport phenomena, and other factors beyond the scope of this discussion. As stated in the introduction, we are mainly interested in the maximum t at a given v and we therefore consider the case $J_O = 0$.

We now show by elementary scaling considerations that the maximum thickness (at $J_O = 0$) varies inversely as the square of the pulling speed and that the distribution, $T(y)$, remains identical except for a scaling factor: $T(y)$ is elongated (compressed) in proportion to the increase (decrease) in v . To duplicate this situation experimentally when v is changed, the melt temperature must be adjusted to maintain $J_O = 0$.

Assume that v_O and t_O are parameters for which a solution to (A-19a) and (A-20) exists and consider the new parameters, v_1 and t_1 :

$$\begin{aligned} v_O &= v_1/a \\ t_O &= a^2 t_1 \\ [v_O^2 t_O &= v_1^2 t_1] \end{aligned} \quad (A-21)$$

Upon substituting (A-21) into (A-19) and (A-20), we find

$$\frac{d}{d(ay)} \left(t_1 K \frac{dT}{d(ay)} \right) - \rho c v_1 t_1 \frac{dT}{d(ay)} = f_1(T) + f_2(T) \text{ and } -K \frac{dT(0)}{d(ay)} = v_1 \rho L \quad (A-22)$$

so that the equations are identical after the transformation but with a new variable, $y_1 = ay$. It follows that v_1 and t_1 are also feasible parameters, that $T(y_1/a) = T(y)$, and that the product $v^2 t$ is an invariant of the problem, defining a maximum thickness for a given growth speed.

Equation (A-19) can be integrated once to give an explicit expression for the $v^2 t$ product. In terms of the heat current density $J = -K(dT/dy)$, Equation (A-19) is written as

$$-\frac{dJ}{dy} + \frac{v\rho C}{K} J = \frac{f}{t} \quad (A-23)$$

Now if we assume that T is a monotonic function of y , then $T(y)$ has an inverse function, $y(T)$, so that J can be expressed in terms of T and we can write:

$$\frac{dJ}{dy} = \frac{dJ}{dT} \frac{dT}{dy} = -\frac{J}{K} \frac{dJ}{dT} \quad (A-24)$$

and (A-23) becomes

$$J \frac{dJ}{dT} + \rho C v J = \frac{K f}{t} \quad (A-25)$$

This can be integrated with respect to temperatures to give

$$J^2 + 2\rho v \int_{T_a}^T C J dT = \frac{2}{t} \int_{T_a}^T K(f) dT \quad (A-26)$$

since $J(T_a) = 0$.

Because of the convective term, this equation is an integral equation for $J(T)$. The linear analysis above, however, showed that the convective term is not very important, since it simply adds to the latent heat. It is appropriate, therefore, to approximate it by a mean value. A convenient assumption which gives the qualitatively correct behavior of J is that $J(T)$ follows a power law: $J = b(T - T_a)^\gamma$, where γ is to be determined.

Then (A-25) becomes:

$$J^2 + \frac{2}{\gamma+1} v\rho \bar{C} (T - T_a) J = \frac{2}{t} \int_{T_a}^T K(f) dT \quad (A-27)$$

where $\bar{C}$ is the mean value of C in the sense that it can be taken outside the integral in (A-26).

The heat current density at the freezing front ($T = T_F$) is given by:

$$J_F^2 + \frac{2}{\gamma+1} v\rho C (T_F - T_a) J_F = \frac{2}{t} \int_{T_a}^{T_F} K(f) dT \quad (A-28)$$

combining (A-28) and (A-29) gives

$$v^2 t = \frac{2}{\rho^2 L \left[L + \frac{2}{\gamma+1} \bar{C}(T_F - T_a) \right]} \int_{T_a}^{T_F} Kf \, dT \quad (\text{A-29})$$

This is an equation for the maximum $v^2 t$ product which is an invariant of the problem. The effect of the convection term is to decrease the product by an amount which depends on the sensible heat, $\bar{C}(T_F - T_a)$, to the latent heat, L . The product depends on the integral of the surface heat transfer functions f_1 and f_2 .

We note that (A-29) is equally true for the partial thicknesses t_1 and t_2 when the functions f_1 or f_2 are used in the integrand, or for the total thickness, $t_1 + t_2$, when $f_1 + f_2$ is used.

The effect of a gradient in the liquid ($J_o \neq 0$) can be seen by substituting (A-20) into (A-28). It is clear that the effect of J_o is to replace L by $L + J_o/v$ and that the effect of a positive J_o is always to decrease the $v^2 t$ product. Thus, the analysis predicts that the maximum thickness at a given velocity occurs with $J_o = 0$ consistent with the general observation in growth from the melt as discussed in the Introduction, and with the experimental observations of EFG and SOC growth.

In the first part of this analysis, a specific two-dimensional "worst-case" problem was solved by numerical analysis. It is of interest to compare the results with the analytic expressions. In the expression for the $v^2 t$ product, there is a parameter, γ . It is easy to show that $\gamma = 1$ for the linearized problem. If we take f equal to $H(T - T_a)$, the solution to (A-19) is of the form $T = T_a + (T_F - T_a) \exp(-\beta x)$, with

$$\beta = \frac{v \rho L}{K(T_m - T_a)} = -\frac{v \rho c}{2K} + \sqrt{\frac{\rho^2 C^2 v^2}{4K^2} + \frac{H}{4t}} \quad (\text{A-30})$$

Solving this for the $v^2 t$ product gives Equation (A-11) identically which was derived for the two-dimensional treatment. We also note that (A-29) reduces immediately to (A-11) if $f = H(T_F - T_a)$ and $\gamma = 1$.

Finally, a way to estimate γ is needed in the general case. One method is to calculate $J(T)$ using (A-26) without the convective term. For example, suppose that f is proportional to T^4 and that $K = K_F T_F/T$ as is the case for silicon. Neglecting the convective term, J^2 will be proportional to the integral of T^3 , or J is proportional to T^2 and $\gamma = 2$. Thus, the value of γ lies between the rather narrow limits of 1 for the linearized case, and 2 for radiative cooling with $T_a \ll T_F$. Since the temperature gradients are highest near the freezing fronts, it is clear the weighted average of the specific heat will weight values near the freezing front the highest. Thus, $C = C_F$ is a reasonably good estimate.

It is perhaps useful to write down at this point a specific expression for the v^2t product for the cooling laws generally assumed, namely:

$$f_1 = f_2 = \epsilon \sigma \left(T^4 - \sum_i \epsilon_i \alpha_i T_i^4 \right) + G(T - T_a) \quad (A-31)$$

and

$$K = K_F T_F / T \quad (A-32)$$

where α_i is the fraction of the solid angle radiating to the surface of the silicon with emissivity ϵ_i and temperature T_i . The result of (A-29) is

$$2v^2t = \frac{K_F T_F \left[\epsilon \sigma (T_F^4 - T_a^4) - 4\epsilon \sigma \left(\sum_i \epsilon_i \alpha_i T_i^4 \right) \ln \frac{T_F}{T_a} + G(T_F - T_a) - G T_a \ln \frac{T_F}{T_a} \right]}{\rho^2 L \left[L + \frac{2}{3} C_F (T_F - T_a) \right]} \quad (A-33)$$

where $2t$ is the total thickness and we have explicitly used $\gamma = 2$, assuming that the radiation term dominates. We reiterate that the main assumptions in deriving this equation are 1) J_o may be neglected, and 2) the solid angles α_i do not depend explicitly on y .

As a specific example, we can calculate the v^2t product using the parameters assumed by Bell.² (In addition to the values tested in Table A-1 per silicon, Bell assumed $T_a = 300^\circ\text{K}$, $\sum G_i \alpha_i T_i^4 = T_a^4$ and used a value of $G = 1 \times 10^{-3} \text{ W/cm}^2\text{ }^\circ\text{K}$ for convective cooling. These numbers give $2v^2t = 3.2 \times 10^{-4} \text{ cm}^3/\text{sec}^2$, which is plotted in Figure A-2. The product is about 25 percent less than that calculated from the limiting velocity obtained by Bell using a numerical procedure and somewhat different boundary conclusions at the cold end. Both his calculation and the present one have many features in common: one-dimensional heat flow, inclusion of convective heat transport, non-linear surface cooling and the temperature dependence of K .

Liquid-Solid Interface Angle

The above analysis can be extended to provide a simple formula for the angle of the freezing isotherm with respect to the surface of the silicon. Consider the boundary condition, Equation (A-20), in the vicinity of the trijunction (liquid-solid vapor junction). The heat current density, J_F , in the solid and J_o in the liquid are actually vectors perpendicular to the isotherm, as shown in Figure A-5. The component of v along these vectors products a heat current density so that

$$J_F = J_O + \rho L v \cos \theta. \quad (A-34)$$

where the horizontal component of J_F is $J_F \sin \theta$, and must equal the heat loss function $f_1(T)$. Thus:

$$\sin \theta_1 = \frac{f_1(T_F)}{\rho L v \cos \theta_1 + J_O} \quad (A-35)$$

From the previous analysis we know that θ_1 is small, so that

$$\theta_1 = \frac{f_1 T_F}{\rho L v + J_O} \quad (A-36)$$

When $J_O = 0$, this agrees with (A-14a).

Figure A-5. Detail of Figure A-1b showing liquid-solid interface. Heat currents J_O in the liquid and J_F in the solid are perpendicular to the freezing isotherm.

Curvature of the Freezing Isotherm

An expression for the radius of curvature of the freezing isotherm can be derived following the same assumptions used above. Consider a point P along the isotherm and choose a rotated coordinate system (x', y') with x' along the isotherm and y' along the normal, as shown in Figure A-6.

Figure A-6. A cylindrical approximation to the liquid-solid interface. The partial thicknesses t_1 and t_2 are measured from 0 to each surface.

The first equation in this system is:

$$\frac{\partial}{\partial y'} \left(K \frac{\partial T}{\partial y'} \right) + K_m \frac{\partial^2 T}{\partial x'^2} = \rho c v \frac{dT}{dy'} \cos \theta \quad (\text{A-37})$$

where K_m appears in the second term because $K(T)$ is constant along x' .

The temperature in the vicinity of P can be written as a Taylor series:

$$T(x', y') = T_m + \left(\frac{\partial T}{\partial y'} \right)_0 y' + \frac{1}{2} \left(\frac{\partial^2 T}{\partial x'^2} \right)_0 x'^2 + \frac{1}{2} \left(\frac{\partial^2 T}{\partial y'^2} \right)_0 y'^2 \quad (\text{A-38})$$

where $\partial T / \partial x'$ and $\partial^2 T / \partial x' \partial y'$ vanish because the x' axis is tangent to the isotherm. Choosing x' and y' to be on the isotherm gives a relationship between x' and y' .

If the isotherm were a circle, its radius would be given by:

$$r = \lim_{y' \rightarrow 0} \left(-\frac{x'^2}{y'} \right) = \frac{\frac{\partial T}{\partial y'}}{\frac{\partial^2 T}{\partial x'^2}} \quad (\text{A-39})$$

$$\frac{1}{r} = \frac{\frac{\partial}{\partial y'} \left(K \frac{\partial T}{\partial y'} \right) - \rho c v \frac{\partial T}{\partial y'} \cos \theta}{\rho L v \cos \theta + J_0} \quad (\text{A-40})$$

In particular, for the curvature at the highest point of the isotherm ($\theta = 0$, $y' = y$), we can use (A-19),

$$\frac{1}{r} = \frac{f}{t} \frac{1}{v \rho L + J_0} \quad (\text{A-41})$$

where the convective transport term does not appear. If we let $2t = t_1 + t_2$, and $2f = f_1 + f_2$, we can write

$$\theta_1 = \frac{t_1}{r} = \frac{f_1}{v \rho L + J_0} \quad \text{and} \quad \theta_2 = \frac{t_2}{r} = \frac{f_2}{v \rho L + J_0} \quad (\text{A-42})$$

which is exactly the same as (A-36). Thus, the curvature arrived at by considering two-dimensional heat flow is totally consistent with the edge angle deduced by considering heat flow in the vicinity of the edge. The analysis is also consistent in the case that f_2 is negative and heat flows from the substrate to the silicon. In this case, θ_2 and t_2 are negative quantities. In the case of unsupported ribbon growth, there is complete symmetry and $f_2 = f_1$, etc.

SUMMARY AND CONCLUSIONS

We have discussed in some detail the heat transport in sheet growth of silicon from the melt, as it affects the thickness at a given growth speed, and as it affects the shape of the liquid-solid interface. We presented a procedure for solving the two-dimensional linearized problem, and showed that there is a tradeoff between growth speed and thickness. This $v^2 t$ tradeoff directly follows from the nature of the one-dimensional heat flow equation and its boundary conditions. Based on approximations that are suggested by the two-dimensional results, we derive simple expressions for the $v^2 t$ product and the angle and curvature of the freezing isotherm that give excellent agreement with the two-dimensional case but also apply to the general nonlinear case.

The main limitations of our analysis are: 1) the assumption of surface heat transfer terms that are functions of temperature only, and not of position along the sheet; and 2) the assumption of zero temperature gradient at the liquid edge of the liquid-solid interface. Because of latter assumption, the $v^2 t$ product gives the maximum thickness at a given v , as limited by the surface cooling.

ACKNOWLEDGEMENTS

The authors gratefully acknowledge helpful discussions with L. E. Scriven, N. E. Bixler, R. A. Brown, and W. J. Silliman of the University of Minnesota Coating Flows Group, and M. Leipold and F. Wolfe of the Jet Propulsion Laboratories. This work presents results of research performed for the Low-Cost Solar Array Project, Jet Propulsion Laboratory of the California Institute of Technology, sponsored by the Department of Energy through an interagency agreement with the National Aeronautics and Space Administration.

REFERENCES

1. "The EFG process applied to the growth of silicon ribbons," J. G. Swartz, T. Surek, and B. Chalmers, J. Electronic Materials, 4, 255-279 (1975).
2. "Thermal analysis of single-crystal silicon ribbon growth processes," A. E. Bell, RCA Review 38, 109-139 (1977).
3. "Maximum growth rates for melt-grown-ribbon-shaped crystals," T. F. Ciszek, J. Appl. Phys. 47, 440-442 (1976).
4. "Theory of shape stability in crystal growth from the melt," T. Surek, J. Appl. Phys. 47, 4384-4393 (1976).
5. "Shape stability in float zoning of silicon crystals," T. Surek and S. R. Coriell, J. Cryst. Growth 37, 253-271 (1977).
6. "The edge-defined film-fed growth of controlled-shape crystals," T. Surek, B. Chalmers, A. Mlavsky, J. Cryst. Growth, 42, 453-465 (1977).
7. "Surface morphology and shape stability in silicon ribbons grown by the edge-defined, film-fed process," T. Surek, C. B. Hari Rao, J. C. Swartz, and L. C. Garone, J. Electrochem. Soc., 124, 112-123 (1977).
8. "Growth, evaluation and modeling of silicon-on-ceramic solar cells," J. D. Zook, S. B. Schuldt, R. B. Maciolek, and J. D. Heaps. Thirteenth Photovoltaic Specialists Conf. - 1978, IEEE Press (1978), pp. 472-478.
9. "Thermal analysis of solidification in web-deudritic ribbon growth," M. D. Harrill, G. A. Rhodes, J. W. Faust, and R. B. Hilborn, J. Crystal Growth 44, 34-44 (1978).
10. "Continuous polycrystalline silicon layers on carbon substrates," C. Belouet, J. J. Brissot, R. Martres, Ngo Tich Phuoc, in "Photovoltaic Solar Energy Conference, Luxenbourg, September, 1977. D. Reidel Publishing, Holland (1978).
11. Solar cells on RAD polycrystalline silicon," E. Fabre, S. Makrain-Ebeid, and Y. Baudet, Thirteenth PV Specialists Conf. op. cit., pp. 1101-1105.

12. "The growth of crystals from liquids," J.C. Brice, North-Holland Press (1973), pp. 160-170.
13. "Conduction of heat in solids," H. S. Carslow and J. Jaeger, Second Edition, Oxford Univ. Press, 1957.
14. "Applied Nonlinear Programming," D.M. Himmelblau, McGraw Hill (1972), p. 111.
15. Carslow and Jaeger, op. cit., p. 114.

☆U.S. GOVERNMENT PRINTING OFFICE:1979 -640-014 4457 REGION NO. 4