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A TRD Trigger for the Tevatron Collider Experiment at D0

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Abstract

A VME-based module for use as an input to the D0 Detector Level 1.5 Trigger is described. Its main function will be the confirmation of electron candidates flagged by the First Level Calorimeter Trigger using digitized data from the Transition Radiation Detector. Features of the board include the use of fast FIFOs to store incoming track coordinates, dual ported SRAM lookup tables for addressing integrated charge data and forming scalars, multiplier/accumulators for speed of calculation, and a single synchronous finite state machine to control all board operations.

I. INTRODUCTION

A. The D0 Triggering System

An hierarchical triggering system[1] has been implemented for D0 since the expected proton/antiproton interaction rate of 50,000 per second would generate too much information to be realistically expected to be written to tape. This triggering system, which is designed to direct only the most interesting events to tape, consists of four levels. Level 0 determines whether an interaction has taken place, and if so, broadcasts its longitudinal position. Level 1 transforms calorimeter information into global energy and local energy cluster counts, with a table of electron candidates; it also uses hodoscopic muon information to find muons in broad roads. The Level 1 system can trigger data acquisition in the time between beam crossings (which occur every 3.5μsec). It is adjusted to reduce the trigger rate to ~200 Hz on the average. Level 1.5 consists of triggers derived from data from the Muon system and from the Transition Radiation Detector(TRD). The Muon trigger fires when a muon above some Pt threshold is found. The TRD trigger module receives the table of electron candidates from the First Level Trigger Framework and sends a trigger back if an electron was found. Each of these triggering systems outputs its decision to the Trigger Framework, which processes the trigger information and then signals the data acquisition crates if readout of the event is desired. The data from these crates is then sent to the Level 2 MicroVAXes where further analysis is done on the data to limit writing only one to two events per second to tape.

Because the level 1.5 triggers do not provide trigger information in the time between beam crossings, they introduce "dead time" since the Trigger Framework must wait for the information. The TRD Trigger must do dozens of read cycles over the VME bus to get information to form its trigger. Thus, it has features that serve to optimize speed in order to minimize the number of missed beam crossings.

B. Using the TRD as Input for a Trigger

It is predicted that high energy electrons will be produced in certain decay modes of the top quark and other particles of interest to D0. The TRD is particularly suited to electron identification. In a TRD, a highly relativistic charged particle will "shake off" some of its field[2] when it traverses the interface of two materials having different dielectric constants. A photon is thus emitted. An electron is most likely to produce transition radiation due to its low mass; all other particles will not incite transition radiation unless they have very large kinetic energy. The D0 TRD has many layers of thin polyethylene sheets with Nitrogen gas between each layer. This forms the "radiator". Surrounding the radiator is a gas-filled wire chamber where the impinging photons ionize the gas and produce signals on the wires. There are three such layers in the D0 TRD, arranged in concentric fashion.

The TRD Trigger is a crude hardware trigger that signals the Trigger Framework if the charge deposited on three radially-aligned wires exceeds some threshold. Before comparison to this threshold, however, a normalizing factor must be applied depending on the angle the track makes with the axis of the detector, since the charge deposited on the wire is proportioinal to the path length through the chamber.

II. OVERVIEW

A. Data Acquisition System

The Central Tracking data acquisition system[3] is served by 36 VME crates, each of which houses a number of 16-channel Flash A/D converter boards (FADCs). Each FADC channel digitizes the amplified and cable-compensated analog waveform received from each chamber wire. The digitization rate is 106MHz and lasts for approximately two microseconds beginning at each beam crossing. When a Level 1 Trigger occurs, digitization of further crossings ceases, and the data from each channel *may* be compressed by storing in its output register only the track's pulse and giving it a time stamp relative to the collider's beam crossing. To accomplish this, each channel employs a Fermilab-designed application-specific integrated circuit (ASIC) called

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the Zero-Suppression Chip (ZSP). The ZSP also calculates the sum of the values of each digitized bin and stores this number in a "Sum" register. It is this register that the TRD Trigger reads to help determine whether an electron traversed the TRD.

There are twelve FADCs in each of eight TRD crates, where four of the crates serve TRD cathodes, and the other four serve TRD anodes. The TRD Trigger uses anode information, so there is one TRD Trigger board in each of the four anode crates. Each of these crates represents one quadrant of the TRD, or 192 anode channels.

the TRD Trigger uses to indicate confirmation of an electron. GO tells the TRD Trigger that the last electron candidate coordinate for the present crossing has been sent.

C. IncomingCoordinates

A single Z number representing the vertex of an interaction is the first coordinate to be latched in the TRD Trigger following a beam crossing. This number is strobed at approximately the same time as the Level 1 trigger. The number is a four-bit number plus a sign bit where the

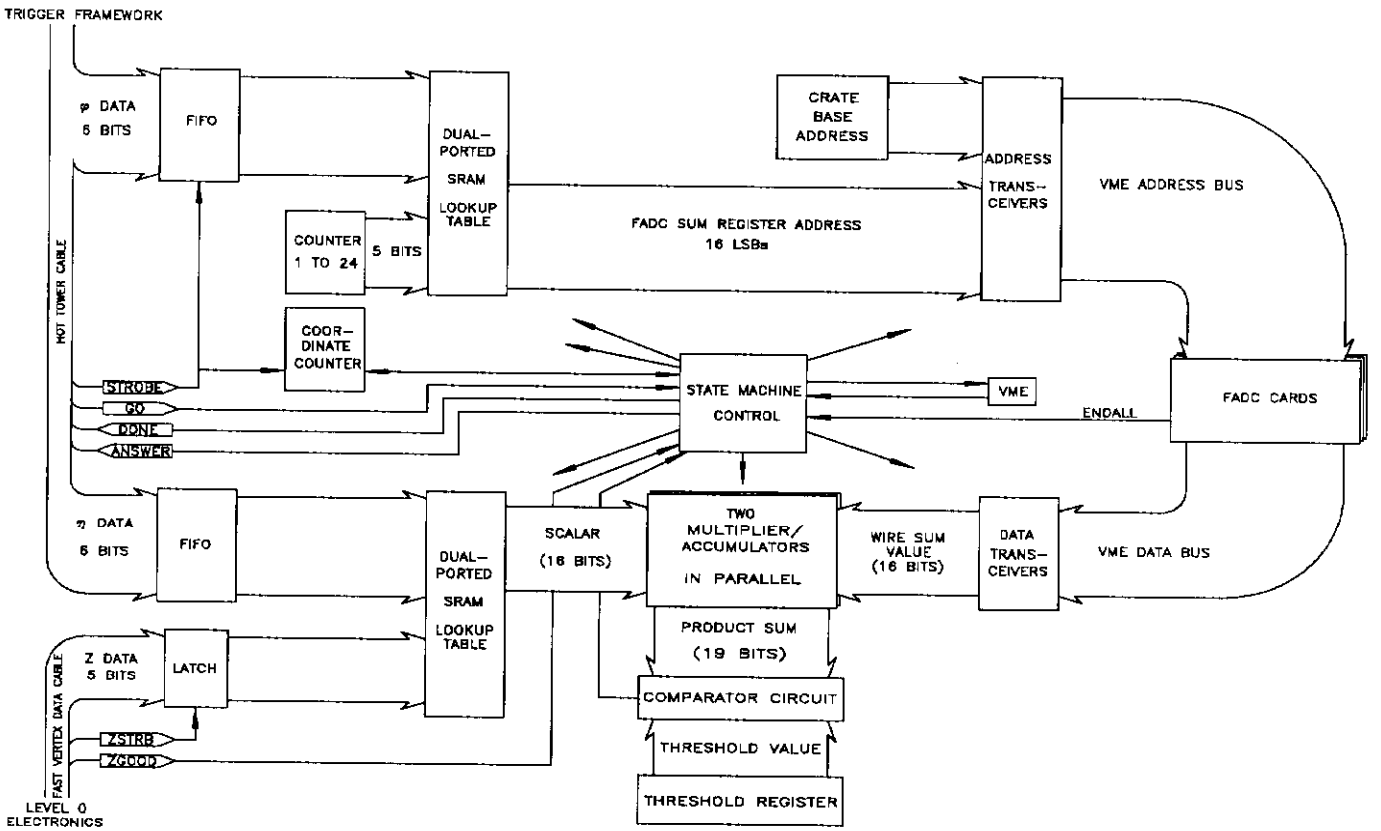

Figure 1. Block diagram of the TRD Trigger and its interconnections.

B. System Interconnections

Figure 1 shows a block diagram of the TRD Trigger and its interconnections. There are two ribbon cables which interface the TRD Trigger to systems external to the crate. One cable carries a five-bit number indicating z-position of an interaction, and originates at the Level 0 electronics. The other cable provides the six-bit phi(azimuthal angle) and eta(pseudo-rapidity[1]) coordinates as determined by the First Level Calorimeter Trigger in the Trigger Framework. There are additional handshaking signals on each ribbon cable such as data-valid strobes and the DONE and ANSWER lines that resulting 31 bins are each equivalent to 6.25 cm along the Z-axis of the detector. The number is derived by the Level 0 electronics from signals that originate on two counter hodoscopes, one positioned around the beampipe on the north endcap calorimeter, the other similarly positioned on the south endcap calorimeter. If the Level 0 electronics cannot calculate a vertex number, which can happen if there was no interaction for the current beam crossing or if the interaction vertex was outside the defined bins coverage, the ZGOOD bit will not be asserted. If the ZGOOD bit is not asserted, the TRD Trigger immediately signals the Trigger Framework that the Level 1.5 trigger has not passed.

The remaining two coordinates, Phi and Eta, are simultaneously strobed into separate FIFOs during the first few microseconds following a Level 1 trigger. FIFOs are

[1]Pseudo-rapidity is defined as $\eta = -\ln(\tan\theta/2)$, where θ is the polar angle relative to the beam axis.

used because the Trigger Framework may send up to eight coordinate pairs, each pair representing the calorimeter tower in which a possible electron was found. The pairs are sent in order of decreasing likelihood of finding an electron, and the TRD Trigger examines the sum registers for each coordinate one at a time. A counter circuit called the "coordinate counter" increments each time a coordinate is strobed in. The state machine decrements this counter after each coordinate pair is examined, and monitors the "empty" pin so that it knows when to stop in the event that an electron is not found.

D. Data Processing and Trigger Forming

Each Phi coordinate represents a slice of the TRD equivalent to eight wires in each layer, or twenty-four wires total[2]. The Phi coordinate, therefore, is directly related to twenty-four FADC sum registers, and the output of the Phi valid FADC data is returned, it is multiplied by a sixteen-bit scalar which comes from a second lookup table, to be described below. The state machine decrements the address counter, and a new address corresponding to the same azimuthal location, but in the second layer, is formed. The second word of FADC sum data is returned, multiplied by the same scalar, and added to the product from the previous cycle. The same thing happens for the wire in the third layer, and a final sum is achieved. If an electron had gone through this slice of phi, the resulting sum will have a significant value, and should be larger than some threshold which can be chosen to reject the majority of other particles. This sum, therefore, is compared to such a threshold. If the threshold is exceeded, the state machine asserts ANSWER and one clock cycle later asserts DONE; this sequence tells the Trigger Framework that the TRD portion of the Level 1.5 trigger has passed.

In all likelihood, the trigger will not occur so

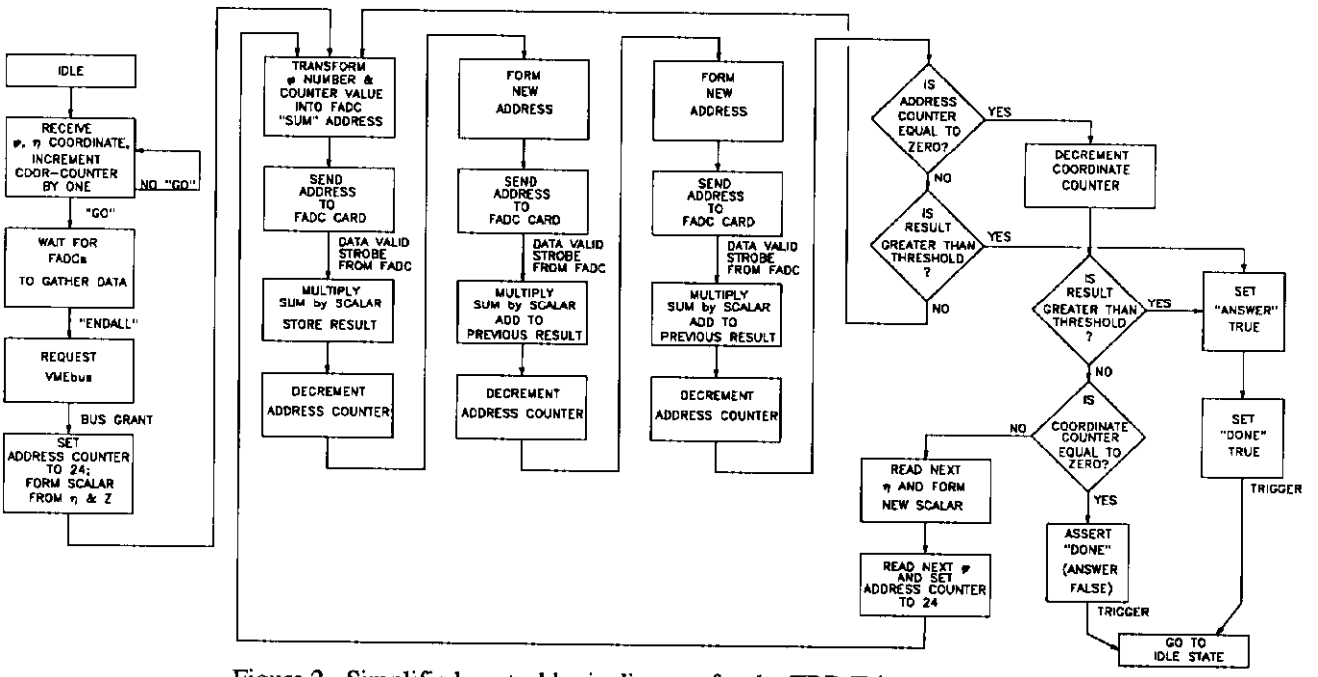

Figure 2. Simplified control logic diagram for the TRD Trigger state machine.

FIFO becomes the six most significant bits of input to the lookup table that forms the addresses of these registers. Another counter that decrements from 24 forms the five least significant bits of the lookup table. The lookup table has been pre-loaded with the proper address values, and the "address counter" is preset concurrently with each FIFO unload strobe. When the FADC cards signal that digitization is complete (the SUM registers are ready), the state machine requests control of the VMEbus and, once granted, begins the first VME cycle (see Figure 2). The first wire addressed is the first wire of that sector in the innermost layer. When immediately. In that case, the state machine loops back and examines the next three adjacent wires, and will continue this looping until all 24 wires for that sector have been examined (the address counter reaches zero) or until the threshold is exceeded. If the threshold is not reached, and the coordinate counter is not at zero, the next hot tower coordinate is examined. The state machine unloads the FIFOs which forms a new scalar and, along with presetting the address counter to 24, forms the address of the first wire in the next phi sector to be examined. All subsequent electron candidates are examined using these loops of the state machine. If all phi-eta coordinates have been examined and the threshold was not exceeded, the state machine asserts DONE without asserting ANSWER. This sequence tells the

[2]The outermost layer actually has sixteen wires per Phi coordinate, but adjacent pairs are summed in the electronics at the channel level.

Trigger Framework that the TRD portion of the Level 1.5 trigger has not passed.

E. The Scalar Lookup Table

As mentioned earlier, the amount of ionization caused by a photon travelling through a wire chamber is proportional to its path length. For this reason, a scalar is needed to normalize the values returning from the FADC sum registers so that comparison to a single threshold may be made to test for an electron. An array of scalars is pre-loaded into a lookup table, and is derived from both the Z and Eta coordinates. Although the value of the scalar can be thought of in simple terms as being proportional to $\sin\theta$, the actual value must be derived from connecting a straight line from the Z coordinate on the axis of the beam to the centroid of the calorimeter tower which produced the Eta coordinate. This line must then be superimposed on the outline of the TRD to determine relative path length. Since there are eleven bits at the input of the lookup table, there can be 2048 separate scalars. In practice, however, there are considerably fewer because the TRD does not provide full θ coverage and the outermost Z coordinates extend farther than the TRD. The lookup table consists of a pair of Cypress 2048 x 8 dual-ported SRAMs[3]. Scalars are downloaded via VME by matching the eleven least significant bits of the VME address bus with the corresponding five-bit Z and six-bit Eta coordinate combinations. The sixteen-bit scalar thus formed, when multiplied by the sixteen bit sum value, can form numbers as wide as thirty-five bits when three such products are added together. Of these thirty-five bits, only the most significant nineteen are sent to the comparator circuit. This allows sufficient precision and avoids the unnecessary complication of dealing with the sixteen LSBs which are multiplexed with the inputs of the Multiplier/Accumulator chips (MACs).

F. Threshold Comparison

The comparison circuit uses three common TTL magnitude comparators(74LS684) and a simple AND/OR configuration to test the nineteen bit output of the MACs against the nineteen bit value loaded into the threshold register. This register consists of three 8-bit D-type read-back latches(74ALS996) which are loaded via VME. The flexibility offered in allowing the scalar and threshold to be adjustable from the D0 control room is valuable in that the downloaded values can be "tuned" to optimize performance.

G. The Multiplier/Accumulators

The Analog Devices ADSP1010A was chosen to perform the math the TRD Trigger uses because this device has a fast multiply/accumulate time (65ns), and because the required algorithm can be easily implemented by manipulating its few control lines by the state machine. These control lines are separate strobes for each input register, a strobe line telling the chip to multiply, two lines for tri-stating the outputs, and one line that clears the output register.

Two MACs are used on each TRD Trigger in order to allow for the case whereby two adjacent wires share a track's charge. When a bit is set in the card's control register, the board will perform the multiply/accumulate sequence in both MACs. A toggle flip-flop in the state machine alternately enables only one MAC's output pins at a time. It also alternately clears the MACs after every three wires so that the effective result is instead of adding only three radially-aligned wires, it adds two adjacent sets of three wires, and compares. Each subsequent comparison overlaps the last three wires. This algorithm allows fewer potentially good triggers to pass unnoticed and creates no more dead time than reading and comparing three wires at a time.

H. Speeding Up the Trigger

In order to speed up the decision process, a feature exists whereby the TRD Trigger performs a preliminary calculation to eliminate coordinates which obviously do not have record of an electron. It can achieve this because each FADC board has a readable register called the BSUM register which sets a bit if the integrated charge on a channel exceeds some settable threshold. The BSUM register is sixteen bits wide, one bit from each channel's Zero Suppression Chip. Upon receiving GO, the TRD Trigger first analyzes the BSUM registers and flags any Phi coordinate for which none of its 24 associated bits is set. These Phi coordinates (and their associates Etas) are skipped when the TRD Trigger enters into its main analysis sequence. This feature is only a rough elimination scheme; it cannot take the place of the actual TRD Trigger operation since there is no Eta-Z scaling performed on the FADC card. The threshold for each FADC channel, therefore, must be set for an electron with maximum transverse trajectory to prevent rejecting possible good events while in this mode.

This mode may be selected by setting a bit in the TRD Trigger's control register. After the state machine recognizes it has control of the VMEbus, and this bit is set, it jumps to a small loop where it sets the address counter to twelve and disables the FIFO output. The addresses emerging from the FADC Sum lookup table are those of the BSUM registers. Incoming data from the twelve BSUM registers is sent to an EPLD[4] which is set up to correlate the bits as they relate to Phi sectors. Since there are eight Phi sectors in a crate (quadrant), there are eight output bits from this EPLD; any output bit at a logic 1 represents a flagged Phi sector where none of its channels exceeded the threshold set in the Zero-

[3]The same pair of Cypress chips(CG7C132, CG7C142) is used for the Sum address lookup table.

[4]Intel 5C180, which has 48 macrocells, 68 pins, and is relatively inexpensive.

Suppression Chip. After these bits have been set, the main sequence of the state machine begins. As each Phi emerges from the FIFO, the six Phi bits are compared, in a second EPLD, to the status of the eight lines flagged by the first EPLD. If a match occurs, indicating no possible electron, a bit is set and the state machine simply unloads the FIFOs so the next Phi-Eta coordinate pair emerges.

This operation can save considerable time. Each Phi-Eta coordinate takes approximately 16μs to examine. If we examine the case when the Trigger Framework sends the maximum of eight coordinate pairs, and the TRD Trigger examines all eight and finds no hits, the total maximum time from GO to DONE is 135μs. If BSUM mode is used and is successful in rejecting all coordinates, the time is reduced to 12μs. If, however, the tracks were such that BSUM mode eliminated nothing, the maximum time could be extended to 147μs.

I. The State Machine

A single, synchronous, finite state machine controls and synchronizes board operations from initializing counters and arbitration of the bus to addressing FADC registers, processing the data, and forming the Level 1.5 decision. The design quite fully utilizes the resources of an Altera EPM5128 MAX EPLD, which consists of 128 macrocells and 256 product terms, and has a t_{pd} of 25ns. The state machine uses all of its available pins, i.e., 20 input signals and 34 output signals. By using such a large device, the complications of putting a large state machine into several EPLDs, and trying to keep all operations synchronized, are avoided. By the same token, a single large state machine is advantageous in this case because the functions of the board occur sequentially; one machine can handle the task nicely and no board operations will be out of step.

J. Information for the Data Stream

The TRD Trigger provides three longwords of data which are available to the VMEbus and can be read by the VME Buffer-Driver (VBD), whose main function is to put digitized FADC data onto the Data Cable which goes to the Level 2 nodes. These three longwords are: 1) FADC address of the outermost wire whose charge helped to cause the Level 1.5 trigger; 2) The Phi, Eta, and Z coordinates associated with the Level 1.5 trigger; 3) The output value of the MAC that exceeded the threshold and caused the Level 1.5 trigger. The data is double-buffered to correspond to the double-buffering of the FADC boards.

K. Diagnostics

In the event that the board needs to be tested or if the loaded values in the lookup tables need to be tested, diagnostic features exist on the board. Simulated Phi, Eta, and Z coordinates may be sent in a special diagnostic mode to VME-accessible registers. Using this mode, a total simulation of the TRD Trigger function may be made, as if data taking were actually occurring. Registers are also available for reading the FIFOs' outputs, and bits exist in the control register for unloading and resetting the FIFOs.

III. CURRENT STATUS

Monte Carlo simulations[4] of the functioning of the TRD Trigger indicate that it will provide an average rejection factor of 2.2 (see Figure 3). Considering that the crate readout for one event will likely take more that 3ms, the additional time of a few hundred microseconds taken by the TRD Trigger to reject a few bad events will be miniscule compared to the time it would have taken to send those bad events to Level 2.

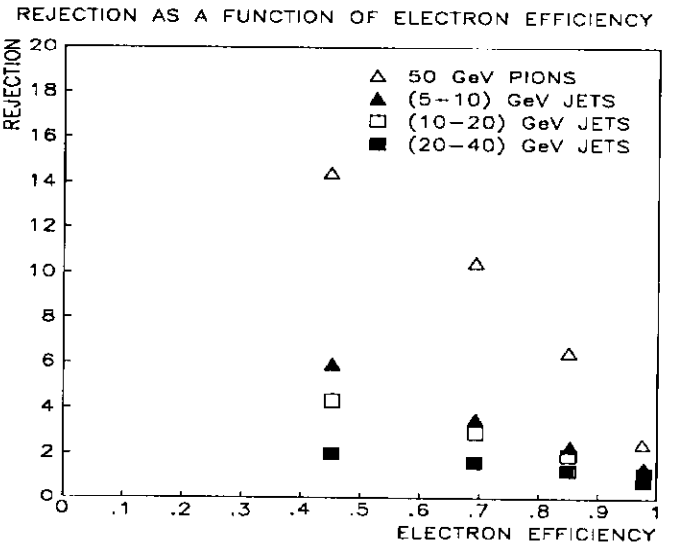

Figure 3. Monte Carlo results of a simulation of the TRD Trigger showing its effectiveness at rejecting pions and jets plotted against various electron efficiencies.

A single working TRD Trigger exists and awaits testing in the final environment. The remaining three modules, plus a spare, are currently being assembled.

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