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MASTER**Plans for Brookhaven Fastbus During the next $\pi \times 10^{16}$ Nanoseconds**

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PLANS FOR BROOKHAVEN FASTBUS DURING THE NEXT $\approx 10^{16}$ NANOSECONDS

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ABSTRACT

During this period new modules and devices will be built to be used in Experiment 749 at the A.G.S. Included will be ~200 channels of A-D converters for Pb-Glass Cerenkov counters, 2000 channels of proportional wire chamber readout, cable segments, segment interconnects, a new unibus interface, and a new on-segment processor. These items and perhaps others will be ready by the end of 1981.

For those of you who don't already know and care to know

$\pi \times 10^{16}$ nanoseconds = .996 year.

The work I will describe here is Brookhaven-Yale Fastbus. It has been used for about a year now at the AGS at Brookhaven to do all the data gathering for Experiment 735, a sensitive test of time reversal invariance in the decay $K^+ \rightarrow \pi^+ + \pi^0 + \nu$. In this experiment we measure the direction of polarization of the π^+ meson. Any component at all of this polarization out of the decay plane is an indication of time reversal invariance violation. The experiment will be completed this week, after running for about 1200 hours during the last year. We have processed over 20 million events through Fastbus and after the usual infant mortality failures the electronics has been remarkably stable.

We will describe the electronics and system in some detail, but we first address the question in part, "why should we build a fastbus?" We heard yesterday of a CAMAC system that will produce a truck-load of tapes a day. Fastbus was designed to be at least an order of magnitude faster. We don't need 10 truck-loads of tape per day. Perhaps some insight into this problem can be gained from my suggestion for the title for the next meeting in this series

**"Topical Conference on Computerized Data
Rejection in Particle and Nuclear Physics."**

If we are going to be able to afford to process the data we can get from our accelerators, we must reject the uninteresting events early in the data train. Indeed, if we are not going to lose all the good events in the dead-time generated by bad or uninteresting events we must reject the bad ones early. This is one of the major reasons for the development of Fastbus.

Enough of the generalities for now. For Experiment 735 we developed not only a system, with water cooled crates and the mechanics of conduction cooled modules, but, of course, the electronics of the modules themselves. To sum it up briefly, we developed the following devices:

1. Latch 32 channel/modules with 3 nanosecond coincidence and veto.
2. TDC 32 channels, each 6 bits wide with 0.1 μ sec resolution for timing μ decays.
3. MEM Look up Used by CONTROLLER to determine azimuthal segment of stopped μ 's. Uses FFLA's, since most of the memory would be filled with zeros.

4. CONTROLLER

Reads data (Latches and TDC). Examines data and either aborts or proceeds to accept data. Encodes bits and stores data. Based on 10801 sequencor chip and is micro-programmed.

5. MEMORY

30 nsec 4K x 16 or 2K x 32 bits FIFO,
FILO, or RANDOM ACCESS.

6. SCALER

2 versions, one commercial with
16ch x 32 bits, one home built
16ch x 28 bits.

7. PRE-DET

synchronize with AGS.

8. INTERFACE

FASTBUS $\longleftrightarrow$ UNIBUS (PDP11)
MAPS address (8 REG) (16 bit unibus
to 32 bit fastbus)
HANDLES INTERRUPTS
HANDLES BROADCASTS
DOES BUS ARBITRATION (FASTBUS)
DOES 8, 16 or 32 BIT transfers

Figure 2

The apparatus contained over 200 scintillation counters. Figure 1 is a schematic of the apparatus. K^+ mesons enter from the lower left and decay in the region on either side of the V counters. Only the mode of decay $K^+ \rightarrow \mu^+ + \nu^0 + \nu$ is of interest to this experiment. The μ^+ meson from the decay is bent by the toroidal focusing magnet into the polarimeter. Here the muon comes to rest in an aluminum wedge and has its spin precessed by an axial magnetic field. The μ^+ decays with a lifetime of 2.197×10^{-6} sec into a positron and 2 neutrinos. The positron is detected in one of the 32 pairs of counters inserted between the aluminum wedges. The field is reversed on each pulse of the AGS. The π^0 decays almost immediately into 2 gamma rays. The lead glass array at the end of the apparatus identifies at least one of these gammas.

```

graph TD
    PDP11[PDP-11] --- INTERFACE[INTERFACE]
    INTERFACE --- Bus
    Bus --- L1((L))
    Bus --- L2((L))
    Bus --- L3((L))
    Bus --- L4((L))
    Bus --- L5((L))
    Bus --- PREDEF[PRE-DEF.]
    Bus --- MEMORY1((MEMORY))
    Bus --- CONTROLLER[CONTROL-LER]
    Bus --- SCALER1((SCALER))
    Bus --- SCALER2((SCALER))
    Bus --- IACL((IA CL))
    IACL --- MEMORY2((MEMORY))
  
```

Figure 4

During the coming winter we will have a multi-segment system in operation for our new experiment, E749. Crates will be interconnected with cable segments. These are segments which obey the same protocol as the crate segments but are not restricted to crates. Units (modules) are interconnected on these segments by cables rather than with a backplane. Figure 5 shows a possible configuration for the new system. We will require ADC's for 240 channels of PB glass and a 2000 chamber, wire-chamber readout system as well as our current latches, memory, pre-det, and scaler system. We will probably build a new Host Interface with a cable segment between the Fastbus crate part and the Unibus part. A set of new processors will be built with RAM for program storage and with an ALU. These will then become truly computers.

Figure 3

The block diagram illustrates the data processing system for the wire chambers. At the top, a box labeled "HOST INTERFACE" is connected to a box labeled "SI". This "SI" box is connected to a horizontal bus line. Below this bus line, there are three "SI" boxes. The first "SI" box on the left is connected to the bus line. The second "SI" box in the middle is connected to the bus line and also to a vertical bus line that leads to three "ADC" boxes. The third "SI" box on the right is connected to the bus line and also to a vertical bus line that leads to a single "SI" box, which is then connected to a series of circles representing "WIRE CHAMBERS".

Figure 5

Debugging is always a problem. Our new system with its several segments, both crate and cable, will have available several debugging modules. We already have a static test stand for preliminary testing of modules. We also have software that works through the Host Interface for dynamic testing of the system. We will build a module with an 8085 μ -processor in it that will plug into the bus and allow both static and dynamic line by line tests of the bus and modules. This same module will also perform protocols to write, read, etc., modules from a terminal.

Figure 6

A Fastbus to CAMAC interface is planned. This CAMAC module will plug into the controller slots and connect externally with a Fastbus cable segment. This is shown schematically in Fig. 6. To fully address a CAMAC crate requires 5N lines, 4A lines, and 5F lines for a total of 14 Fastbus address bits. This would allow $2^{32-14} = 2^{18} = 128$ thousand CAMAC crates in the system.

I would return to general arguments now. Any standard to be useful must serve a large number of needs. The utility of a standard can often be increased by making it more complex. If the increased costs, both tangible and intangible, of the increased complexity is not outweighed by the increased utility, the complexity should not be added. We believe that the Brookhaven-Yale system has gone as far as the standard should go. There is no limit to the complexity that the user can incorporate in his explicit system nor should there be. However, to impose a narrow need upon all users of a system does no service to the community. The value of a standard is measured not by how many cute ideas are incorporated into it, but rather by what the value per cost is. A good standard knows when to stop.