PANEL ON THE IMPACT OF CHANGING COMPUTER TECHNOLOGY ON NUCLEAR AND PARTICLE PHYSICS*
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Large spectrometers which will play a major role at ISABELLE, with their many thousands of detector elements, can be expected to generate copious amounts of data. Considering also that some experiments may generate events at rates as high as 10^6 per second, it readily leads one to the conclusion that the data handling problems to be faced at ISABELLE will be quite formidable. In order to provide a basis for generating an appropriate model for computing at ISABELLE, the data handling group examined the needs of several possible detectors during the course of the 1978 Summer Study. While these proposed detectors may never see the light of approval they do represent a broad spectrum of computing requirements and detector complexity.

The five devices chosen for study were (1) small angle detector, (2) lepton detector, (3) wide angle detector, (4) axial field spectrometer, and (5) large aperture dipole spectrometer.¹ These devices are listed in order of increasing complexity and magnitude of data handling needs. The on-line computing requirements were estimated in terms of the canonical large machine at Brookhaven, the CDC-7600. The small angle detector generated 200-32 bit words per event at rates ranging from 100 to 1000 per second. An event analysis time of 2 msec to obtain kinematic parameters leads to an on-line requirement of $1/8$ of a 7600. An estimate for an axial field spectrometer at ISABELLE was based on a possible extrapolation of the ISR axial field spectrometer. A typical AFS event at ISABELLE will consist of 6000-32 bit words. Assuming a rate of two events per second and the time to reconstruct an event is about 2.5 seconds, we arrive at a requirement of two 7600s to service the AFS.

Given high event rates, the process of selecting the events for full analysis occurs in several stages, with more time available in consecutive stages as the amount of data being handled decreases. The data handling involved in the study of the inclusive production of jets at 90° using the two-arm spectrometer in the wide angle hall illustrates this process.² The most sensitive aspect of such an experiment is finding a trigger that selects a high p_T jet without bias and without excessive background. The jet can best be selected by utilizing fairly complete kinematic information on all its particles. To provide time to obtain this kinematic information a pretrigger that is unbiased for any real jets is required. The design goal was for a pretrigger based on single particle momentum and total energy content that operating in 200 to 300 nsecs could reduce the rate to about 10^4 per second. A slow trigger, based on topological properties of the event, was then added to reduce the rate to about 10 per second within a period of 50 μ sec.

The single particle trigger is made by demanding hits in the first three chamber planes corresponding to the bending coordinate through the use of pre-coded RAM matrices whose bits are set to one or zero depending on whether or not the particular three hit correlation is an allowed track. In constructing the slow trigger the assumption was made that criteria likely to be useful in selecting relatively unbiased jets are total energy above some E_{th} value and multiplicity of emitted particles. Achieving a total energy cut to be made with sufficient precision and speed a great need was seen for fast decision making special function processors.

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One special function processor (SFP) was chosen for specific study, the one responsible for finding tracks in the chambers and computing momenta. The specific problem addressed was that of computing the sum of the charged particle transverse momenta. The proposed processor is based on an architecture suggested by Sippach, and in principle is capable of finding and fitting tracks in the chambers 100 to 1000 times faster than a 7600.

It seems feasible to construct special function processors to act as triggers given fairly simple geometries. It is an open question as to the degree of generality which can be achieved with this approach. A group at Columbia University is attempting to develop a hardware architecture which can be applied to complicated detector geometries. Their goal is to produce a set of hardware modules which when suitably interconnected are capable of performing sophisticated calculations at extremely high speeds.³ The processing algorithm is represented in a hardware structure which attempts to maximize the parallelism of operation. Control and memory are distributed throughout the system so that the hardware partitions can operate autonomously. The information transmitted through the system consists of lists of data values, indices and two control bits called complete and valid. Valid means that the corresponding data element is a member of the data set to be processed by the module receiving the signal. The complete bit is generated at each level by the incidence of complete bits coming from lower levels, starting with the complete bit generated by each interface when it is done reading in data. There is a central clock and data moves in a pipeline sense at the clock rate.

During the 1978 ISABELLE workshop a description of a processor envisioned for an existing multiparticle MWPC spectrometer was presented. The spectrometer has three chambers in front of a magnet and two chambers in back of the magnet. Each chamber has U,V,Y,X views. Each of the 20 planes is read out as a sparse data set with each element encoded as a 10-bit binary number representing a particular wire hit. The different planes are encoded separately, so that these data sets can be processed concurrently. All possible wire pairs are tested, and as the computation proceeds, constraints are used to eliminate incorrect pairings. Tables of precomputed values which reflect the geometric relationships of the chambers are stored in modules requiring such data. Bit maps are used to provide a fast test of whether a triple of points satisfies a given relationship. The proposed design is based on ECL-10K technology and uses a basic clock cycle of 50 nsec. The time to calculate a track parameterization, a chi-square and the twenty plane wire set is estimated to be about 10 μ sec for a six track event. If this general scheme proves to be feasible it will clearly play a significant role in the computing strategy to be used in future experiments.

Leaving aside the role to be played by special function processors, let us next consider the subsequent stages of data handling. Once the decision is made to accept data from the detector the next stage of data handling is now typically managed by a PDP-11. In the future the PDP-11 will probably be replaced by one or more microprocessors, depending on the number of logically independent sections in the detector. These devices make simple histograms and perform other rudimentary tests of the data, apply calibrations and do other simple housekeeping functions. The data will next be transmitted, via a high speed bus, to a mid-sized

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computer devoted to servicing an individual experiment. The machine should be at least as powerful as a VAX and capable of fully processing a significant fraction of the events as well as making detailed and complete tests of the entire experiment. It will be equipped with a full set of peripherals, including large capacity disks and 6250 BPI tape drives for recording the raw data.

One of the factors which has limited the amount of data collected by experiments has been the pain associated with handling large numbers of tapes. Assuming saturation sets in the level of 1000 tapes, in the past this corresponded to a data sample of about 1.5×10^{11} bits for tapes written at 800 BPI. This number becomes 10^{12} bits when 6250 BPI drives are used. A number of new technologies currently under development offer significantly higher storage capacity than magnetic tape. Perhaps the most promising on a short-term basis is the video disk, which will have a storage capacity 1 to 2 orders of magnitude larger than 6250 BPI tape. In addition to its obvious role as an archival medium, the video disk might eventually replace magnetic tape as the basic recording medium for raw data.

Next we consider how experiments might obtain access to a shared facility which would have the computational power of multiple CDC 7600s. An attractive way to do this is to use a local network capable of moving data at a very high rate. Network Systems Corp.

markets a product called Hypernet which offers many of the features required to construct a modular and expandable local network. Their system is based on a serial transmission bus cable that connects passively into adapters that link the bus to a number of commonly used computers. They also provide adapters for a number of high performance peripherals. Using standard coax cable, data rates of 40 megabits are possible at distances up to 1000 feet. Beyond this distance it is necessary either to use more expensive cable or decrease the data rate. Other firms are considering prospective product lines of similar capability. The flexibility inherent in organizing a system around such a bus will offer many advantages with respect to resource and load sharing.

References

1. M. Zeller, Proc. 1978 ISABELLE Summer Workshop, Brookhaven, p.319, BNL Report 50885.
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3. G. Benenson, B. Knapp and W. Sippach, Proc. 1978 ISABELLE Summer Workshop, Brookhaven, p. 371, BNL Report 50885.

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