UCRL-CR--105789

DE91 007147

FEB 06 1991

Real-Time Multi-Dimensional Processing Hardware Designs

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October 1990

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Livermore
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FINAL REPORT ON
"REAL-TIME MULTI-DIMENSIONAL PROCESSING HARDWARE DESIGNS"
RESEARCH ACTIVITIES

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Submitted to STEVE AZEVEDO
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October 31, 1990

I. INTRODUCTION

The overall goal of this project is to evaluate the potential of extremely fast hardware architectures for image processing. Primary focus is upon hardware realizations of the Radon transform and backprojection because of their applicability to computed tomography. In this report, we summarize our results from September 1989 through October 1990 in the electronic design, layout, and simulation of a new unified Radon transform and backprojection very-large-scale-integrated (VLSI) integrated circuit (IC).

The Radon transform and its inverse (a filtered backprojection) have been used in the area of image reconstruction, particularly for computed tomography (CT). However, it has more general applications in image processing and is restricted in its use by its large computational demands. Like the Fourier transform in the late 1960's, the Radon transform could possibly impact many areas if forward and inverse transforms could be computed very rapidly. Highly optimized algorithms and multi-processor hardware architectures for the forward and inverse Radon transform have been and are being studied to allow maximum improvements in computational speed. This UCD project is on the leading edge in developing such a computational "engine", a "Radon transform computer" (RTC), that could be applied to a variety of applications. Two hardware approaches to realizing the "Radon transform computer" have been designed at UCD. The first uses commercially available, general purpose digital signal processing (DSP) integrated circuits (ICs). We have constructed and tested a "Radon Transform Processor" (RTP) multi-processor board that uses TMS320C25 DSP chips. The RTP has 4 DSP chips in place and is expandable. These studies demonstrate that a multi-processor DSP chip realization of the RTC can be substantially faster than other presently available alternatives. This design is reported upon in our separately submitted "Final Report on the "RADON TRANSFORM COMPUTER" Project". A second approach is a UCD-designed fully custom CMOS VLSI IC optimized for the forward transform and back-projection calculations. The chip architecture is pipelined to allow data to enter the processor at a rate of one point per clock cycle. As fabricated in a common 1.5-micron CMOS technology, this chip will operate at estimated clock frequency between a worst-case 27 MHz and a best-case 50 MHz, allowing reconstructions at video rates.

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In both hardware designs above, we are using the Parallel Pipeline Projection Engine (PPPE) system architecture [1-3] for our high speed Radon transform computer. The PPPE architecture consists of a group of processors with 2 data distribution paths; one bus that connects all processors in parallel, and a processor-to-processor path is used to pipeline data through the processors. In computing the forward transform, each processor computes one projection of the Radon transform for one particular angle. Each processor, operating in parallel with the others, takes the input pixel, computes the appropriate bin to add the pixel value to in the transform space, performs the addition, and stores the result in local RAM. When the complete image has been processed, the Radon transform of the image is stored in local memory of the processors. For maximum processing speed, there should be one processor per projection; otherwise multiple passes of the image must be made with each processor computing the Radon transform values for different angles on the multiple passes. For handling the back projection, the PPPE architecture employs the same group of processors, each being preloaded with the Radon transform values for one particular projection angle. The image is reconstructed a pixel at a time - the value of each pixel is passed down the pipeline, with each processor adding the contribution of its projection to that pixel.

Our interests are in the high-speed reconstruction of high-resolution images from collected projection data, and the computation of the forward transform, especially for more sophisticated multiple pass algorithms. Our Radon transform computer specifications require computing the forward transform and backprojection, handling 1024 pixel by 1024 pixel images, using 720 projections over 180 degrees, using 16-bit collected data, and processing data as rapidly as possible, possibly as much as 100 times faster than existing hardware for Radon transform computations.

In an effort to achieve these goals, we focused our research activities in three areas during the 1989-90 funding period. These activities are:

1. Design, construction, and testing of a multi-processor RTP prototype board to compute the Radon transform and backprojection using four TMS320C25 DSP chips.
2. Design, simulation, and layout of a custom CMOS VLSI chip with a unified Radon transform/backprojection architecture that will be capable of at least 10MHz data rate processing of images.
3. Evaluation of the hardware requirements for high speed filtering of data to be backprojected.

In this final report, we summarize some of our results from September 1989 to October 1990. The design, construction, and testing of a four-processor prototype multi-processor (RTP) board using TI TMS320C25 DSP chips (item 1) has been completed and is reported upon in our separately submitted "Final Report on the "RADON TRANSFORM COMPUTER" Project". The design of our fully custom CMOS VLSI chip (item 2) has been completed. The chip has been designed, the layout completed, and the chip is now going through its final pre-fabrication simulations. We are now finishing the extensive detailed final documentation of the R/Bchip. This extensive documentation will be provided to Steve Azevedo when we have submitted the chip for fabrication. (Fabrication is being done at by LSI Logic, Inc., a co-sponsor of this project, at no cost to LLNL.) The present status of the custom chip design activity is summarized in Section II. Evaluations of the hardware requirements for fast filtering of data for filtered backprojection (item 3) have been completed and are summarized in our separately submitted "Final Report on the "RADON TRANSFORM COMPUTER" Project".

In the next section, we briefly summarize the new custom CMOS VLSI unified Radon transform/backprojection IC architecture, layout, and simulated performance.

II. CUSTOM CMOS VLSI UNIFIED RADON TRANSFORM/BACKPROJECTION IC

Figure 1 shows the block diagram of the new unified Radon transform/backprojection (R/B) IC. Each R/B chip contains four blocks: the address generator, the datapath, the RAM address counters, and the on-chip projection RAM. The address generator maps the Cartesian coordinates of the input image into the polar coordinates of the projection space. The datapath uses the polar coordinate to address the projection RAM in the backprojection operation and in the Radon transform. The on-chip projection RAM acts as local storage for the operation.

Figure 2 shows the block diagram of the address generator and the RAM counters. The address generator consists of sine/cosine RAMs, two accumulators, and a final adder. The sine/cosine RAMs store sine, cosine, and starting bin addresses for 32 angles. Storing this information requires two 32x27 RAMs. The angle information is read into this RAM before the reconstruction process begins. Then as one angle is selected, the sine, cosine of the angle, theta, and the values " $X0*\cos(\theta)$ " and " $Y0*\sin(\theta)$ " are read out and stored in registers. Once the reconstruction begins, these values are combined to calculate "s",

$$s = X*\cos(\theta) + Y*\sin(\theta),$$

where "X" is the horizontal Cartesian coordinate of pixel "i", "Y" is its vertical Cartesian coordinate, and "(X0, Y0)" is the starting location of the image. "s" is used for two purposes. The integer part of "s", called "bin", is used as the Radon address for the projection RAM. The fractional part of "s", called "s-bin" is used to linearly interpolate between the Radon values at adjacent addresses, "bin" and "bin+1".

The RAM address counters determine the address inputs of the odd and even RAMs. The odd and even counters permit addressing the RAMs individually, and thus doubles the operating speed.

The forward projection of a 1024x1024 12-bit image requires a RAM of 1024 words by 22 bits. This RAM was broken up into two 512x22 RAMs, one for even addresses and one for odd. The division allows the access to adjacent bin locations in one clock cycle. Each of these 512x22 RAMs consist of two 256x22 static RAMs. In the backprojection operation, the RAMs are loaded with the filtered projection data. When the backprojection begins, adjacent data points are simultaneously addressed, read out and used to calculate the contribution of the projection to the current pixel. In the forward transform calculation, the RAM acts as storage for the projection for one angle.

The main datapath calculates both the forward and the backprojection transforms using three adders and one multiplier. It uses registers to pipeline the calculation in both transforms and uses multiplexors to switch the signals properly for the two different operations. The number of adders has been reduced from five to three, and the speed has been increased since our last report. The datapath performs two similar types of calculations. In the backprojection operation it calculates the contribution of the filtered projection to the present pixel, "i(t)",

$$i(t) = i(t) + r'(\text{bin}, \theta) * [1 - (s - \text{bin})] + r'(\text{bin} + 1, \theta) * (s - \text{bin}),$$

where " $r(s, \theta)$ " denotes a filtered projection value at the location "s" of the angle, "theta". In the forward transform, the datapath uses the input pixel value and "s-bin" to find the pixel's contribution to the current "bin". This time two adjacent locations in the projection RAM need to be read, accumulated to, and written back, in one clock cycle,

$$\begin{aligned} r(\text{bin}, \theta) &= r(\text{bin}, \theta) + i(t) * [1 - (s - \text{bin})] \quad \text{and} \\ r(\text{bin} + 1, \theta) &= r(\text{bin} + 1, \theta) + i(t) * (s - \text{bin}), \end{aligned}$$

where " $r(s, \theta)$ " is the forward radon transform value at "s" at an angle "theta". Performing a read-modify-write operation of a location in a RAM is slow. However, we store the intermediate values in registers, so that this operation is not limited by the access time of the RAM.

The datapath uses a single 8x12 signed multiplier, and two 22-bit and one 12-bit signed adders to calculate both the forward transform and the backprojection. Critical path analysis indicates that the chip will operate at a maximum speed of 50 MHz, and a worst case speed of 27 MHz. The R/B chip has 125 pins and measures 10mm x 10 mm. The chip will be fabricated in a 1.5 um CMOS technology by LSI Logic, Inc. The design and verification of the R/B IC is nearly complete. The final checks on the chip should be completed in November, and prototypes ICs available by January or February.

IV. REFERENCES

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2. E. B. Hinkle, J. L. C. Sanz, and A. K. Jain, "Radon-Based Image Processing in Parallel Pipeline Architecture", Proc. SPIE 86, San Diego, CA 1986.
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Figure 2 Address Generator and RAM Counters

Figure 1: Block diagram of the datapath

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02 / 20 / 91