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Monolithic Junction Field-Effect Transistor Charge Preamplifier for Calorimetry at High Luminosity Hadron Colliders *

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Abstract

The outstanding noise and radiation hardness characteristics of epitaxial-channel junction field-effect transistors (JFET) suggest that a monolithic preamplifier based upon them may be able to meet the strict specifications for calorimetry at high luminosity colliders. Results obtained so far with a buried layer planar technology, among them an entire monolithic charge-sensitive preamplifier, are described.

I. INTRODUCTION

The present paper discusses the results achieved so far in a research and development program which aims at realising a monolithic charge-sensitive preamplifier employing epitaxial-channel JFETs.

The silicon JFET, by virtue of its good noise behaviour, its high radiation resistance and its ability to operate at cryogenic temperatures, appears to be a suitable front-end element in calorimetry applications at high luminosity colliders [1,2].

Among the existing JFET technologies, the one employing an epitaxial layer for the channel and a diffused gate still presents the best noise performances. Discrete JFETs based on this technology feature indeed the lowest amount of noise in the low-frequency region. Besides, their white noise follows rather closely the theoretically expected behaviour for the channel thermal noise. Contributions due to spreading resistances are usually negligible.

It can be, therefore, understood why the monolithic integration of epitaxial channel JFETs by a process able to retain their noise characteristics is a task worth pursuing. It is not an easy task, though, for the epitaxial channel JFET does not lend itself to a straightforward monolithic integration.

The preamplifier assumed as a target in the monolithic integration programme is described by the circuit diagram of Fig. 1 [1]. It employs only N-channel JFETs and a diode level shifter.

The circuit of Fig. 1 consists of an input cascode (J_1, J_2) with an active load (J_3, J_4) and a bootstrapping source follower J_7,

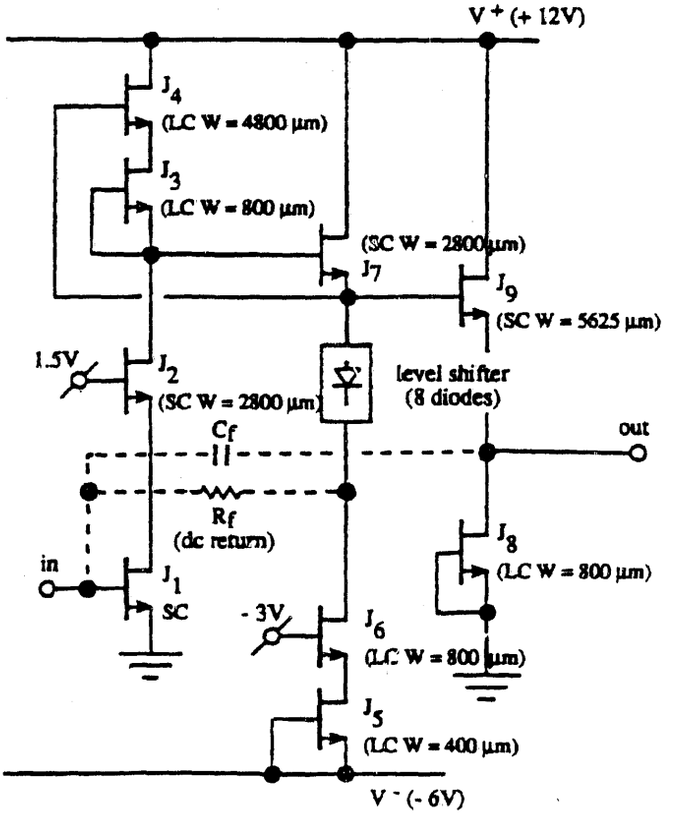

Fig. 1 Circuit diagram of the N-channel JFET charge-sensitive preamplifier.

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which serves also the purpose of buffering the high impedance point on the drain of J_2. The signal path is completed by the output source follower J_9. The feedback resistor R_f and the capacitor C_f, are not part of the monolithic chip, but rather externally added components in the present version of the preamplifier. As pointed out in [1], the JFETs on the signal path, J_1, J_2, J_7, J_9 are realised as short channel (SC) units, 5 μm gate lenght, in order to achieve an adequately large gain-bandwidth product. Instead, J_3 through J_6 and J_8, for which the requirement of a large r_{DS} is more important, are realised as long channel (LC) devices, about 7 μm gate lenght.

The monolithic integration of the circuit of Fig. 1 brings about several technological difficulties in order to retain the noise and radiation resistance characteristics that the individual JFETs would feature as discrete elements [2].

A dielectric isolation process seemed at a first glance, to provide the most suitable approach. Difficulties in the procurement of Dielectrically Isolated (DI) material meeting the specifications and featuring adequate quality prompted the development of a junction isolated process. First, a process employing deep trenches (V-grooves) for achieving interdevice isolation has been tried [2]. The low yield due to the presence of the broad and deep grooves required in monolithic JFET circuits led to the development of a fully planar process based on a buried layer junction similar to the one already in use in bipolar monolithic integration [3.4].

Regardless of the technology employed, the preamplifier is described by the the layout shown in Fig. 2.

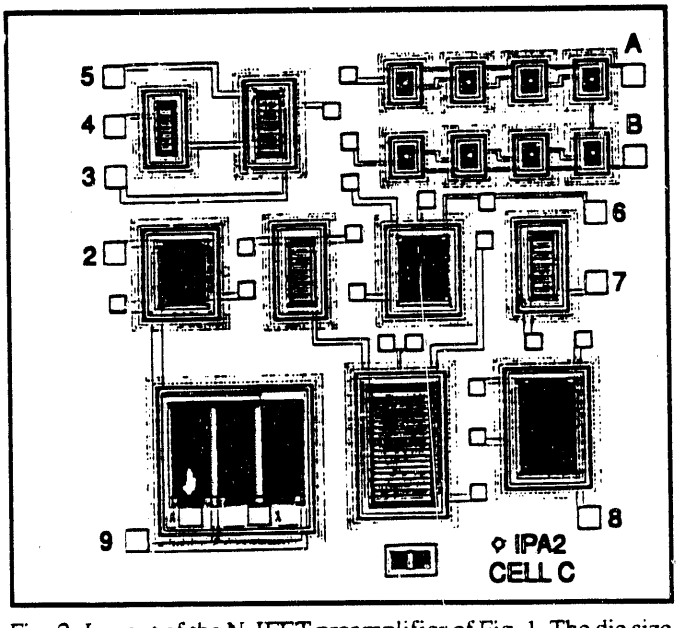

Fig. 2 Layout of the N-JFET preamplifier of Fig. 1. The die size is 3 mm x 3 mm.

II. REALISATION BASED ON THE BURIED LAYER APPROACH

The buried layer process starts from an N-type substrate into which highly doped p-type regions (buried layers) with acceptor concentrations in the 10^{19} to 10^{20} cm^{-3} range are diffused, as shown in Fig. 3.

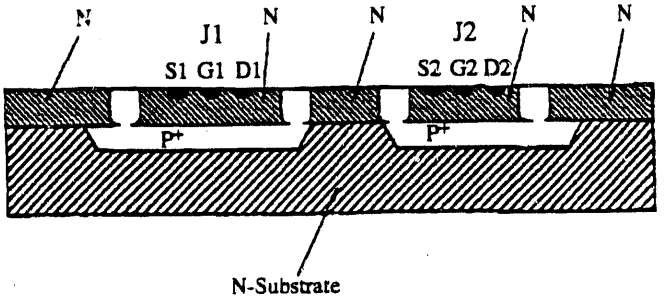

Fig. 3 Cross-section of a JFET in the buried layer process.

The buried layers define the tubs on which the JFETs are realized and, together with the vertical isolation diffusion, constitute the backside gate. An N-type epitaxial layer grown on top of the chip, provides the channel region of the JFETs.

The doping profile in the gate region of the device, before the diffusion of the topside gate is shown in Fig. 4

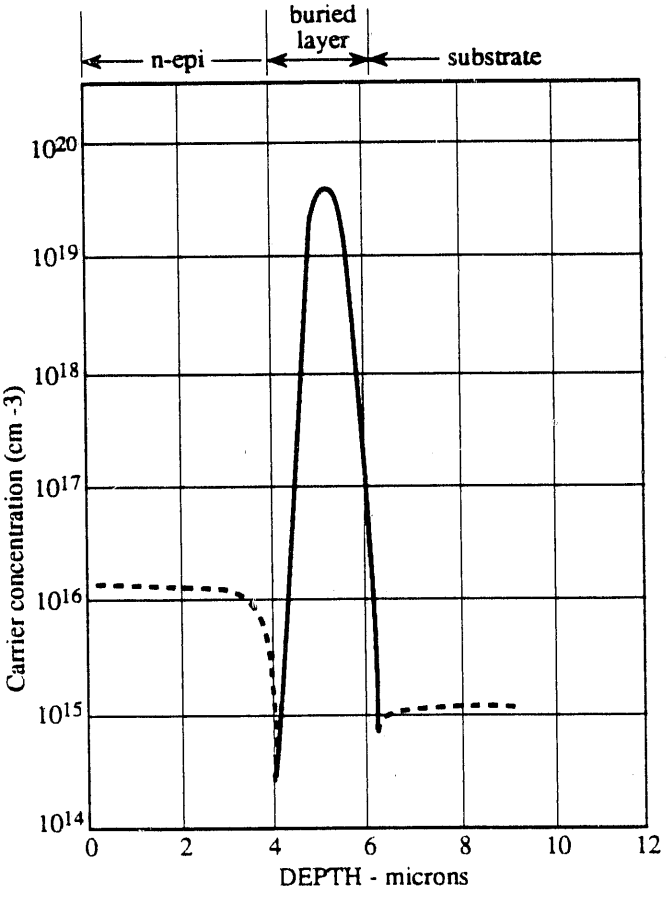

Fig. 4 Doping profile in the gate region of the device prior to the diffusion of the topside gate.

The extent to which the JFET realised on a buried layer chip approaches the transconductance characteristics of the corresponding discrete devices is shown in Fig. 5.

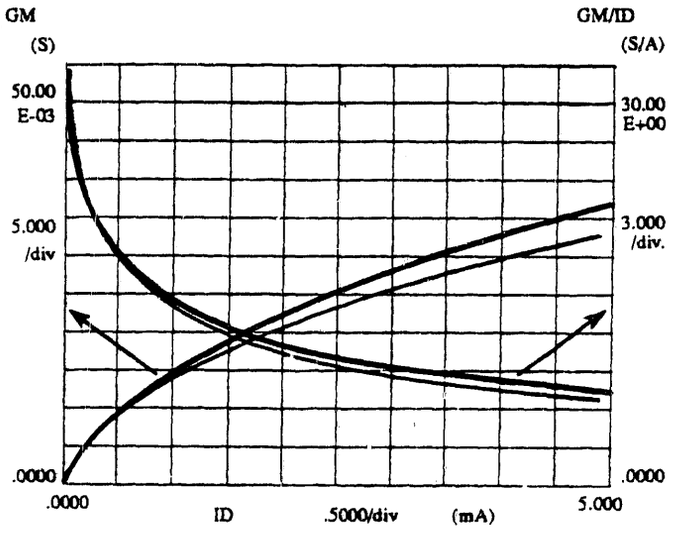

Fig. 5 Transconductance g_m and g_m/I_D ratio as functions of drain current I_D for a discrete JFET, NJ450 (thicker line) and the corresponding device, part of a monolithic chip in buried layer technology (W=11400 μm) (thinner lir).

Compared to the double epilayer, V-groove devices described in [2], the JFETs obtained as parts of a monolithic buried layer chip have a much better noise behaviour, as apparent in Fig. 6.

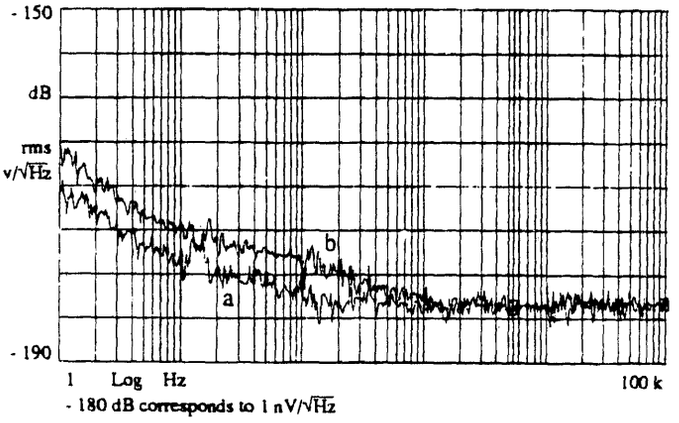

Fig. 6 Noise voltage spectra of discrete NJ450 (a) and the corresponding part (W=11400μm) on the buried layer monolithic chip (b).

The comparison is carried out in conditions of equal transconductance, 30.5 mA/V for both devices. According to Fig. 8, the device part of the monolithic buried layer chip has a noise voltage density in the white noise region which equals the value of the corresponding discrete device, thus overcoming the problem of excess thermal noise due to the spreading resistance associated with the backside gate, which was present in the devices described in [2].

Compared to the discrete unit of equal dimensions, the JFET part of the monolithic chip implemented in the buried layer technology has a somewhat higher low-frequency noise and this may be related to the fact that the growing process of the N-type epitaxial layer, which defines the channel, cannot be considered fully optimised as yet.

III. MONOLITHIC PREAMPLIFIER TEST STRUCTURE IN BURIED-LAYER TECHNOLOGY

A test structure of the monolithic preamplifier has been realised according to the buried-layer process. It differs from the circuit diagram of Fig. 1 for just one point, that is, the on-the-chip, diode-based dc level shifter has been replaced by an external resistive shifter, in order to leave the freedom of adjusting the internal voltages in the preamplifier. Besides, bonding pads have been added in some points of the circuits to allow the measurement of the standing currents in the different branches of the circuit.

The standing current in J_1, which according to the circuit diagram of Fig. 1 is determined by the I_{DSS} of J_3 was found to be larger than the expected value, about 10 mA instead of 5 mA. Such a difference, which is reflected also in a power dissipation, 290 mW, largely exceeding the design value, is related to the control of the pinch-off and I_{DSS} values, which have not yet been optimised in the buried-layer process.

At the measured current of 10 mA, J_1 has a transconductance of 48.5 mA/V.

The noise behaviour of the monolithic preamplifier is summarised in figures 7 and 8 that show results of measurements

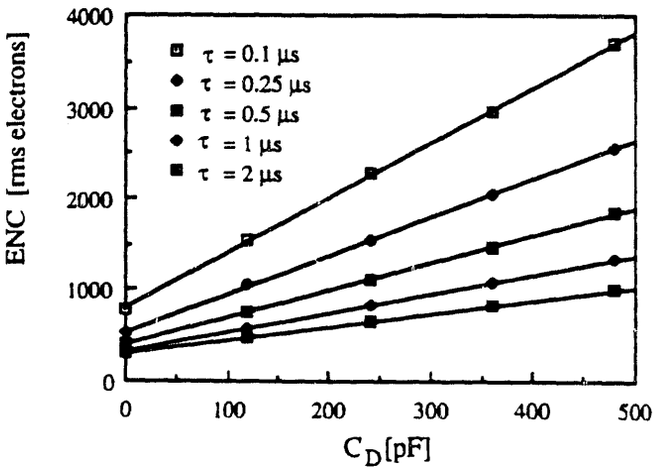

Fig. 7 Equivalent Noise Charge as a function of the time constant τ of the semigaussian filter. The peaking time in the impulse response of the preamplifier-amplifier system is 2τ. The detector simulating capacitance C_D is the parameter of the family of curves.

carried out by connecting the preamplifier to a semigaussian shaping amplifier. The equivalent noise charge ENC at five different values of the capacitance C_D simulating the detector is plotted in Fig. 7 as a function of the shaping time constant τ of the filter. At a detector capacitance of 480 pF and at a shaping time constant of 100 ns, an ENC of less than 4000 rms electrons has been measured.

The dependence of the Equivalent Noise Charge on the detector simulating capacitance C_D is shown in Fig. 8.

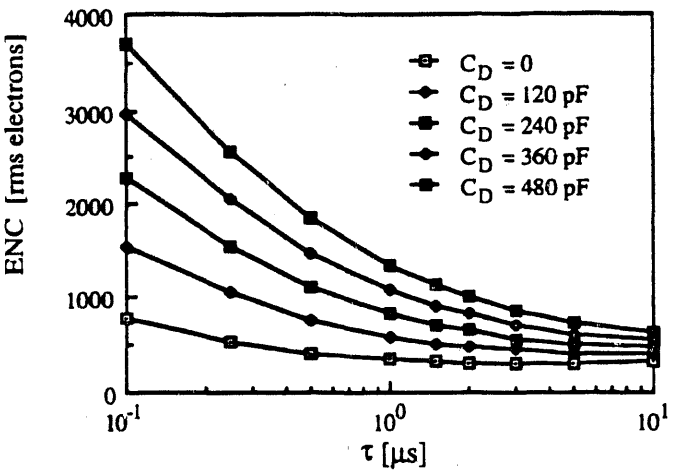

Fig. 8 Equivalent Noise Charge as a function of the detector simulating capacitance C_D. The time constant τ appears as a parameter in the family of curves.

It is interesting to compare the measured values of the capacitance sensitivity $dENC/dC_D$ obtained from Fig. 8 with the values that are expected theoretically under the assumption that the only source of noise is the channel thermal noise in J_1. Such a comparison is carried out in Table I.

Table I

τ [μs]	$dENC/dC_D$ [e/pF]	
	theorical	measured
0.1	6.34	6.25
0.25	4.01	4.21
0.5	2.83	2.95
1	2.00	2.08
1.5	1.64	1.69
2	1.42	1.46
3	1.16	1.14
5	0.89	0.86
10	0.63	0.62

As it emerges from Table I, the agreement between the measured and the calculated values of $dENC/dC_D$ is very good, so that the total noise referred to the preamplifier input is very close to the channel thermal noise of the input transistor J_1.

IV. FUTURE WORK

Optimisation of the buried layer process from the point of view of a tighter control of the pinch-off voltages must be achieved in order to increase the yield and keep the power dissipation close to the design value.

An alternative preamplifier configuration in which J_1 is implemented as a tetrode structure will also be considered. A complete characterisation of the chip for use in hadron collider calorimetry must include an evaluation of its resistance to ionising radiation and neutrons, which will be carried out as soon as packaging of a small preamplifier lot will be completed.

The present design and layout were intended to explore different technological solutions with the same set of masks. As it appears from Fig. 2, the choice of the diode string as a voltage shifter is not optimal from the point of view of the silicon real estate. A resistive voltage divider may result in a considerable area saving. Also a layout targeted to the buried layer process may exploit stricter design rules and reduce the spacing of the components allowing a further reduction of the size.

V. CONCLUSIONS

The buried layer process seems to have provided a viable approach to the design of monolithic JFET preamplifiers of outstanding noise characteristics. Tests carried out on a preamplifier employing at the input a JFET with 11400 μm gate width have demonstrated that the noise behaviour of the preamplifier is close to the one which would be expected if the total noise referred at the preamplifier input were the thermal noise in the input device, that is, the monolithic circuit approaches the noise performances of a hybrid preamplifier using discrete JFETs.

VI. ACKNOWLEDGEMENTS

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