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10/17/79

OCTOBER 1979

14. 156
PPPL-1590

UC-20b

MASTER

DIGITAL COMPUTER SIMULATION METHOD
FOR COMPLEX CONVERTER SYSTEMS

BY

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Figure 2. Frequency of use of the 100 most common words in the 100 most common sentences.

Also, multiple of four printer must be included in the bid.

[illegible]

The method described here improves the computational efficiency by an approximation which assumes successively to be independent of the overall circuit for small time increments. At each time step the output noise voltage and current are updated for all repeated subcircuit sections, extending from the source to the load.

The efficiency of the model and any other approximate method depends on the accuracy required and hence the time step increment. The method presented here has been demonstrated to produce satisfactory results at a modest computer cost for complex converter arrangements which are beyond the scope of most other simulation methods. Furthermore, the inherent flexibility of the modeling format permits easy modification of the problem and is well suited for computer application.

1. A large number of people are employed in the service sector.
 2. The service sector is growing rapidly.
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 6. The service sector is becoming more innovative.
 7. The service sector is becoming more sustainable.
 8. The service sector is becoming more responsible.
 9. The service sector is becoming more transparent.
 10. The service sector is becoming more accountable.

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There are a number of reasons why the results of the present study may not be generalizable to other populations. First, the sample was relatively small and consisted of a convenience sample of students from a single institution. Second, the study was cross-sectional and did not include a control group. Third, the study did not include a measure of social desirability bias. Fourth, the study did not include a measure of self-esteem. Finally, the study did not include a measure of social support.

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The above information was obtained from the files of the FBI, New York Office, and is being furnished to you for your information. The information was obtained from the files of the FBI, New York Office, and is being furnished to you for your information.

Below the main line of the program, the following code is used to perform the step-by-step program method for a positive directed acyclic graph of the network. When a node is "fired" and its immediate neighbors are all in the "fired" state, a particular element of the network is detected for "firing." This element is added to the "fired" set, and its immediate neighbors are checked to see if they are in the "fired" state. If so, they are added to the "fired" set.

When the value in $TIMED$ is equal to a constant n , the register value only a certain value is assigned to the register logic at General. When the value in $TIMED$ exceeds the input delay plus the desired timing jitter, the value is rejected and the amount of the rejection is small.

The thetans are represented by a series of

INDEX NOTATION:

- I = 1, 2, 3 phase
- J = 1 to J power supply units
- K = 1 to K transformers per feeder
- L = 1 to L secondaries per transformer
- M = 1, 2 (+), (-) DC pole

ABBREVIATIONS:

- CLR = current limiting reactor
- PRI = transformer primary
- SFC = transformer secondary

Figure 3 - SINGLE PHASE REPRESENTATION OF COMMON POWER SUPPLY UNIT

logic statements which control an ideal switch. Conduction occurs with the presence of positive forward voltage and the firing pulse and/or when the forward current exceeds a small value which is characteristic of the thyristors being used.

Thus, the basic building block of the program is the common power supply unit shown in Figure 3. The DC bridge terminals may be connected in series or parallel to a load or to a current source. The use of the index notation provides a convenient means of identifying branch currents and node voltages, and also allows the extension of the model to include multiples of the common unit. For example, two common power supply units can be created in the model simply by extending the range of the J index from 1 to 2. Similarly, the AC feeder configuration could be changed to include two reactor feeder branches by extending J from 1 to 2 and reducing K from 2 to 1.

The model elements $\bar{R}$, conceptually shown as resistances to ground in Figure 3 are used as references to a virtual neutral and form the basis of the method of circuit analysis.

METHOD OF CALCULATION

The introduction of the $\bar{R}$ elements facilitates the calculation method by introducing a loop around which the branch current and voltage drop may be computed for a particular branch, independent of the rest of the circuit (an approximation valid for small time increments).

Figure 4 - BRIDGE LEG REPRESENTATION

Figure 5 - VOLTAGE TRANSFORMATION

Referring to the example of Figure 3 the calculation at each time step begins with the computation of the source voltage for each phase ($I = 1, 2, 3$):

$$V_{BUS(I)} = E \cdot \sin(\omega t - (I - 1) \cdot \pi/3)$$

The differences between these three voltages and those determined during the previous time step at the J transformer terminal nodes ($I = 1$ to J where $J =$ number of power supply units in the model) serves to drive current through the current limiting reactor branches. Using the Euler approximation, and with DT equal to the time step interval:

$$\Delta ICLR(I,J) = (V_{BUS(I)} - V_T(I,J) - ICLR(I,J) \cdot RCLR) \cdot DT / LCLR$$

The currents $ICLR(I,J)$ are then updated according to:

$$ICLR(I,J) = ICLR(I,J) + \Delta ICLR(I,J)$$

The voltages $V_T(I,J)$ are next updated using the new currents $ICLR(I,J)$, the element RT , and the previous time step values of the currents $IPRI(I,J,K)$:

$$V_T(I,J) = (ICLR(I,J) - IPRI(I,J,1) - IPRI(I,J,2)) \cdot RT$$

The above equation represents the node current equations at the $V_T(I,J)$ transformer nodes. These node current sums, when non-zero, represent essentially the differences between the previous time step currents $IPRI(I,J,1)$, $IPRI(I,J,2)$ and the present time step currents $ICLR(I,J)$. These differences, applied to the elements RT , serve to update the voltages V_T which are presented as the sources to the next set of circuit branches. This computational sequence continues through the remaining circuit branches proceeding from the source to the load, and is repeated at each time step. A flow chart of the computation process is given in Figure 6.

The introduction of the R elements provides a loop around each $R-I$ branch which, when considered as an independent circuit, may be characterized by a single first order differential equation and solved by the Euler approximation. The solution or output of each branch provides the input to subsequent circuit branches. Over small time increments the approximation regarding the independence of the sub-loop from the remainder of the circuit produces a small sub-loop solution discrepancy which is compensated for by the effect of the R elements.

The accuracy, stability, and efficiency of the calculation method are influenced by the relationship between the sub-loop time constants, the R elements, and the time step interval. In general the element R for a particular loop is chosen such that $1/R$, the sub-loop time constant, is about five times the time step interval. The time step is typically chosen based upon the accuracy required versus the computer execution cost.

The load may be represented as an impedance by adding additional circuit branches as required or by specifying a particular load current. In general, short circuit studies are performed by including the DC bus or DC side reactance as the load branch whereas studies involving voltage drop and commutating angle are made by specifying a load current.

TYPICAL APPLICATION OF THE METHOD

Utilizing the index notation multiple series power supply units may be assembled in the model. Similarly, with proper division of load current, multiple parallel power supply units or parallel bridges may be assembled.

When it is desired to study the performance of parallel arrangements of phase shifted bridges, it is necessary to represent each parallel path in the model. However, certain configurations possess a symmetry which allows multiple parallel paths to be represented

Figure 6 - FLOW CHART

by a single path with appropriate adjustment of load current. For example, the converter arrangement of Figure 1 has four identical parallel paths and may be represented by one which carries 1/4 of the total load current.

As an example of a typical design study utilizing the described calculation method and computer program, the following analyses were performed for the Toroidal Field (TF) converter of the TFTR, shown in Figure 1.

Normal Operation

A study was made to predict the performance of the converter at various values of load current and with various firing angles. A simulation run was made at each operating point.

Typical results for one parallel 24 pulse path of the TF converter are shown in Figure 7 for $\alpha = 0^\circ$ and full load current.

The program is capable of printing and plotting currents and voltages as a function of time for each point in the system. In addition it calculates average DC voltage and commutating angle. In order to determine the expected harmonic content at various operating points a Fourier analysis routine may be appended to the main program to analyze the currents and/or voltages of interest.

Abnormal Operation

The program is suitable for simulating most of the common internal power supply faults such as misfire and commutation failure as well as bypass operation, firing suppression, and overload operation with commutating angle $u > 60^\circ$. This latter condition is shown with $\alpha = 0^\circ$ in Figure 8. According to our knowledge most other rectifier simulations are not able to operate in this mode.

Short Circuit Conditions

A short circuit study was made to determine the overcurrent conditions which may be expected to occur in the external AC and DC equipment as well as the internal power supply components such as thyristors and interconnecting bus work and cables.

Based upon the initial results for a "bolted" power supply fault it was determined that additional DC reactance was required to protect the equipment external to the power supply. Figure 9 shows typical short circuit scenarios with and without the DC current limiting reactor.

CONCLUSIONS

The described calculation method constitutes an effective tool for the analysis of complex converter systems. The method of formulation of the problem is extremely flexible and can be adapted to a variety of AC and DC circuit arrangements. As such, the effects of variations in the basic design of a system may be easily investigated. The computer coding required to implement the method is straightforward, and the storage requirements and typical execution times are not excessive.

The method may be applied to similar conversion systems such as those encountered in DC transmission, DC industrial power supplies, and DC magnet coil supplies for thermonuclear research.

ACKNOWLEDGMENTS

"The work described herein was performed pursuant to Princeton Plasma Physics Laboratory's Subcontract No. 258 under DOE contract No. FY-74-C-02-5073 with Princeton University."

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SECONDARY LINE CURRENT

PRIMARY LINE CURRENT

6 PULSE OUTPUT VOLTAGE

24 PULSE OUTPUT VOLTAGE

Figure 7 - TF PARAMETERS AT FULL LOAD WITH $\alpha = 0^\circ$

VOUT - 6 PULSE BRIDGE VOLTAGE

ISEC - SECONDARY LINE CURRENT

Figure 8 - OVERLOAD OPERATION WITH $\alpha > 60^\circ$

BOLTED DC FAULT

DC FAULT WITH REACTOR

Figure 9 - EFFECT OF DC SIDE CURRENT LIMITING REACTOR