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MICROPROCESSOR CONTROL AND DATA
ACQUISITION AT THE LLNL
100-MEV ACCELERATOR

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MICROPROCESSOR CONTROL AND DATA ACQUISITION AT THE LLNL 100-MeV ACCELERATOR

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Summary

A distributed microprocessor control and data acquisition network has been designed for implementation on the Lawrence Livermore National Laboratory 100 MeV electron/positron accelerator (LINAC). The system has been designed to be as transparent to the user as possible by stressing responsiveness, reliability, and relevance of data presented to the user. Implementation of the network will take place in modular fashion in three stages, so as to minimize disruption of normal operations. The first elements to be installed will be the beam transport system controls, beam position monitors, and accelerator operating status monitors. These units will reduce beam set-up time. Beam diagnostic equipment is now being designed that will be used in a second stage implementation. This stage will concentrate on determining beam parameters and allowing the user to optimize the beam for a given parameter. The final stage will be to install experimenter data acquisition equipment. The equipment will augment the presently existing data acquisition system.

The completed network will allow a more efficient operation of the LINAC, resulting in reduced experiment costs, and more controllable beam parameters, both of which are major concerns of experimenters.

Introduction

The continuing evolution of the microprocessor has made available powerful and increasingly cost effective, computer controlled data acquisition, and control systems. Experience at virtually all of the major nuclear research facilities throughout the world has shown that increased operating efficiency is achieved through the use of computer and microprocessor data acquisition and control. Described in this paper is a distributed processing network designed to acquire accelerator and experiment data and control accelerator functions on the LLNL 100 MeV electron/positron accelerator.

The accelerator, built in 1969, has been used for nuclear, atomic, and photonuclear physics. Currently, the scope of research is being expanded. Concomitant with the broadening of research scope comes the need for higher level accelerator diagnostics and control. The computer control system we have designed for use at the accelerator embodies several desirable features. The system has been designed to be as transparent to the user as possible. In this way the user "feels" the characteristic of the control process rather than the characteristic of the control system. System transparency is characterized by responsiveness, reliability, and relevance of data presented. Computer control is effected in parallel with existing control functions allowing accelerator operation without computer operation. The system is designed in modular fashion,

allowing future expansion and upgrading to be performed without interruption to normal accelerator operations. Additionally, provision for display of data at locations other than the control console is desirable and will be provided.

A block diagram of the data acquisition and control system is shown in Figure 1. The system consists of an LSI-11/2 command/control microcomputer, in combination with input and output media for user and system interface, and the subunit processors which acquire data and perform preprocessing functions as well as control functions.

Subunit Processors

The subunit processors read and process data from the various accelerator transducers, implement control functions, and perform self tests. The underlying philosophy behind the subunit processors is (1) to process as much data at the "local" level as is consistent with system responsiveness requirements and (2) achieve a high level of reliability by using common subunits for ease of repair or replacement.

Figure 2 shows the block diagram of a typical subunit processor. Each subunit assembly is dedicated to perform the I/O, memory, and processing requirements of a subset of accelerator data acquisition and control functions. Each processor can be optimized for maximum number of functions performed versus desired response times. The use of dedicated processing subunits reduces software design time and facilitates fault location, as the overall large, complex system has been broken down into more manageable subunits.

The heart of the subunit processor is an Intel** 8085 Microprocessor, an 8-bit-data, 16-bit-address with a 1.3 μ sec. basic cycle time. The address bus is broken down into two parts: A0-A9 allows addressing of 1K ($K=1024$) of memory, while A10-A15 are decoded to give a maximum of 64 memory and I/O selects. Additionally, address lines A8 and A9 are decoded to specify one of four data latches on the ADC/DAC interfaces. All I/O is memory-mapped for increased data manipulation and efficiency. I/O and memory can be interchanged to achieve an optimal dedicated system. Definition of subunit function is achieved through programming of PROMs (PROMs contain all the software necessary to operate the subunit processor in its dedicated configuration), and configuring RAM and I/O ports appropriately.

Communication with the command/control microcomputer is accomplished through a buffered UART. Data rates for input to and output from the command/control microcomputer are 19.2K baud. Data from the command/control microcomputer is loaded into

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latches on board the subunit processor, minimizing the time required for data transfers. (Additional details of operation of the communication interface are given below, in the "Command/Control Microcomputer" section.)

The ADC/DAC interfaces contain converters for input and output of analog data. Figure 3 is a block diagram of a typical interface. The ADCs are clocked with the accelerator main trigger so that each trigger pulse loads new data into the data latches. Minimum trigger pulse separation is 694 μ sec., which allows ample time for conversions. Control lines WR and RD are used to strobe data into and out of the latches while address lines A8 and A9 are used to select individual latches on the interface. Each ADC/DAC interface has two 8-bit output ports and two 8-bit input ports permitting 16-bit bidirectional data transfer.

Command/Control Microcomputer

The command/control microcomputer (CCM) reads data from, and writes data to, the subunit processors and disk unit, processes data and user input from the console keyboard or touch panel, and drives the console display and printer. The microcomputer is the LSI-11/2, a 16-bit data and address microprocessor with a 0.3 μ sec. basic machine cycle. The operating system is disk based, with RAM memory for storage of all data. External ROM and RAM can be expanded to meet system needs. User input routines are interrupt driven, giving fast response. Using the position-dependent priority structure of the LSI-11/2, inputs from the touch panel and console are given highest priority, maximizing responsiveness to user input. The touch panel is divided into major accelerator functions and commonly-exercised user functions. Actuation of a touch panel function gives the user a menu on the console. The user then exercises a menu option and the requisite action is executed. Upon completion of the task the user is informed of results and the CCM returns to normal operation. The console is used to directly access and display any of the accelerator data acquisition and control functions and to augment the touch panel controls, allowing optimization of accelerator parameters. The most recent command from either touch panel or console keyboard is displayed along with any graphics associated with the command. The display will track data as it is generated, giving a quasi-real-time display of data and accelerator status. Any system failures are immediately reported on the console display, identifying type of failure and components involved. Both console and touch panel can be fanned out to give output and limited (remote terminals will not have accelerator control ability for safety) input control at remote locations. The disk unit is used for program storage, input of accelerator initial set-up data, and storage of data acquisition system data. Hard copy output of data is obtained from matrix the printer.

The CCM communicates with the subunit processors via a serial line unit. Communication is initiated by the CCM. The CCM sends the address of the source of destination of data to the subunit processor communication data latches. The CCM then initiates an interrupt which is serviced by the subunit processor. The subunit processor performs the requisite data transfer and returns to normal service. In cases where the CCM sends data to the subunit processor, the actual data is also sent to data latches on the subunit processor. Loading the data into latches prior to interrupt request allows the subunit processor to operate at maximum efficiency. In cases where the CCM reads data from

the subunit processor, the subunit processor performs a read operation which simultaneously strobes the data into the UAR/T transmitter buffer.

The CCM is designed to avoid jamming by too much data. Data is read from the subunit processors and compared to the data from the previous cycle. If no change has occurred, the CCM jumps to the next operation. In the event that an excess of data is generated, the CCM switches modes and ignores predestinated nonpertinent data. The nonpertinent data is sampled periodically until normal data volume is attained, then the CCM returns to normal operation.

The console display allows the user to view alphanumeric data and graphic representation of accelerator parameters. While the accelerator is not very extensive physically, it is overwhelming in quantity of information. The display structures the data so that the user is not buried by volumes of irrelevant data. For this reason the display is intended to show only data closely associated with the parameter the user chooses to view. Using the touch panel, the user selects an accelerator parameter to be displayed. The required data is displayed in the central part of the display screen along with a small set of relevant data. If additional data is desired, the user requests the addition using the console keyboard. The auxiliary data is displayed on the perimeter of the display screen. Subsequent requests for auxiliary data override previous requests. The combination of touch panel, console keyboard, and display allows the user to access any accelerator parameter and display it in a manner which minimizes confusion.

The overall data acquisition and control system has been designed to make available to the operator and user, data pertinent to tuning, and maintaining peak operating performance of the LINAC. It is designed, predominately, as an operator convenience allowing, at least, an operator to sit at the console and operate the facility as if it were hard wired. Higher level control routines will also aid the operator by performing the tedious chores associated with maintaining and improving accelerator performance. When fully implemented it is expected that a greater operating efficiency can be achieved using the data acquisition and control system, resulting in a reduction of operating costs and increased system performance.

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FIG. 1 DATA ACQUISITION AND CONTROL SYSTEM BLOCK DIAGRAM

FIG. 2 TYPICAL SUBMIT PROCESSOR BLOCK DIAGRAM

FIG. 3 ADC / DAC INTERFACE BLOCK DIAGRAM