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PROCESSING OF POLY-Si ELECTRODES FOR CHARGE-COUPLED DEVICES

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A technique has been developed to fabricate poly-Si electrodes for charge-coupled devices. By controlling the microstructure of a poly-Si film, an anisotropic etchant was selected to provide essentially uniform electrode width dimensions. The electrode widths have only a 6% variation for the majority of the devices over the area of a 2 inch silicon wafer.

Charge-coupled devices (CCD's) are analog shift registers that transfer charge by potential differences along the surface or through the bulk of a doped semiconductor. Because the basis of the charge transport is the location of potential wells under adjoining electrodes, tight electrode tolerances on the order of $1\text{ }\mu\text{m}$ are required. Consequently, one of the major problems in the fabrication of poly-Si electrode CCD's is the development of multi-level overlapping conductors.

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layer in each device often has a different width dimension than the subsequent layer. This leads to poor potential well definition and thus inefficient charge coupling. This paper is, therefore, concerned with a processing technique to control the poly-Si electrode configuration over the surface of the wafer and thereby provide a greater yield of efficient CCD's.

Microstructure of CVD Si

Chemical vapor deposition (CVD) processing of poly-Si has been an area of study for many years. The method of forming a poly-Si film is generally by thermal decomposition of silane (SiH_4) as it flows over a heated substrate. The influence of the deposition conditions on the microstructure of poly-Si have been investigated (1-3).

In processing of poly-Si electrodes for CCD's, each Si layer deposited has a thickness of 0.6μ to 0.8μ . From diffracted x-ray intensity measurements, Kamins and Cass (1) have shown the crystallographic orientation of a CVD Si film as a function of thickness and temperature. Their data for a film thickness of 0.6μ is given in Figure 1. It is noted that the crystallographic orientation of a $0.6 \mu\text{m}$ Si film deposited at 900°C is mainly $\{111\}$ although a significant amount of $\{110\}$ orientation is present. However, by lowering the deposition temperature to 750°C , the orientation of the film becomes $\{110\}$ with very little $\{111\}$.

The grain size of a CVD Si film has also been examined as a function of deposition temperature. From transmission

electron microscopy studies, the grain size of Si deposited at 750°C is found to be much finer than at a deposition temperature of 900°C (1). The size of the grains are approximately 0.05 μ at 750°C and 0.1 μ at 900°C. Consequently, both the orientation and the size of the grains of a CVD Si film can be altered by the temperature of deposition. In this way, the microstructure of the film can be adjusted to optimize the etching characteristics of Si.

Etching of Poly-Si

Most of the data found in the literature on etching of Si is primarily concerned with single crystals. Kendall (4) has shown that single crystal Si can be etched to solve specific processing problems by varying the etch composition. However, in the case of poly-Si, each grain is a single crystal that is oriented differently than its neighbors. An etchant, therefore, that is used for single crystal Si may not necessarily perform adequately for poly-Si. This has been the case in earlier efforts to etch poly-Si by the standard HNO_3 -HF based systems. These etchants tend to attack poly-Si non-uniformly due to the different orientation of the grains. The reason for this is that the crystallographic planes of Si have different surface energies due to the number and location of unpaired bonds (5). As a result, the higher surface energy plane is generally the plane of fastest etching. Consequently, this leads to uneven removal of the poly-Si film, and a large variation is observed in the

device electrode width dimension across the wafer. With the addition of a subsequent poly-Si layer to be etched, it is, therefore, very difficult to obtain multi-level overlapping electrodes that have controlled dimensions.

Anisotropic etchants have been shown to have a marked dependence on the crystallographic orientation of Si (4,6,7). Kindall has shown that KOH and H_2O is an anisotropic etch in that it has an etch rate on the $\{110\}$ of Si that can be as much as 400 times faster than on the $\{111\}$. Using this etch solution, he was able to produce grooves in single crystal Si that were 0.6 μm wide and 44 μm deep.

Because of this etch rate dependence on crystallographic orientation, a study was undertaken to investigate the effect of KOH and H_2O on CVD poly-Si. It was felt that if the microstructure of the poly-Si was altered to obtain a predominantly $\{110\}$ texture, then the use of a KOH and H_2O solution would permit controlled etching. The etch rate along the 110 direction would be much faster than other directions inherent in the grain boundaries. This would permit the removal of poly-Si from unwanted areas by etching mainly in the direction normal to the surface of the wafer. The variation of the electrode width dimension for each device would, therefore, be minimal. With the next CVD poly-Si layer to be etched, control of the alignment of the overlapping electrode could then be obtained.

Anisotropic Etching

To obtain a $\{110\}$ preferred orientation, a poly-Si film of approximately 0.7 μm was deposited on an oxidized Si

wafer at a deposition temperature of 750°C. A layer of phosphorus was then deposited at 950°C using phosphorus oxychloride. A phosphorus diffusion drive to increase the conductance of the poly-Si was achieved by a heat treatment at 900°C for 10 minutes in O₂, 5 minutes in water vapor, and then again for 10 minutes in O₂. Using standard photolithography, the CCD electrode mask pattern was developed to observe the etching effect on the electrode width dimension.

Based on the etch rate of Si with temperature (8), a solution of 35 w/o KOH at a temperature of 34°C was used to etch the predominantly {110} poly-Si layer. After etching for 15 minutes, all the unwanted poly-Si was removed from the wafer. Figure 2 shows the remaining poly-Si electrode configuration after etching. The poly-Si is completely etched away from areas between the electrodes as well as the larger areas outside of the device. Scanning electron micrographs of the etched poly-Si are shown in Figure 3 and 4. The anisotropic nature of the KOH etch is readily observed in that variable line widths can be maintained with essentially right angle walls.

The ability of the KOH and H₂O solution to etch uniformly over a 2 inch Si wafer is shown in Figure 5. It is found that the electrode widths for the majority of the devices over the area of the wafer have only a 6% variation from the design dimension of 7.5 μm.

Conclusion

The etching of geometrical shapes in a poly-Si film can be accomplished by;

1. controlling the microstructure of the film by selecting a deposition temperature to obtain a preferred crystallographic orientation, and
2. using an anisotropic etchant that only attacks the preferred orientation of the grains.

By this technique, poly-Si electrodes have been successfully formed in the processing of charge-coupled devices.

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Fig. 1 Crystallographic orientation of a 0.6 μm thick CVD poly-Si film as a function of deposition temperature.

Fig. 2 A poly-Si CVD electrode pattern after etching for 15 min in a solution of 35 w/o KOH at a temperature of 34°C.

Fig. 5 Scanning electron micrograph of the edge of an etched poly-Si CVD electrode.

Fig. 5 Poly-Si electrode width variation over a 2 inch Si wafer after etching for 15 min. in a 35 w/o KOH solution of 34°C.