ELECTRICAL ENGINEERING DEPARTMENT

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RESEARCH IN REMOTE SIGNAL

TRANSMISSION ELECTRONICS

E. J. Kennedy, T. V. Blalock

J. Phelps, R. Rochelle, F. Dyer

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ABSTRACT

Research has been directed toward the evaluation of semiconductor circuits suitable for operation at temperatures of 250°C to 300°C. These circuits are to be utilized in monitoring neutron flux in a breeder reactor. Worst-case performance evaluations are made on an amplifier-discriminator circuit utilizing commercially available operational amplifier chips incorporated in a hybrid thick-film package, which is suitable for use to 250°C. Another hybrid thick-film amplifier-discriminator system was developed and tested for use to 300°C. A DC-DC converter to supply +10v and -10v for amplifier power was designed, and evaluated up to an operating temperature of 300°C. Detailed design theory equations for high temperature DC-DC converters are presented. Significant problems with ceramic capacitors utilized at 300°C were found.

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CHAPTER I

INTRODUCTION

This report covers work performed for the Oak Ridge National Laboratory (ORNL) by the University of Tennessee, Knoxville, (UTK) Electrical Engineering Department during the period from December 1978 to October 1979. The research was directed toward the use of semiconductor devices, capacitors, resistors, etc., capable of operation to a maximum temperature of 300°C for a sustained period of up to 2000 hours. The circuits are anticipated to be utilized in a system for monitoring core neutrons during the initial loading of Liquid Metal Fast Breeder Reactors (LMFBR), such as the Clinch River Breeder Reactor (CRBR). This is required to be an in-vessel system (no penetration of reactor housing), installed at the start of core loading and remaining in place in a sodium pool until the final phase of the loading sequence. The system is therefore required to have a self-contained power source, and provide wireless transmission of the neutron count to ex-vessel monitoring equipment. A sketch of the proposed system is shown in Fig. 1. The block diagram of the instrumentation is shown in Fig. 2. This system consists of an amplification block which amplifies an input pulse from the counter (typically 3 mV magnitude), processes the amplified signal through a single resistance-capacitance (RC-CR) filter, through a level discriminator, and finally produces an output 2 MHz signal from the acoustic transducer. This signal is acoustically coupled through the liquid sodium, and received by a crystal receiver outside the vessel.

The basic tasks of the project are subdivided into 5 distinct categories;

- (1) Neutron fission-counter development.
- (2) Amplifier-Discriminator development.
- (3) Ultrasonic transducer and driver.
- (4) DC-DC converter circuitry.
- (5) Power supply (energy source).

Figure 1. Proposed CRBR Initial Core-Loading Monitor.

Figure 2. Block Diagram of Initial Core-Loading Monitoring Instrumentation.

Of these 5 tasks, UTK was assigned responsibility for tasks (2) and (4), above. The remaining tasks, including final assembly and testing, are to be accomplished at ORNL.

The two UTK tasks ultimately involved three distinct phases of work to be accomplished during the duration of the first year of the contract. The first phase was to assist ORNL by bench tests and evaluation of a Hybrid Thick-Film amplifier and discriminator circuit, fabricated using commercially available dielectrically-isolated monolithic operational amplifier chips, that was capable of operation to a temperature of approximately 250°C (this circuit will hereafter be referred to as Hybrid Circuit I). The initial development of this circuit was previously accomplished by E. J. Kennedy of UTK in conjunction with J. T. DeLorenzo of ORNL, during the summer of 1978. The Hybrid Thick-Film layout of this circuit as well as circuit fabrication was accomplished at ORNL. In addition, we performed a statistical analysis of this circuit, using the PCAP program at UTK, to enable a worst-case estimation of circuit performance at 250°C to be obtained. The final testing of Hybrid Circuit I for greater than 2000 hours was done at ORNL.

The second phase of the research work was to design a second Hybrid Thick-Film amplifier-discriminator circuit for use to a maximum temperature of 300°C, and also one capable of reasonable radiation tolerance (this circuit is hereafter referred to as Hybrid Circuit II). UTK did all bench tests and evaluation of this circuit, as well as layout and fabrication of a prototypic circuit. As much long-term evaluation as possible was accomplished on this Circuit II. As for the Hybrid Circuit I, we also did a computer worst-case simulation to allow a more complete evaluation.

The second major Task to be accomplished by UTK was to explore the concept of a DC-to-DC converter, suitable for operation to 300°C for greater than 2000 hours. This circuit was to accept an input voltage (typically 5-7 volts) from

either a high-temperature battery or an isotopic power source, and provide output power to either Hybrid Circuit I or II, as well as power for the neutron detector. The power sources and the detector are to be obtained during FY 1980 by ORNL, and were not required for completion of the existing FY 1979 work. The University of Tennessee provided circuit design and bench tests for the DC-to-DC converter, as well as several hours of long-term tests.

The work performed by UTK on Hybrid Circuit I, for 250°C operation, is detailed in Chapter II. Chapter III covers research on Hybrid Circuit II, for 300°C operation. The circuit design, operation, and characteristics of a prototype DC-DC Converter, for use to 300°C, is detailed in Chapter IV. A summary of work performed, and recommendations is included in Chapter V.

CHAPTER II

AMPLIFIER CIRCUIT I FOR 250°C OPERATION

A previous design of circuitry suitable for operation to 250°C was made during the summer of 1978 by E. J. Kennedy of UTK, in conjunction with J. T. DeLorenzo of ORNL. An initial layout of the Hybrid Thick-Film circuit was done by ORNL in Fall, 1978, and subsequently evaluated at temperature.

This circuit utilized the Harris Semiconductor, Inc. dielectrically - isolated operational amplifier, HA-2625, having a 100 MHz gain - bandwidth product (80 MHz at $V_{\text{supply}} = \pm 10\text{V}$). There are two stages of gain, a third - stage of combined gain and filtering, and a fourth-stage comprising a biased-off amplifier, monostable-multivibrator configuration to obtain a combination discrimination, pulse-shaping function. A schematic of this circuit is shown in Fig. 3.

The first two amplifiers of Figure 3 have a gain of 16, and a bandwidth of approximately 5 MHz. The third amplifier has a center frequency gain of 14.7×0.3 , or 4.4, for an overall gain of 1160. The noise filter is a standard CR-RC design with $\tau = 2.5 \mu\text{sec}$, or a center-frequency of 64 kHz. To reduce the input noise and lower input leakage current of the first amplifier stage, a cascode connection using IMF5911 dual dielectrically-isolated JFETs was originally used. In addition to those capacitors shown in Fig. 3, there were 6 other (0.01 or 0.1 MFD) bypass capacitors utilized in the hybrid circuitry. All capacitors were US Capacitor Corp. monolithic chip ceramic, type X7R formulation (except C2, which was a stable NPO ceramic). The resistors were thick-film, DU-PONT 1600 Series, with $\text{TCR} < 100 \text{ ppm}/^\circ\text{C}$. This circuit was successfully operated at 250°C at ORNL for greater than 2000 hours, with the failure of only one component, a 0.1 MFD bypass capacitor. This circuit is to be reported in considerably more detail by ORNL in a later report.

Figure 3. Simplified Schematic Diagram of Amplifier Circuit I for 250°C Operation.

Worst-Case DC Analysis

Our first requirement was to evaluate the Hybrid Circuit I for worst-case dc drift characteristics. This was done using the PCAP (Princeton Circuit Analysis Program) [1] computer - aided - design program available on the UTK IBM 360-370 system. This program has available DC, AC, and Transient Analysis. A Worst Case and Sensitivity analysis is available with the DC Analysis system, while provision is available to compute the mean, standard deviation, and rms values in Transient Analysis.

The sensitivity is defined in the standard way as the per unit change in a node voltage due to a per unit small change in the parameter,

$$S_{\alpha}^{V_K} \equiv \frac{\partial \ln V_K}{\partial \ln \alpha} \approx \frac{\Delta V_K / V_{K0}}{\Delta \alpha / \alpha_0} \quad (1)$$

For worst-case solutions, it is necessary to specify maximum and minimum values of all parameters of interest, as well as the nominal value. Worst-case solutions are then computed for each element value that produces an extreme (W.C. Min and W.C. Max). A standard deviation is also calculated, with the assumptions that the specified tolerances represent ± 3 standard deviations for the parameters, and that node voltages are linear about the nominal operating point. Thus, results are generally valid only for small per unit tolerances.

Modelling and Results

The dc model for the Hybrid Circuit I was obtained from specifications on the HA 2625 op amp, and analysis of the input circuitry of the op amp at 250°C. As an example, the first-order model for one side of a typical IMF 5911 JFET is shown in Fig. 4(a), and the actual characteristics (at 250°C) are compared to the computer - modelled characteristics in Fig. 4(b). Although the computer model is in considerable error at higher currents, it is a very good representation of the actual characteristics near the operating point of the first stage (2V, 1.4ma).

(a) First-order Model for IMF5911

(b) Comparison of Model vs. Actual Characteristics

Figure 4. Example of DC Modelling of IMF5911 JFET at $250^{\circ}C$.

The combined JFET cascade and op amp circuit diagram (this is the 1st amplifier of Fig. 3) is shown in Fig. 5. The DC model utilized for this circuit is in Fig. 6, with all expected min-max variations indicated for temperature changes from 25°C to 250°C. The nominal predictions of this model at 25°C, when compared to measured DC node voltages and currents of the actual circuit, were within 5% agreement. Data on the HA2625 op amp was obtained from measured DC characteristics at 25°C, 150°C, 200°C, and 270°C, for several units. These data were obtained utilizing the Tektronix 577 Curve Tracer and 178 Linear IC Test Fixture. The worst-case and sensitivity analysis was performed for a possible $\pm 10\%$ deviation in all JFET parameters, $\pm 5\%$ resistor changes, large differences in the op amp input currents ($\pm 20 \mu\text{a}$), open - loop gain (10K to 100K), offset voltages ($\pm 7\text{mv}$), PSRR and CMRR values. In addition, it was assumed that the power supply value could be within a $\pm 8\text{V}$ to $\pm 12\text{V}$ range. The results of the analysis are indicated in Table I. The parameter values causing the most problem were possible mis-matches between the IMF 5911 transistors. For this reason (and also to reduce the number of wire-bonds) in the final design for Hybrid Circuit I, the input JFET was removed and the first stage op amp input connected directly to the 20K input resistor (Mod. 3 of Table I). This does produce a slight increase in the noise at 250°C.

With the best circuit now available, the remaining two op amp stages were modelled by their worst-case anticipated changes and the worst-case dc analysis for the complete final circuit of Hybrid Circuit I was obtained. All coupling capacitors were modelled by their nominal leakage resistance at 250°C. The results are indicated in Table II. It is apparent that each amplifier stage is well within its linear range for all worst-case predictions.

Figure 5. Input Stage of Hybrid Circuit I.

Figure 6. PCAP Model of Figure 5 for DC, Worst Case, and Sensitivity Analysis.

TABLE I

Worst-Case Predictions For the First Stage of Hybrid Circuit I
(250°C Operation)

Parameter	Basic Circuit(Fig. 5)	Mod. 1	Mod. 2	Mod. 3 (Final)
Max. output DC voltage	+19V	+16.5V	+0.95V	+0.81V
Min. output DC voltage	-16V	-13.6V	-0.92V	-0.80V
1 σ std. dev.	1.00V	2.18V	0.14V	0.19V
Nominal output DC voltage	+0.44V	+0.45V	+0.007V	+0.0001v
Results	Output Saturated	Output Saturated	Good linear operation	Good Linear operation

Mod. 1 is the circuit of Figure 5, but removing the cascode transistors Q2A-Q2B.

Mod. 2 is the circuit of Mod. 1, but the circuit has a DC closed-loop gain of unity, with a 0.1 MFD capacitor in series with R_2 to ground.

Mod. 3 is the circuit of Figure 5, but both JFET stages (Q1-Q2) were removed, and the op-amp connected directly to the 20K resistor (R_1 of Fig. 5). Resistor R_2 is in series with a 0.1 MFD capacitor to ground. This is the final design for the first stage.

TABLE II

Worst-Case Predictions For Final Design, Hybrid Circuit I
(250°C operation)

Parameter	1st Amp	2nd Amp	3rd Amp
Max. output DC voltage	+0.81V	+2.2V	+0.57V
Min. output DC voltage	-0.80V	-1.6V	-0.64V
1 σ std. dev.	0.19V	+0.54V	+0.20V
Nominal output DC voltage	0.0001V	+0.013V	-0.012V

Pulse Response Predictions

The Hybrid Circuit I was also computer modelled for prediction of operating gain and transient response at both 25°C and 250°C, assuming an input signal from the neutron detector of -3mV amplitude, with 0.5μsec rise-time. The models utilized typical characteristics of the op-amps at 25°C, and extrapolated performance data for 250°C operation. The computer predicted responses are shown in Fig. 7, for a filter time-constant of 2.5μsec, and for an operating temperature of 250°C. The differences between predicted responses at 25°C and at 250°C was within 5%. The actual measured response on the constructed Hybrid Circuit I could not be exactly correlated with the theoretical curves, because the constructed circuit utilized a 2μsec filter time-constant, and an increased gain for the third stage.

At the present time, the constructed circuit at ORNL has accumulated over 2000 hours of operation with no significant changes in pulse gain or waveform aberrations observable. The only failure has been one 0.10 MFD bypass capacitor. More extensive data on the actual circuit is to be presented by ORNL in a later report.

A Gaussian Filter Implementation of Circuit I

We were asked by ORNL to investigate the possibility of a Gaussian filter implementation, instead of the existing RC-CR filter currently in use with the Hybrid Circuit I. Theoretically, a Gaussian filter has the distribution

$$F(s) = \left(\frac{s}{s+c}\right)\left(\frac{1}{s+c}\right)^m, \quad (m \rightarrow \infty) \quad (2)$$

where c = fundamental filter time constant. Utilizing the present three Op Amps we were able to implement the above equation with an $m = 5$ approximation. Two different circuits were evaluated, and the best choice is

(a)

(b)

Figure 7. Computer Predicted Response of Hybrid Circuit I at 250°C .

(c)

(d)

Figure 7. (continued)

shown in Figure 8, for $\tau = 1$ microsecond. A comparison of this circuit with the presently utilized Hybrid TF Op Amp Circuit I indicates the Gaussian filter requires 2 more resistors and 3 more capacitors. Also, the forward gain is reduced considerably due to the presence of the four additional poles. The Gaussian filter was evaluated by computer model, and also breadboard tested. The breadboard results were within 1% of the theoretical computer predictions. The computer predicted output is shown in Figure 9, for an overall pulse gain of approximately 330. Since this design requires additional components, and has a reduced gain, it should only be used where an improvement in signal to noise ratio is required.

Figure 8. Gaussian Filter Approximation.

Figure 9. Computer Predicted Output of Op Amp 3
For Circuit I In a Gaussian Filter Approximation.

CHAPTER III

HYBRID CIRCUIT II FOR 300°C OPERATION

The operational amplifier Circuit I was limited in operation to about 260°C maximum. Hence, to reach an operating temperature of 300°C, it was necessary to design a separate amplifier, utilizing discrete devices and a hybrid thick-film construction. Since there would be considerably more wire-bond connections than in the op amp circuit, the number of amplification stages was reduced from 3 to 2. This required more gain per stage, and therefore a much larger gain-bandwidth product than the 100 MHz (typically, 80 MHz at $V_s = \pm 10V$) value of the HA-2625 unit. The basic circuit design concept is illustrated in Fig. 10. The optimum filter time-constant was, in experimental work at ORNL utilizing Hybrid Circuit I, found to be equal to approximately 1 μ sec.

Amplifier Circuit II Design

The original basic design constraints were to utilize as few discrete semiconductor devices as possible (thereby minimizing the number of wire-bond connections), as few capacitors as possible, as low a quiescent current as possible, the maximum number of N-channel junction field-effect transistors (JFETs) as compared to bipolar transistors [this was important, since earlier tests had verified that N-channel JFETs operate easily to above 300°C, whereas bipolars and diodes are usually poor beyond 250°C because of dominance of electron-hole reverse junction bias currents], and as large a stable gain-bandwidth product as could be achieved.

After many different circuit evaluations, the circuit of Fig. 11 was deemed most appropriate for the above constraints.

Hybrid Construction. A hybrid thick film version of this circuit was constructed on a 1 in. x 1 in. ceramic substrate. Only one circuit layout was required,

Figure 10. Basic Concept For Hybrid Circuit II.

Figure 11. Schematic of Hybrid Circuit II. Q1 = IMF5911, Q2 = 2N4861, Q3 = Process 55 (NSC), Q4 = IT137, Q5 = IT127, Q6 = 2N4861.

since Amplifier A of Fig. 10 was obtained by utilizing resistor values indicated in Fig. 11, with the signal applied to the input through a 50 pF capacitor; amplifier B of Fig. 10 was obtained with resistor R1 (of Fig. 11) trimmed to 10K-ohms, R4 to 10K-ohms, R3 to 160-ohms, C5 was a 100 pF chip capacitor, and the signal from amplifier A coupled to amplifier B through a 100 pF chip capacitor. Also, for amplifier B the output drive current capability was increased by trimming resistor R9 of Fig. 11 to 400-ohms. A sketch of the hybrid layout for the amplifier is shown in Fig. 12.

Amplifier Characteristics. A computer verification of the frequency response of Circuit II was made. At 25°C the gain-bandwidth product was 250 MHz for each amplifier, while the total current drain for both amplifiers A and B was 8.4 mA (this compares with 80 MHz and 11 mA for the op amp Circuit I). The pulse response was modelled using 300°C parameters. The computer predicted pulse response, at the output of amplifier B, is shown in Fig. 13 for an input pulse from the detector of + 0.003 v, with a 0.5μsec rise-time, and for a filter time-constant of 2.2μsec. This compares well with the response prediction for the op amp Circuit I, of Fig. 7(d), for 250°C.

At 300°C the gain-bandwidth product of each amplifier decreases 30% due to a decrease of the transconductance (gm) of the input JFET (Q2 of Fig. 11).

Worst-Case DC Analysis. A worst-case dc analysis of the Circuit II, Fig. 11 for operation from 25°C to 300°C, gave a computer predicted maximum output dc voltage of +5.35v, a minimum value of -5.63v, and a nominal dc output voltage of -0.04v. The 1-σ standard deviation was 0.59 volts. These values assumed all JFET and Bipolar parameters could deviate by ±10%, all resistors by ±5%, and the power supply voltages could vary from ±8v to ±12v. This is a rather large deviation in the output voltage, but still linear operation of the amplifier would result.

Figure 12. Hybrid Thick-Film II Layout For Amplifier A or Amplifier B. Substrate dimensions are 1 in. x 1 in.

Figure 13. Computer Predictions for Output Pulse of Amplifier B, Circuit II, at 300°C . Detector Input is +3mV, 0.5 μsec Rise-Time.

Noise Analysis. An analysis of the noise characteristics for input Amplifier A was made, at 25°C . A computer plot of the anticipated output noise of Amplifier A is shown in Fig. 14, for input resistors of 20K-ohms and 40K-ohms. The noise is basically, at 25°C , due entirely to the thermal noise of the input resistor. At 300°C , the noise is due to the thermal noise of the input resistor plus the shot noise of the gate current of Q2.

Amplifier Circuit II Experimental Results. There were 4 hybrid thick-film circuits constructed, two of Amplifier A and two of Amplifier B. The first unit of Amplifier A was evaluated at various temperatures from 25°C to a maximum test oven limit of 330°C . The output pulse response of Amplifier A at 25°C , 301°C , and 333°C is indicated in Fig. 15 for an input signal (coupled through 47 pF) of +3 mv. The ringing observed in the photographs is due to the long lines coupling in-and-out signals and power supply leads. Figure 16 shows test results of gain changes, changes in the output dc voltage and dc current over the temperature range from 25°C to 330°C , for the first unit of Amplifier A.

The first unit of Amplifier B saturated at 252°C , due primarily to an unusually high pinchoff voltage on transistor Q1A (Fig. 11), which caused a reduction in the overall dc loop gain, resulting in erratic output dc voltage drift.

Both of the first units A and B were constructed with a mistake in the layout (Fig. 12). In the second two units constructed, this mistake was corrected by cutting through two conductors and wire-bonding leads between two points. Tests on these latter two units are described later.

Discriminator Design

The combination comparator - monostable multivibrator circuit used for discrimination purposes is shown in Fig. 17. The comparator level is furnished by a negative voltage ($-V_{\text{REF}}$) applied to the input transistor Q1A. When the input signal from Amplifier B reaches a level of $+ [V_{\text{REF}} + |V_{\text{BE}}(\text{Q1A})|]$, then Q1A

Figure 14. Theoretical Output Noise for Circuit II, Amplifier A, at 25°C.

(a) $T = 25^{\circ}\text{C}$

(b) $T = 301^{\circ}\text{C}$

(c) $T = 333^{\circ}\text{C}$

Figure 15. Output Pulse Response of Amplifier A at Three Temperatures. Scale = $0.5\mu\text{sec/div}$, 50 mv/div .

(a)

(b)

Figure 16. Test Results of Amplifier A for Hybrid Circuit II.

Figure 17. Discriminator Circuit for Amplifier Circuit II.

Q1 = 2N4044, Q2 = 2N4044, Q3 = 2N4416, Q4 = IT137, Q5 = 2N3563.

conducts, which provides base turn-on current to Q4B, and an output positive feedback loop is established. The output pulse width of the signal to Q5 is determined by the charge removal from capacitor C2, and therefore basically the time constant $R4C2$ controls the pulse width. Transistor Q1B compensates the temperature characteristic of Q1A, while Q4A similarly compensates the turn-on of Q4B with temperature. The circuit is ultimately limited above 300°C operation by the h_{FE} multiplication of I_{CBO} of Q4B, which causes Q5 to turn-on.

The nice feature of this comparator is that no current is required from V^+ until an input pulse exceeds the trigger level established by V_{REF} .

The Hybrid Thick-Film layout for the comparator is shown in Fig. 18. This circuit was constructed utilizing DU-PONT type 9910 gold conductor ink and type 1600 resistor ink.

Experimental Results. The experimental output pulse response of the comparator at 25°C and 300°C is shown in Fig. 19. The output pulse width increased from 8.2 μ sec at 25°C to 12 μ sec at 300°C. The change in input discriminator threshold voltage at 25°C and 300°C is shown in Fig. 20. The 0.05V change amounts to a + 1% change in full-scale value.

Results of Long-Term Tests For Amplifier - Discriminator System.

The complete amplifier-comparator system consisting of Amplifier A, Amplifier B, and a comparator were attached to a 3 3/4" x 4 1/2" ceramic substrate, with wires connected for input, output of each stage, and power supply connections, and put on long-term test at 300°C. A photograph of the system is shown in Fig. 21. An input + 3 mv pulse was applied through 47 pF (this simulates the input from the neutron detector), and output pulse gains and comparator signal observed. All output dc voltages and power supply currents were monitored during the test. After 39 hours, the 0.01 MFD capacitor on the negative power supply shorted on the B amplifier (C6 in Fig. 11). This capacitor was replaced and tests continued until at 164 hours of operation, the 0.01 MFD

Figure 18. Hybrid Thick-Film Layout for Comparator Circuit. Substrate Size is 1" by 1".

(a) 25°C, upper = output pulse, 5v/div, 2 μ sec/div.

(b) 300°C, upper = output pulse, 5v/div, 2 μ sec/div.

Figure 19. Output Pulse Response of Comparator Circuit at 25°C and 300°C. The Lower Trace is the Applied Input Pulse.

Figure 20. Threshold Voltage of Comparator Input as a Function of Temperature.

bypass capacitor (C5 in Fig. 17) became essentially shorted. Again, the capacitor was replaced, and tests continued. At approximately 170 hours, it was found that two other 0.01 MFD bypass capacitors had shorted. These were replaced, but after 182 hours of operation a long aluminum wire-bond on Amplifier A was pulled apart by cracking and shrinkage in the high-temperature silicone encapsulant that was utilized to protect the semiconductor devices. A photograph of the problem area is shown in Fig. 22(a). Also shown in this same figure is an observed silver migration between the PA-AG conductors underneath the silicone encapsulant. Since final circuits are to be constructed utilizing gold conductors, this latter problem is of no consequence. As an illustration, the photograph of the comparator circuit after 182 hours [in Fig. 22(b)] indicates no migration, since this latter circuit was constructed with gold ink for conductors.

One significant outcome of the test of the complete Amplifier II system at 300°C was the discovery that the power supply rejection of the amplifiers was very poor at the frequency of the DC-DC Converter (~ 100 kHz). In fact, with 100 mv (100 kHz) ripple on the V^+ supply, the observed output on amplifier A was >150 mv; since the gain of Amplifier A is 55, for a 3 mV anticipated input signal the output would be 165 mv. Hence, the signal would have essentially the same amplitude as the disturbance due to the power supply ripple.

A PCAP analysis was performed to verify the observed results. A graph of the gain from V^+ to the output, and from V^- to the output, as a function of frequency at 300°C is shown in Figs. 23 and 24, respectively. Although the power supply rejection for ripple on the negative supply is satisfactory, the positive supply ripple (gain) has a peak of 9 db at 100 kHz. This would correspond to an output voltage for amplifier A of 280 mv, for a 100 mv ripple on the positive supply.

Figure 21. Photograph of Complete Amplifier - Comparator System for 300°C Tests.

(a) Amplifier A. (A) indicates wire break,
(B) indicates area of silver migration. X15 scale.

(b) Comparator Circuit, gold metalization, X15 scale.

Figure 22 Photograph of Amplifier II Test Circuit
After 182 Hours at 300°C.

Figure 23. Computer Predicted Gain From Positive Power Supply To The Output, for Amplifier II, at 300°C.

PLOT OF DB G(20, 15), SF = 10**(0), VERSUS FREQ

Figure 24. Computer Predicted Gain From Negative Power Supply
to the Output, for Amplifier II, at 300°C.

CHAPTER IV

DC-DC CONVERTER DEVELOPMENT FOR 300°C OPERATION

I. INTRODUCTION

The general goal of the dc-dc converter task was to explore the concept of a dc-dc converter suitable for operation at 300°C for greater than 2000 hours and fed by a 5 to 7 volt battery. The detailed goals of the task were the following:

- (1) exploratory investigations of materials and semiconductors for operation at 300°C and at frequencies in the range 10kHz to 100kHz,
- (2) initial circuit design,
- (3) purchase of suitable devices, wire, cores, resistors, and capacitors for evaluation,
- (4) breadboard testing at 25°C,
- (5) design modifications,
- (6) long term testing at 300°C, and
- (7) computer statistical analysis for worst-case estimations.

Characteristics of candidate semiconductor devices (diodes, bipolar transistors, JFETs, MOSFET, and VMOS transistors) were measured at 25°C, 250°C and 300°C. Devices for use in a dc-dc converter were selected on the basis of the measurement results. A survey of core materials and high temperature testing led to the selection of a high-permeability silicon-steel toroidal tape core with a Curie temperature of 730°C for use in the switching regulator. A high temperature enameled wire was used to construct the coils for the breadboard tests; however, since tests showed that the enamel slowly deteriorates at 300°C, an aluminum oxide coated aluminum wire suitable for use to about 600°C has been obtained and will be investigated for use in the coil fabrication in a continuation of this work.

Several dc-dc converter circuits were studied and the configuration selected for further development consisted of an astable multivibrator driving a VMOS switch in a dual-coil switching regulator. This configuration initially used a Siliconix VMOS VM33Ak transistor, and evolved into the converter of Fig. 25 with the help of optimization analysis and experimental evaluation. A typical procedure was to stress the converter over the entire temperature range (25°C to 300°C) to identify problem areas which were addressed by design modifications.

The design theory for the dc-dc converter of Fig. 25 is developed in Section II of this chapter. Section III presents some important considerations in the implementation of the converter. The experimental results obtained from cycling the converter breadboard over the temperature range of 25°C to 300°C are given in Section IV.

II. DESIGN THEORY

The analysis of the dc-dc converter of Fig. 25 will be performed in three parts: first, the design equations for the switching regulator will be derived; second, the multivibrator clock and error amplifier section will be analyzed; and third, the complete converter system will be studied using the results of the first and second parts of the analysis.

Switching Regulator

The switching regulator section of the dc-dc converter of Fig. 25 consists of the circuit between the gate of the Q5 VMOS transistor and the dc output voltages V_O^- and V_O^+ . This section will be analyzed by using the basic describing differential equations to find the inductor currents, the regulator duty cycle, the regulator transfer characteristics, and the load ripple voltages.

Basic Describing Equations. In the model of Fig. 26, energy is stored in the magnetic field of the core by establishing a current $i_1 = i$ in inductor L_1 during time T_1 . The current in L_2 is zero during T_1 because of the rectifier diode. During the switch off-time T_2 , the stored energy less inductor losses is transferred to the load and filter components. In the following analysis it will be assumed that the frequency and the inductance value are sufficiently high so that the inductor current never decreases to zero during time T_2 .

For the case of small coil losses, the operation of the regulator can be described approximately by the following differential equations:

$$(0 < t < T_1) \quad V_B' = L_1 \frac{di}{dt}, \quad (1)$$

$$(0 < t < T_1) \quad i_2 = 0, \quad (2)$$

$$(T_1 < t < T_2) \quad V_O^- + V_D + L_2 \frac{di_2}{dt} + M \frac{di_1}{dt} = 0, \quad (3)$$

Fig. 25. Complete DC-DC Converter System

Fig. 26. Basic Switching Regulator,

$$(T_1 < t < T_2) \quad V_0^+ + V_D + M \frac{di_2}{dt} + L_1 \frac{di_1}{dt} = 0, \quad (4)$$

where $V_B' = V_B - V_s$.

Solving Eqs. (1), (2), (3), and (4) for the case $V_0^- + V_D$ and $V_0^+ + V_D$ nearly constant over one switching period ($T_1 + T_2 = T$) gives

$$(T_1 < t < T_2), \quad i_1 = \left\{ \left[\frac{(V_0^- + V_D) M - (V_0^+ + V_D) L_2}{L_1 L_2 - M^2} \right] (t - T_1) + I_{m1} \right\} U(t - T_1), \quad (5)$$

$$(T_1 < t < T_2), \quad i_2 = \left\{ \left[\frac{(V_0^+ + V_D) M - (V_0^- + V_D) L_1}{L_1 L_2 - M^2} \right] (t - T_1) + I_{m2} \right\} U(t - T_1), \quad (6)$$

$$(0 < t < T_1), \quad i = \left[\frac{V_B'}{L_1} t + I_m \right] U(t), \quad (7)$$

where the first terms on the right side are transient currents, and the second terms are constant currents during the indicated time periods.

In the limit as the coils become identical and as the coefficient of coupling approaches unity ($L_1 L_2 = M^2$), then $V_0^+ \rightarrow V_0^- \rightarrow V_0$, $L_1 \rightarrow L_2 \rightarrow L$, and $M^2 \rightarrow L_1 L_2$, and the currents become

$$(T_1 < t < T_2) \quad i_1 = \left[- \frac{(V_0 + V_D)}{2L} (t - T_1) + I_{m1} \right] U(t - T_1) \quad (8)$$

$$(T_1 < t < T_2) \quad i_2 = \left[- \frac{(V_0 + V_D)}{2L} (t - T_1) + I_{m2} \right] U(t - T_1) \quad (9)$$

$$(0 < t < T_1) \quad i = \left[\frac{V_B'}{L} t + I_m \right] U(t) \quad (10)$$

The duty cycle is defined as

$$D = \frac{T_1}{T}, \quad (11)$$

$$\text{where } T = T_1 + T_2. \quad (12)$$

Using Eq. (11) and the fact that the frequency of switching is $f = 1/T$, the maximum values of the inductor transient currents can be expressed as

$$\Delta I = \frac{V_B}{Lf} D, \quad (13)$$

$$\Delta I_1 = \frac{V_o + V_b}{2Lf} (1-D), \quad (14)$$

$$\Delta I_2 = \frac{V_o + V_b}{2Lf} (1-D). \quad (15)$$

The power relationships are

$$P_{in} = (I_m + \frac{\Delta I}{2}) V_B D \quad (16)$$

$$P_s = (I_m + \frac{\Delta I}{2}) V_s D \quad (17)$$

$$P_D = [I_{m1} + \frac{\Delta I_1}{2} + I_{m2} + \frac{\Delta I_2}{2}] V_D (1-D) \quad (18)$$

$$P_o = [I_{m1} + \frac{\Delta I_1}{2} + I_{m2} + \frac{\Delta I_2}{2}] V_o (1-D). \quad (19)$$

The average output currents can be expressed in terms of the output voltages and the load resistors:

$$\frac{V_o}{R_{L1}} = \frac{T_2}{T} (I_{m1} + \frac{\Delta I_1}{2}), \quad (20)$$

$$\frac{V_o}{R_{L2}} = \frac{T_2}{T_1} \left(I_{m2} + \frac{\Delta I_2}{2} \right). \quad (21)$$

The remaining basic relationship is the energy balance equation which relates the currents in L_1 and L_2 at the boundary between time T_1^- and T_1^+ . This boundary condition is found by setting the stored magnetic energy in the regulator coil core at T_1^- equal to the value at T_1^+ ; thus,

$$\begin{aligned} \frac{1}{2} L (\Delta I + I_m)^2 &= \frac{1}{2} L (\Delta I_o + I_{m1})^2 + \frac{1}{2} L (\Delta I_o + I_{m2})^2 \\ &+ L (\Delta I_o + I_{m1})(I_{m2} + \Delta I_o), \end{aligned} \quad (22)$$

where, as before, it is assumed that the coils L_1 and L_2 ($\Delta I_1 = \Delta I_2 = \Delta I_o$) are identical and the coefficient of coupling is unity. Solution of Eq. (22) leads to the following relationship among the currents:

$$\Delta I + I_m = 2\Delta I_o + I_{m1} + I_{m2} \quad (23)$$

Inductor Constant Currents. The constant currents that flow in each inductor during periods T_1 and T_2 can be found from Eqs. (11), (12), (13), (14), (15), (20), (21), and (23):

$$I_{m1} = \frac{V_o}{R_{L1}(1-D)} - \frac{(V_o + V_D)(1-D)}{4fL} \quad (24)$$

$$I_{m2} = \frac{V_o}{R_{L2}(1-D)} - \frac{(V_o + V_D)(1-D)}{4fL} \quad (25)$$

$$I_m = \frac{V_o}{(1-D)} \left[\frac{1}{R_{L1}} + \frac{1}{R_{L2}} \right] - \frac{V_D D}{2fL} \quad (26)$$

Duty Cycle. The duty cycle expression in terms of voltage values can be found by first setting the power into the coil ($P_{in} - P_s$) equal to the power out of the coil ($P_D + P_o$) from Eqs. (16), (17), (18), and (19). Thus,

$$(I_m + \frac{\Delta I}{2}) V_B' D = (V_o + V_D)(1-D) [I_{m1} + I_{m2} + \Delta I_o]. \quad (27)$$

Again it should be noted that the coil losses are neglected. The saturation resistance loss and the rectifier losses, however, are included approximately through V_s and V_D .

Substituting for the currents in Eq. (27) using Eqs. (13), (14), (15), (24), (25), and (26), and solving for the duty cycle yields

$$D = \frac{V_o + V_D}{V_B' + V_o + V_D}. \quad (28)$$

Transfer Characteristic. The small signal transfer characteristic of the regulator can be found by solving Eq. (28) for V_o and then computing the derivative dV_o/dD :

$$V_o = \frac{D}{1-D} V_B' - V_D, \quad (29)$$

$$\frac{dV_o}{dD} = \frac{V_B'}{(1-D)^2} = \frac{(V_o + V_D + V_B')^2}{V_B}. \quad (30)$$

For large signal analysis, Eq. (29) can be used to determine the transfer $\Delta V_o/\Delta D$ while the derivative expressed by Eq. (30) can be used for the small signals.

Output Ripple Analysis. The output ripple can be estimated from an analysis of the circuit model of Fig. 27 which represents the coil as a current source and the filter by a simple RC low-pass network. The current model for the coil is justified if the output voltage percentage change is small during the time T_2 . The ripple voltage calculated for the simple RC filter will be higher than for the actual LCR filter and will, therefore, be a worse-case estimate produced by reasonably tractable mathematics.

The analysis will proceed by first performing a transient analysis for the circuit of Fig. 27 (a) which will result in an expression for $V(t)$ in period T_2 in terms of V_i and V_f . A similar analysis will then be done for the Fig. 27 (b) circuit which will find $V(t)$ in period T_1 also as a function of V_i and V_f . Next, the two solutions will be combined to give the ripple voltage $\Delta V = V_f - V_i$.

In the time interval T_2 , the output voltage is given in the s - domain by

$$V_o(s) = \frac{V_i}{s} + \left[\frac{I(s) R - \frac{V_i}{Cs}}{R + \frac{1}{Cs}} \right] \frac{1}{Cs}, \quad (31)$$

where

$$I(s) = \frac{I_{m1} + \Delta I_1}{s} - \frac{\Delta I_1}{T_2} \frac{1}{s^2}, \quad (32)$$

which comes from Eqs. (8) and (14) rewritten in the time domain for the Fig. 27 (a) circuit with a shift in time reference to give

$$i_1(t) = [I_{mi} + \Delta I_1 (1 - \frac{t}{T_2})] U(t). \quad (33)$$

Substituting Eq. (32) into (31) and applying the Laplace transform inversion operation gives in interval T_2

$$v(t) = V_i e^{-\frac{t}{\tau}} + R (I_{m1} + \Delta I_1) (1 - e^{-\frac{t}{\tau}}) - \frac{R \Delta I_1}{T_2} \tau \left[e^{-\frac{t}{\tau}} + \frac{t}{\tau} - 1 \right], \quad (34)$$

where $\tau = RC$.

In the time interval T_1 , the output voltage is given by a simple exponential decay:

$$v(t) = V_f e^{-\frac{t}{\tau}}. \quad (35)$$

Now putting $t = T_2$ in Eq. (34) gives the value $v(T_2) = V_f$. Likewise setting $t = T_1$ in Eq. (35) gives $v(t) = V_i$. We now have two independent equations in the two unknowns V_i and V_f . Solving these equations, simplifying, and forming the difference $V_f - V_i = \Delta V$ yields the output ripple voltage across the positive voltage terminals:

$$\Delta V = R \Delta I_1 \left[\left(\frac{I_{m1}}{\Delta I_1} + \frac{\tau f}{1-D} \right) \left(1 - e^{-\frac{(1-D)}{\tau f}} \right) - \frac{1-D}{\tau f} \right] \left[\frac{1 - e^{-\frac{D}{\tau f}}}{1 - e^{-\frac{1}{\tau f}}} \right] \quad (36)$$

(a) Charging circuit

(b) Discharging circuit

Fig. 27. Circuit Model for Ripple Analysis for RC Filter.

Multivibrator Clock and Error Amplifier

The clock for the dc-dc converter of Fig. 25 is the astable multivibrator consisting of transistors Q1, Q2, Q3, and Q4 and associated circuitry. The duty cycle of the multivibrator is controlled by the currents I_1 and I_2 from the error amplifier consisting of transistors Q6, Q7, Q8, and Q9 and associated circuitry. The basic reference for the system is provided by the Zener diode V_Z . The negative feedback network is configured so that the magnitude of V_0^+ is nearly equal to the Zener voltage V_Z . The magnitude of V_0^- is set by the turns ratio of L_2 and L_1 . To insure that V_0^- closely tracks V_0^+ , the L_2 and L_1 coils are bifilar wound.

Basic Timing Equations. The transient analysis to obtain the basic timing relationships for the multivibrator can be performed with the help of the models of Fig. 28. These models are shown for the C1 timing capacitor network. The models for the C2 circuit are the same except the start-up network (R1, D1, D2) is omitted.

Writing the charging equations, solving for the times T_1 that Q1 is saturated and T_2 that Q2 is saturated, and simplifying yields

$$T_1 = (R1)(C1) \ln \left[\frac{2 V_B - V_D - V_{CE4}^{sat} - V_{CE2}^{sat} - V_{CE3}^{sat} - V_{BE2}^{sat} - V_{q2} + I_1 R_1}{V_B - V_D - V_{CE4}^{sat} - V_{q1} + I_1 R_1} \right], \quad (37)$$

$$T_2 = \frac{C2}{I_2} [V_B + V_{q1} - V_{CE2}^{sat} - V_{CE4}^{sat} - V_{BE1}^{sat} - V_{q1}], \quad (38)$$

where V_{CE}^{sat} is a collector-emitter saturation voltage; V_{BE} is a base-emitter saturation voltage, V_D is the diode D1 or D2 forward bias voltage, V_{q1} is the base-emitter cut-in voltage, and V_q is the voltage loss across a timing capacitor due to charge removal from the base of Q1 or Q2 during turn-off.

For the usual case where $I_1 R_1$ is sufficiently large to cause the logarithmic argument to approach unity, we can use the approximation

(a) $Q2$ and $Q3$ saturated ; $Q1$ and $Q4$ off

(b)

Fig. 28. Models for Multivibrator Transient Analysis

$$I_n X = (X-1) - \frac{1}{2} (X-1)^2 \quad (39)$$

which when applied to Eq. (37) gives

$$T_1 = \frac{V_{BC1}}{I_1} \left[Y - \frac{V_B}{2I_1 R_1} Y^2 \right], \quad (40)$$

where

$$Y = \frac{1 + \frac{V_{\theta} - V_{CE1}^{sat} - V_{CE3}^{sat} - V_{BE2}^{sat} - V_{q2}}{V_B}}{1 + \frac{V_B - V_D - V_{CE4}^{sat} - V_{\theta}}{I_1 R_1}} \quad (41)$$

The time T_2 can be rewritten as

$$T_2 = \frac{V_{BC2}}{I_2} X, \quad (42)$$

where

$$X = 1 + \frac{V_{\theta} - V_{CE2}^{sat} - V_{CE4}^{sat} - V_{BE1}^{sat} - V_{q1}}{V_B} \quad (43)$$

Equations (40), (41), (42), and (43) are the usual basic timing equations for the astable multivibrator. For those cases of small $I_1 R_1$ values, Eq. (37) must be used instead of Eq. (40).

Duty Cycle of the Multivibrator. The duty cycle is defined as the fractional time that the Q5 VMOS transistor is on (saturated). Thus,

$$D = \frac{T_1}{T_1 + T_2} = \frac{T_1}{T}, \quad (45)$$

where T is the period of the multivibrator.

For the typical case where $C1 = C2 = C$, $2I_1 R_1 \gg V_B$, V_{CE} 's are equal, V_{BE} 's are equal, and $V_{q1} = V_{q2}$, Eq. (45) can be expressed in terms of the error amplifier output currents:

$$D = \frac{I_2}{I + I_{R1}}, \quad (46)$$

where

$$I = I_1 + I_2 \quad (47)$$

and

$$I_{R1} = \frac{V_B - V_D - V_{CE4}^{sat} - V_a}{R_1} \quad (48)$$

It is now clear that the duty cycle is controlled by the error amplifier.

Clock Frequency. The multivibrator frequency of oscillation is the reciprocal of the period T and can be found from Eqs. (40), (42), and (45) as a function of the total current I , the start-up circuit current I_{R1} , the battery voltage V_B , the timing capacitors C , the junction voltages, and the duty cycle D :

$$f = \frac{I}{CV_B Y} [D - D^2(1 + \frac{I_{R1}}{I})]. \quad (49)$$

The frequency depends on the duty cycle and reaches a maximum value when the duty cycle is

$$D_f = \frac{0.5}{1 + \frac{I_{R1}}{I}}, \quad (50)$$

which is slightly less than 50%.

Transfer Characteristic. The error amplifier changes the multivibrator duty cycle by adjusting the charging currents I_1 and I_2 in response to a voltage change at the base of Q9. The input impedance at the Q9 base is large compared to R_9 so that the $\Delta V_{b9} = \Delta V_0^+$. The desired small signal transfer dD/dV_0^+ can be found by multiplying the error amplifier transfer dI_2/dV_0^+ and the multivibrator transfer dD/dI_2 . Since the currents I and

I_{R1} in Eq. (46) are relatively constant for a small change in V_o^+ , differentiation of Eq. (46) yields

$$\frac{dD}{dI_2} = \frac{1}{I + I_{R1}} \quad (51)$$

Using the hybrid-pi model for the error amplifier analysis gives that transfer as

$$\frac{dI_2}{dV_o^+} = - \frac{1}{2(R_e + r_e) \left[1 + \frac{R_e + r_e}{2 R_E} \right]} \quad (52)$$

Thus,

$$\frac{dD}{dV_o^+} = \frac{-1}{(I + I_{R1})(2R_e + 2r_e) \left[1 + \frac{R_e + r_e}{2 R_E} \right]} \quad (53)$$

Start-up Characteristics. The $R1$, $D1$, $D2$ network assures that the multivibrator will always start even if the converter output voltage is zero. The circuit also prevents latch up which can occasionally occur if both $Q1$ and $Q2$ saturate when perhaps the battery power first comes on or other spurious transients occur.

Since the reference voltage for the load is V_B (Fig. 25), the voltage V_a (Fig. 25) is $V_B + V_o^+$. If V_o^+ is less than V_Z as in the startup condition, then the Zener reference V_Z is off and the base of $Q9$ is near $V_B/2$. Since, in this state, V_a is at a voltage at least $V_B - V_{D4}$, there will be a current I_2 flowing into the base of $Q1$ which will cause $Q1$ to saturate. The startup network supplies a current through $R1$ to insure that $Q1$ does not remain in saturation but is pulled out of saturation by $Q2$ coming on. The resistor $R1$ must be chosen large enough to exert minimum effect on the

normal charging current control from the error amplifier output, but small enough to supply adequate base current to saturate Q2 for the entire V_B range and temperature range.

System Considerations

The complete feedback system consisting of the switching regulator, error amplifier, and multivibrator clock will be discussed in this section. Important system considerations are duty cycle limitations, loop transmission synthesis, ripple rejection, voltage regulation, current limitations, and battery voltage range.

Duty Cycle Limitations. A duty cycle limit occurs when the total current I in the emitter resistor R_E is switched through one side of the Q6-Q7 differential pair (Fig. 25). We first consider the case of maximum available duty cycle which occurs for $I_2 = I$.

Setting $I_2 = I = (V_0^+ - 2V_{BE})/(R_E + R_{e/2})$ in Eq. (46) and using Eq. (48) gives the maximum available duty cycle

$$D_{av}^{max} = \frac{1}{1 + \frac{(R_E + R_{e/2})}{R_1} \left[\frac{V_B - V_D - V_{CE4}^{sat} - V_a}{V_0^+ - 2V_{BE}} \right]} \quad (54)$$

It is clear from Eq. (54), that an absolute lower limit on V_B is

$$V_B > V_D + V_{CE4}^{sat} + V_a, \quad (55)$$

to avoid $D = 1$ which is unacceptable for proper regulator operation.

The duty cycle needed, D^{needed} , by the switching regulator is expressed by Eq. (28). Thus,

$$D^{needed} \leq D_{av}^{max}, \quad (56)$$

which leads to a restriction on the range of the battery voltage V_B :

$$V_B \geq \frac{V_s - (V_D + V_{CE4}^{sat} + V_a) \left[\frac{1 + \frac{V_D}{V_o^+}}{1 - \frac{2V_{BE}}{V_o^+}} \right] \left[\frac{R_E + R_{e/2}}{R_1} \right]}{1 - \left[\frac{1 + \frac{V_D}{V_o^+}}{1 - \frac{2V_{BE}}{V_o^+}} \right] \left[\frac{R_E + R_{e/2}}{R_1} \right]} \quad (57)$$

For the components used in the system of Fig. 25, the right side of Eq. (57) is a negative quantity which indicates, for that case, that the restriction on V_B imposed by duty cycle limitations is controlled by Eq. (55).

An important design consideration is expressed by Eq. (54) which shows that for a given V_B and V_o^+ , there is a maximum accessible duty cycle which is constrained by the ratio $(R_E + R_{e/2})/R_1$. The largest duty cycle range is obtained for $R_1 \rightarrow \infty$. Thus, the startup circuit constrains the upper limit of the duty cycle. For an anticipated range of V_B , the ratio $(R_E + R_{e/2})/R_1$ must be chosen to allow the appropriate range in duty cycle for a given V_o^+ .

The minimum accessible duty cycle is zero which occurs for all of the current I being switched through Q6 into the base of Q1 (Fig. 25); consequently, the startup circuit does not constrain the lower limit of the duty cycle.

Loop Transmission Design. The high temperature (300°C) operation of the dc-dc converter constrains the value of capacitors to be no more than $0.1\mu\text{F}$. Investigation of available capacitors indicated that capacitors with values above $0.1\mu\text{F}$ were not sufficiently reliable at 300°C . These low capacitance values make it difficult to establish a dominant pole in the system loop transmission and also to sufficiently suppress ripple in the output voltage.

For greatest reduction in ripple voltages, the dominant pole should be established in the output filter. The low capacitance constraints precluded this usual design strategy. The Q9-Q7 Darlington configuration (Fig. 25) was

used to raise the impedance level at the base of Q9 so R9 could be chosen sufficiently high to establish a dominant pole at the Q9 base for a capacitance C9 of 0.1 μ F. It was then necessary to use a π - section LC filter at the system output to reduce the output voltage ripple due to the clock fundamental frequency. The transistors Q8 and Q9 are a matched pair on the same substrate for good temperature tracking. Having to deal with the significantly large and temperature sensitive base-current voltage drop across R9 is a consequence of this solution of the dominant pole problem.

The loop transmission for small sinusoidal perturbations at low frequencies can be found as follows: Representing the circuit to the left of the cathode of the rectifier diode (Fig. 25) as a voltage source, [see Eq. 29], and assuming that R9 has negligible loading effects on the filter, the small-signal frequency-domain voltage transfer function from the cathode of D4 to the base of Q9 is

$$\frac{\Delta V_{y9}}{\Delta V_{04}} = \left[\frac{1}{1 - \left(\frac{f^2}{f_{cL}^2}\right) + j\left(\frac{f}{f_L}\right)} \right] \left[\frac{1}{1 + j\left(\frac{f}{f_d}\right)} \right], \quad (58)$$

where

$$f_{cL} = \frac{1}{2 \pi \sqrt{L_{F1} C_F}}, \quad (59)$$

$$f_L = \frac{R}{2 \pi L}, \quad (60)$$

$$f_d = \frac{1}{2 \pi (R_{Q9})(C9)}, \quad (61)$$

$$C_F = C_{F1} = C_{F4}, \quad (62)$$

and R_9 is the Thévenin resistance parallel to C_9 . The loop transmission is now found by multiplying Eq. (58) by Eq. (30) and Eq. (53):

$$G(f) = \frac{G(o)}{(1 + j \frac{f}{f_a}) [1 - \frac{f^2}{f_{CL}^2} + j \frac{f}{f_L}]}, \quad (63)$$

where

$$G(o) = \frac{-(V_o^+ + V_D + V_B)^2}{2V_B' \left[(I + I_{R1}) (R_e + r_e) \left[1 + \frac{R_e + r_e}{2R_E} \right] \right]}. \quad (64)$$

Eqs. (63) and (64) can be used to establish the desired output voltage regulation, output voltage stability for system parameter variations, and power supply transient response while maintaining appropriate phase margin against system closed loop oscillations. The $G(f)$ is applicable for small signals and for frequencies lower than the clock frequency.

Load Voltage Regulation for Load Current Changes. Under open-loop conditions ($D = \text{constant}$) the output voltage is given by Eq. (29) rewritten to show dependence on load current:

$$V_o = \frac{D}{1-D} [V_B(I_L) - V_S(I_L)] - V_D(I_L). \quad (65)$$

The rectifier diode voltage changes as the natural logarithm of load current and contributes a small variation in V_o ; the VMOS switch voltage drop V_S is due to current flowing through the channel "on" resistance and is therefore slightly load current dependent; the battery voltage variation is caused by a non zero internal impedance. Inductor core losses increase the switched current and consequently cause a variation in V_o through V_S changes. Small changes in voltage drops across coil resistances also contribute to the open-loop V_o variations.

For the switching regulator with continuous inductor current, the open-loop increment in output voltage, ΔV_o^{ol} , should be quite small for typical load current variations. The closed-loop voltage variation can then be made very small indeed with a large value of loop transmission since

$$\Delta V_o^{cl} = \frac{\Delta V_o^{ol}}{G(0) + 1} \quad (66)$$

Battery Voltage Regulation. The open-loop output voltage changes directly with V_B according to Eq. (29). If large variations in V_B are anticipated, then a high loop transmission must be synthesized to maintain sufficiently stable V_o . For small changes in V_B , Eq. (66) can be used to find corresponding ΔV_o values; for large signals Eq. (66) can be used to estimate ΔV_o values by using some average value of $G(0)$.

Load Current Limitations. The strongest constraint on the maximum value of the load current occurs for the minimum value of V_B . For this condition the VMOS switch is conducting the maximum current which focuses on two important design considerations: (1) the VMOS power dissipation capability must be adequate, and (2) the VMOS drive must be sufficient. The second consideration is usually the most important since the minimum gate voltage drive is available when the VMOS is experiencing the maximum current demand. This condition often establishes the minimum allowable value of V_B .

The peak inductor current must not take the magnetic core into or near saturation if low ripple and high efficiency is to be maintained. This problem is solved by proper sizing of the core, selection of core material, and establishment of proper turns on the core. Careful attention must be given to the core Curie point and the variation of magnetic permeability with temperature and magnetizing force.

Battery Voltage Range. As already discussed, the allowable battery voltage range is constrained by duty cycle limitations and VMOS drive requirements. Another important design consideration is the effect of battery voltage on the multivibrator loop gain which must be much greater than unity to insure fast and reliable switching. In general, the loop gain decreases with V_B for low values of V_B . The loop gain is also temperature dependent. Perhaps the best way to check this effect is to run the multivibrator over the entire temperature range while determining experimentally the minimum V_B for proper astable operations.

Output Voltage Magnitude. The addition of the resistors R_e to adjust the magnitude of the loop transmission causes the output voltage to depend not exclusively on the Zener voltage V_Z . If the base-emitter voltages of the transistors Q6, Q7, Q8, and Q9 are assumed equal in magnitude, then Eqs. (28) and (46), along with a voltage summation from the positive output node to the base of Q8, gives the expression for the positive output voltage:

$$V_o^+ = \frac{b + \sqrt{b^2 + 4c}}{2}, \quad (67)$$

where

$$b = V_Z - V_B' - V_D + R_e I - 2(I + I_{R1})R_e, \quad (68)$$

$$c = (V_Z + R_e I)(V_B' + V_D) - 2V_D R_e (I + I_{R1}). \quad (69)$$

If $R_e = 0$, $V_o^+ = V_Z$.

It would be desirable to set $R_e = 0$ to cause V_o^+ to depend only on the fundamental reference V_Z . However, with the largest allowable capacitance value of 0.1 μF for suitable capacitors, it was necessary to lower the system loop transmission by installing the resistors R_e to maintain loop stability.

In the usual case, an output voltage is specified and the value of V_Z must be computed. Solving Eq. (67) for V_Z yields

$$V_Z = V_o^+ + R_e I \left[1 + 2 \frac{\frac{I_{R1}}{I} (V_o^+ + V_D) - V_B'}{V_o^+ + V_D + V_B'} \right] \quad (70)$$

For the system of Fig. 29, with $V_o^+ = 10$ V and $V_B' = 6$ V, the required value of V_Z is 10.47 volts.

III. DC-DC Converter Implementation

The dc-dc converter of Fig. 25 is shown in Fig. 29 with component values indicated for the design used in the system evaluation over the temperature range 25°C to 300°C. The converter was designed to supply a load current in the range 10mA to 15mA from both +10V and -10V outputs. The output common terminal is at a potential of V_B volts with respect to the converter ground. The negative supply switching coil L_2 is bifilar wound with L_1 to cause close tracking of the two output voltages. The positive output, V_O^+ is sampled for negative feedback control. The error signal applied to the differential amplifier is $V_O^+ - V_Z$ so that the 10V Zener diode IN5240 is the basic reference of the outputs.

The following sections present some implementation details and design calculations. All circuits were constructed with discrete components.

Semiconductor Devices

The bipolar transistors IT127 and IT137 used in the converter had collector leakage current, I_{CO} , of about 10 μ A at 300°C. The important effects of the leakage currents are the following: (1) the I_{CO} induced voltage of about 1V is established across R9 which effectively shifts the reference voltage without compensation. Compensation is accomplished with R8 and by implementing Q8 and Q9 as a matched pair. (2) The I_{CO} induced voltages across R3 and R4 tend to turn Q3 and Q4 on at high temperatures which lowers the converter efficiency and can cause improper multivibrator operation if I_{CO} is too high. We plan to investigate the use of low leakage MOSFET devices to replace the Q3-Q4 pair in future designs. Leakage currents in the other bipolar transistors (Q1, Q2, Q6, Q7) have negligible effects due to the low impedance sinks for the currents.

The start-up circuit diodes and the rectifier diodes are low gate-leakage (10 μ A at 300°C) JFETs connected in a diode configuration. The leakage currents have negligible effect on system operation.

$$L_{F1} = L_{F2} = 7.4 \text{ mH @ } 1 \text{ kHz} \\ = 4.9 \text{ mH @ } 100 \text{ kHz}$$

$$L_1 = L_2 = 5.6 \text{ mH @ } 1 \text{ kHz} \\ = 3.7 \text{ mH @ } 100 \text{ kHz}$$

Fig. 29. DC-DC Converter for High Temperature Tests.

The transistor switch is a fast VMOS device with polysilicon gate. The metal gate VMOS VN33AK device used in earlier designs had excellent drive capability but the rapid fading of the gate threshold voltage (for temperature increasing above about 250°C) caused thermal runaway at high battery currents. The VMOS UN0106N2 devices tested so far do not exhibit this runaway problem (these devices are from supertex, Inc.).

The UN0106N2 has about 8 Ω "on" resistance at 25°C and about 16 Ω at 300°C. The devices can be paralleled to obtain lower "on" resistances and, hence, greater drive capability. The device has a threshold voltage of about 2V at 25°C and 0V at 300°C. The channel leakage current is 4mA at 300°C and about 16mA at 310°C at a gate voltage near zero.

Passive Components

The resistors used in the Fig. 29 circuit were metal film 1% components that have shown only slight changes with temperature cycling. The 0.1 μ F filter capacitors and the 27pF commutating capacitors were the monolithic X7R formulation. The timing capacitors C1 and C2 were NPO ceramic capacitors that showed little change over the temperature range. The X7R capacitors decreased with temperature so that the 300°C value was about 0.4 times the 25°C value. This effect could increase the clock frequency ripple voltage in the converter output and also cause change in the system phase margin. The 0.1 μ F capacitor failures at high temperatures have occurred most often for capacitors under voltage stress; thus, the C9 dominant pole capacitor and the C8 ripple rejection capacitor were returned to V_B for minimum voltage stress.

Frequency of Operation

Low ripple requires high frequency operation of the multivibrator clock. The converter of Fig. 29 runs at about 75 kHz at 25°C and 83 kHz at 300°C according to Eq. (49) for a nominal battery voltage of six volts and an output voltage of 10 volts. The greatest uncertainty in the calculation

of the frequency is caused by the charge removal voltage V_q . For the calculation above, V_q was 1.1 V which was a measured value at 25°C. It is interesting to note that the frequency should theoretically change very little with temperature which is an advantage of the Fig. 29 circuit. Our original goal was to run the system at 100 kHz; however, the smaller values required for C1 and C2 ($\sim 0.001\mu\text{F}$) caused the charge removal voltage V_q to be larger than desired for reliable operation. The experimental results show that the actual frequency of operation of the Fig. 29 circuit is about 100 kHz at 300°C. We think that this higher-than-expected frequency at 300°C is due to a larger V_q caused by a decrease in the frequency response of the IT127 transistors. The solution of this problem requires additional research and perhaps a design modification.

Loop Transmission

The loop transmission for the system of Fig. 29, as obtained from Eqs. (63) and (64) for $V_B^- = 6\text{V}$, $V_O^+ = 10\text{V}$, and load current of 12.5 mA, is

$$T = \frac{-26.11}{(1 + j \frac{f}{15.9}) [1 - (\frac{f}{5860})^2 + j \frac{f}{17200}]},$$

where f is in Hz and the low-frequency values are used for the inductances. The unity gain frequency for T is about 400 Hz and the phase margin is approximately 90°. The low value of loop gain was used to insure high stability against oscillations for a wide range of test conditions over the 25°C to 300°C temperature variation. We would expect to use a much larger loop transmission magnitude in a final design.

IV. Experimental Results And Conclusions

The final circuit of Fig. 29 was breadboarded and tested at high temperatures. The converter was breadboarded on a 3" x 4" ceramic plate. Components were attached to the plate with silver epoxy. Electrical connections were made with the conducting silver epoxy to ensure stability even when the solder was melted.

The converter has been operated at 250°C at a load current of 12.5 mA at $\pm 10V$ output for 102 hours with only small changes in operating characteristics; the battery current increased 4.2%; the frequency decreased 6.3% from 111 to 104 KHZ, and the output voltage decreased 0.8%.

After the 102 hours at 250°C, the temperature was increased to 270°C where a 0.1 μF filter capacitor failed. The filter capacitor was replaced by a chip capacitor (0.1 μF). The converter was then operated about 90 hours at 300°C until other 0.1 μF capacitors failed. The .002 μF NPO timing capacitors C1 and C2 have not failed.

The converter has been cycled from room temperature up to 300°C in excess of 20 times in addition to the 102 hours at 250°C and 90 hours at 300°C. There have been approximately 15 failures (high leakage) of the 0.1 μF capacitors used in the output filters. Most failures have been above 250°C, affecting mostly the capacitors with the highest voltage stress. Thus, a combination of high voltage and temperature stress is required to cause capacitor failure.

There have been no failures or noticable changes in characteristics of any of the semiconductor devices or of the silicon steel inductor cores. Although the VMOS VN33AK device showed thermal runaway at 300°C it did not fail but resumed normal operation at lower temperatures.

The 8064 polythermaleze wire used to fabricate the inductors would not be suitable for 2000 hour operation due to gradual deterioration of the insulating coating.

Data collected from cycling the breadboard model over the 250°C to 300°C temperature range is shown in Figs. 30 through 38.

Figure 30 indicates the total D.C. to D.C. converter efficiency. The gradual decrease of the efficiency with increasing voltage is caused primarily by increasing multivibrator current and losses in the transistor switch due to greater voltage excursions (more time in the active region). Efficiency losses at the lower battery voltages are due to increasing inductor currents, switch losses at reduced drive, and increasing operating frequency. Also, efficiency losses with increasing temperature is caused by increasing multivibrator current and probably by the effect of the reduced mobility of the carriers in the channel of the switch transistor.

Figure 31 indicates the efficiency of the regulator considering the system exclusive of the multivibrator section. Again, the causes and effects are the same except for increase of multivibrator current with temperature and voltage. The efficiency of the converter is low, varying from 30% to 60%; however, the low efficiency may not be detrimental because the power being converted is small.

Figure 32 shows the variation of the switching frequency with temperature and voltage. Note the frequency decreases two-fold at the higher temperatures; this is most likely due to the base charge storage mechanism in transistors Q1 and Q2. The large change in frequency with temperature may be decreased by selecting a device with capability of higher frequency operation. The lower temperature data agrees reasonably with the predicted response.

Figure 33 depicts the duty cycle control variation with temperature and voltage. Increased temperature causes an approximate 5% increase in duty cycle over the room temperature value; this change accounts for increased power losses at the higher temperatures.

Figure 34 shows the fundamental ripple voltage output. Notice that it increases with increasing temperature because the X7R capacitors decrease in value by about a factor of 0.4 from room temperature to 300°C.

Fig. 30. Total Efficiency of the DC-DC Converter.

Fig. 31. Efficiency of the Switching Regulator.

Fig. 32. Frequency of Operation of the Converter.

Fig. 33. Duty Cycle Variation with Battery Voltage.

Figure 35 shows the regulator output voltage at different temperatures and voltages. The voltage increases at the higher temperatures primarily due to an increasing of the voltage reference (Zener Diode) voltage. It is an avalanche diode, therefore, the voltage is expected to increase with temperature. Loss of regulation at lower voltages is caused by lower VMOS drive voltages and reduced channel mobility of the switching device. Small changes in the output voltage at the higher voltages is due to small voltage variations across the error amplifiers emitter resistors and loop transmission changes.

Figure 36 illustrates the spike ripple; that is, the impulse voltage due to switching transients. We think that this ripple is due to grounding and shielding effects that are strongly layout dependent.

Figure 37 shows the spike ripple variation with load changes and is also somewhat unpredictable.

Figure 38 demonstrates the load regulation, which is less than 1% until the system completely loses regulation.

Fig. 34, Fundamental Ripple Voltage.

Fig. 35, Output Voltage Regulation Against Battery Voltage Changes,

Fig. 36. Spike Ripple as a Function of Battery Voltage and Temperature.

Fig. 37. Spike Ripple as a Function of Load and Battery Voltage.

Fig. 38. Load Regulation as a Function of Battery Voltage and Temperature.

CHAPTER V

SUMMARY AND SUGGESTIONS FOR FURTHER STUDY

Research has been performed to investigate semiconductor circuits suitable for operation to a temperature of 250°C. We have verified an amplifier system utilizing four operational amplifiers that will perform adequately at 250°C for greater than 2000 hours. A design for a hybrid thick film amplifier system capable of operation at 300°C has been obtained. Tests have been performed on a DC-DC Converter suitable for operation to 300°C.

During the extent of the last years research, there have been several areas defined that need further clarification and work performed. These areas are clarified as follows:

Amplifier Design

The results of the 300°C evaluation, and the recent downgrading of operating temperature to 230°C maximum, along with improved radiation hardening, have redefined the available options and design concepts.

(1) We can now look into the use of other types of capacitors that will work at 230°C, but could not be considered for 300°C, such as tantalum and electrolytic types. Also, this will allow much larger values (10-100 MFD) to possibly be used, thereby lowering the ripple from the DC-DC converter.

(2) The main problem areas with the amplifiers designed for 300°C are (a) too many capacitors required, (b) too large a range of output dc voltage drift, (c) a 30% reduction in gain-bandwidth product from 25°C to 300°C and (d) most importantly, a poor power-supply rejection of ripple at the frequency of the DC-DC converter (~ 100 kHz). These problems can be considerably alleviated in all areas by going to a differential-amplifier design. With the drift better controlled, we should be able to eliminate several coupling capacitors. We have a design available that is now undergoing computer evaluation, and should be the basic amplifier suitable for the next contract period requirements.

Also, since radiation hardening is required, we will have to use more semiconductor devices to achieve the goals.

(3) In a 230°C maximum environment, there are several other alternative existing dielectrically-isolated single-chip op amps that we must evaluate. This type of design would offer the minimum number of semiconductor devices, wire-bonds, and possible considerably improved reliability, and lower power requirements.

(4) The radiation hardening requirement will require considerable testing to evaluate the overall design compromise.

(5) It is essential that any capacitors utilized in a final design undergo testing at temperature previous to their inclusion in the final circuit.

DC-DC Converter Design

The results of our high temperature tests indicate that additional effort is needed in the following areas, listed in order of importance:

(1) We need to find a more reliable high value (0.1 μ F or above) capacitor for operation to 230°C. This agrees with (1) above.

(2) The multivibrator current at 300°C is about a factor of four above the room temperature value due to high leakage currents in Q3 and Q4 (Fig. 25). This lowers the converter efficiency and in some cases may degrade the VMOS drive pulse.

(3) The multivibrator ripple voltage in the output circuit is typically about 50mV. This may be too high if the power supply rejection of the amplifiers is low. Also, there are switching spikes in the converter output that could generate spurious pulses in the amplifiers. Additional attention should, therefore, be given to grounding, shielding, and filtering.

- (4) At 300°C, the converter loses regulation for battery voltages below about 5.5 volts. This mechanism is not yet well understood. Our design goal was to provide adequate regulation down to a battery voltage of 4 volts over the entire temperature range.
- (5) The converter load and supply voltage regulation is considered marginal with the present loop gain of about 26. Our goal is to raise the loop gain to 100 while still maintaining adequate system stability against oscillations.
- (6) The new Al_2O_3 insulated wire recently obtained needs to be tested as the coil winding at 300°C.
- (7) Radiation hardening of future converter designs would require additional evaluation of all converter components.
- (8) Worst-case computer statistical analysis should be performed after the converter design is finalized.

LIST OF REFERENCES

1. PCAP [Princeton Circuit Analysis Program]. An improvement of the basic IBM ECAP program, developed by W. H. Surber, Princeton University, Copyright, 1970.