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CADMIUM SULFIDE/COPPER SULFIDE HETEROJUNCTION CELL
RESEARCH BY SPUTTER DEPOSITION

Quarterly Technical Progress Report for the Period March 1—June 30, 1981

By
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August 1, 1981

Work Performed Under Contract No. AC02-77CH00178

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Solar Energy

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Period: March 1, 1981 - June 30, 1981

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ABSTRACT

This report covers work conducted during the period March 1, 1981, through June 30, 1981.

A second series of hybrid cells with sputter-deposited Cu_2S layers has been fabricated. An efficiency of about 4 3/4%, without antireflection coating, was achieved for one of the cells. This result approaches the 5 3/4% which was achieved in the first set (different Cu_2S deposition conditions) and confirms the viability of the sputtering process for this application.

Significant progress has been made in fabricating all-sputtered cells with CdS layers deposited by planar magnetron reactive sputtering. Efficiencies of approximately 3%, without antireflection coatings, have been achieved in the as-deposited state for seven cells. Individual cells have yielded a J_{sc} of 12 mA/cm^2 (which exceeds the 2nd quarter goal of 10 mA/cm^2), a V_{oc} of 0.53V, and a fill factor of 0.72. Taken together these parameters would yield an efficiency of 4 1/2%. A strong coupling is found between the properties of the Cu_2S and CdS layers. However, the conditions which maximize J_{sc} , V_{oc} and the fill factor do not appear to be mutually exclusive. Reflectance measurements indicate that 30% or more of the incident radiation is being reflected from the front surface of the cells over the wavelength range of the solar spectrum. Thus optimization of the cell parameters with a suitable antireflection coating should yield cell efficiencies of about 6%.

Characterization of the junctions formed in the all-sputtered cells under near-optimum deposition conditions indicates that they have remarkable properties in their as-deposited state, being very similar to high performance conventional cells after heat treatment. Junction ideality factors are about unity in the light, with J_0 values of about $2 \times 10^{-8} \text{ mA}/\text{cm}^2$. Interface recombination velocities are as low as a few times $10^5 \text{ cm}/\text{sec}$. CdS depletion layer widths are about 2000 nm in the dark and collapse to about 200 nm under illumination.

1. PROJECT DESCRIPTION

1.1 Overall Objective

The overall objective of the program is to investigate and evaluate the application of magnetron reactive sputtering for the production of solar cell quality thin films of CdS/Cu₂S.

Sputtering, particularly using magnetron methods, has great promise for depositing high quality films over large areas at the production volumes required to reach the long term national goals of \$0.15-0.40/peak-watt for thin film photovoltaic modules. A general goal is to find the proper role for sputtering technology in the overall photovoltaic program.

The all-sputter-deposited thin film CdS/Cu₂S solar cells fabricated prior to the present program were characterized by low short circuit currents, and efficiencies of about 1% or less.^{1,2} A specific objective of this program has therefore been to increase the short circuit current and thus improve the efficiency of these devices.¹ Particular attention is being given to identifying differences between sputtered and evaporated coatings and to determining the physical basis for these differences. Accordingly, liberal use is being made of hybrid cells which incorporate various combinations of sputtered and conventionally formed layers (i.e., layers of evaporated CdS and wet and dry CuCl ion exchange-formed Cu₂S).

A three-laboratory team has been assembled to conduct the program.¹ The reactive sputtering process is being investigated, and the sputtered coatings and cells are being prepared, at Telic Corporation. Characterization of the cells and coatings is being done at the Lockheed Palo Alto Research Laboratory. Evaporated CdS coatings for hybrid cells and comparative studies, and wet and dry ion exchange Cu₂S layers for the hybrid cells, are being prepared at the University of Delaware Institute of Energy Conversion. The program is being coordinated by Telic Corporation.

1.2 Work Statement

The present program was formulated to address the deficiencies in the all-sputter-deposited cells, which were identified in previous work and are

reviewed in Ref. 1. The basic tasks are described below.

Task 1 - INCREASE SHORT CIRCUIT CURRENT

This task involves examining the effectiveness of various procedures for increasing the short circuit current. The procedures to be tried include (1) using graded doping concentrations in the CdS layers; (2) using uniform CdS films with improved properties and with conductivity control by doping and off-stoichiometric deposition; (3) etching of the CdS surface in HCl prior to the Cu₂S deposition; (4) using post-deposition in situ heat treatments of the CdS films prior to the Cu₂S deposition; (5) using post-deposition in situ heat treatments of the CdS/Cu₂S heterojunctions; (6) forming hybrid cells by using the ion exchange processes to deposit Cu₂S onto sputtered CdS; and (7) using techniques such as photoluminescence and scanning electron microscopy to evaluate and compare the sputter-deposited CdS with evaporated CdS.

A second quarter goal was to achieve short circuit currents of 10 mA/cm² or greater. (This goal has been achieved for both hybrid and all-sputter-deposited cells.)

Task 2 - OPTIMIZE Cu₂S DEPOSITION

This task involves attempting to establish optimum deposition conditions for sputtering the Cu₂S. This includes a determination of the optimum thickness for the Cu₂S. This task is being performed in conjunction with Task 1 to achieve efficient solar cells. Attention is to be given to comparing and contrasting the characteristics of Cu₂S produced by sputtering and by the ion exchange methods.

Task 3 - IMPROVE DEVICE DESIGN

This task involves making improvements in the basic device design. It is to be undertaken once short circuit currents ≥ 10 mA/cm², as specified in Task 1, are achieved. The task includes examining the effects of better top grid electrode and antireflection coatings. It also includes quantitative photon economy analysis to evaluate improvements and to identify approaches for achieving further improvements.

Task 4 - PLANAR MAGNETRON SPUTTERING

This task involves examining the ability of a planar magnetron sputtering source to produce CdS films of suitable conductivity by off-stoichiometry doping.

Task 5 - DEVICE CHARACTERIZATION AND FABRICATION

This task is being conducted in support of the other tasks described above. It involves characterizing device performance and determining the effectiveness of various post-deposition treatments. The heat treatments are to be conducted in H₂/Ar and in air. The cells are

characterized prior to, and progressively through the course of the heat treatments. The cells are to be characterized by the following techniques:

- 1) I-V characterizations of the solar cells are to be made in the dark and under AM1 illumination.
- 2) C-V characterization of the cells are to be made in the dark, under AM1 illumination, and as a function of the spectral content of the light. The relationship between the junction photo-capacitance and the junction collection efficiency is to be determined.
- 3) The effects of heat treatment on the dark capacitance and photo-capacitance is to be determined.
- 4) The quantum efficiency of selected cells is to be determined as a function of wavelength, both with and without bias light.

The optimum conditions for producing high efficiency CdS/Cu₂S solar cells by sputtering is to be determined. The optimization will include the following:

- 1) Determining the effects of the Cu₂S thickness on J_{sc} and cell performance;
- 2) Determining the effects of graded doping profiles on cell performance;
- 3) Determining the effects on cell performance of in situ heat treatment of the CdS layer prior to the Cu₂S deposition;
- 4) Determining the effects on cell performance of etching the CdS prior to the Cu₂S deposition.

Hybrid cells are to be fabricated and tested as a means of evaluating the performance of the various sputtered layers required to make a cell. This activity is to include:

- 1) Fabrication and testing of hybrid cells in which the Cu₂S is deposited by sputtering onto evaporated CdS that has been demonstrated to be capable of producing conventional cells with efficiencies of over 7.5%.
- 2) Fabrication and testing of hybrid cells which combine sputter-deposited CdS with Cu₂S layers formed by both the wet and dry CuCl ion exchange methods.

A goal for the end of the program is to achieve a 6% efficient cell prepared by ion exchange deposition of Cu₂S onto sputtered CdS or by sputter deposition of Cu₂S onto sputtered or evaporated CdS. (This goal has essentially been met by a hybrid cell with sputtered Cu₂S deposited onto evaporated CdS.)

2. SHORT CIRCUIT CURRENT (Task 1)

2.1 Introduction

The major deficiency in the all-sputter-deposited cells fabricated in our previous work was a low short circuit current (J_{sc}).^{1,2} The cell I-V characteristics indicated that the cause of the low J_{sc} was excessive junction recombination losses. Capacitance-voltage measurements suggested that the recombination losses were due primarily to a low junction electric field, which resulted in turn from the fact that the depletion layer in the sputter-deposited films did not shrink significantly under AM1 illumination. Thus it was concluded that the poor performance of the sputter-deposited cells could be traced primarily to the properties of the CdS layer.² Accordingly, Task 1 involves primarily the examination of processes and procedures which are designed to improve our understanding of the sputtered CdS layer and the properties it must possess for effective use in Cu_2S/CdS solar cells.

The major activity during the present reporting period has involved the evaluation of CdS coatings deposited using a planar magnetron source. The primary method of evaluation has been by the fabrication of all-sputter-deposited cells. Short circuit currents as high as 12 mA/cm^2 have been achieved. This work is discussed in Section 4.0.

Photoluminescence measurements have now been completed on some of the planar magnetron sputtered CdS films. These results are reported in the next section. Preliminary attempts at fabricating hybrid cells with ion exchange Cu_2S formed on cylindrical magnetron sputtered CdS layers are described in Section 2.3.

2.2 Photoluminescence Studies

In studies at the Institute of Energy Conversion an empirical correlation has been found between the photoluminescence spectrum of evaporated CdS layers and their subsequent performance in cells.³ We have previously reported^{1,4} examinations of the photoluminescence behavior at liquid nitrogen temperatures for CdS coatings deposited by cylindrical-post magnetron reactive sputtering

under typical cell deposition conditions; i.e., substrate temperature of 250°C, H₂S injection rate of 57 Pa-liters/sec. Coatings, 6000 nm thick on Nb coated glass substrates, yielded the usual exciton emission at about 490 nm and a "green edge emission" which peaked at longer wavelength (~540 nm) than the edge emission (~520 nm) which is typically seen for the IEC evaporated material.⁴ Thinner such coatings (3000 nm thick), or coatings doped with In, did not yield photoluminescence emission in the visible spectrum.¹ However, 3000 nm thick coatings deposited at lower temperatures (200°C) or on relatively inert substrates (quartz) did yield visible photoluminescence, suggesting the possibility of a substrate interaction.⁴

Photoluminescence data are now available for CdS coatings deposited by planar magnetron reactive sputtering. Even thin (3000 nm thick) planar magnetron coatings have yielded visible photoluminescence emission. Coatings deposited onto Nb coated glass substrates at typical cell deposition conditions (substrate temperature - 250°C, H₂S injection rates of 57 and 70 Pa liters/sec), during our preliminary studies of reactive sputtering with the planar magnetron (see Ref. 4, Sec. 5.0), yielded exciton emission at ~490 nm and green edge emission in the range between 537 and 540 nm. Figure 1 shows the emission spectrum for such a coating deposited at 57 Pa-liters/sec. The spectrum for an evaporated coating is also shown for comparison.

However, despite the observed photoluminescence for some of the thin planar magnetron coatings (e.g., data shown in Fig. 1), no correlation has been found thusfar between the photoluminescence spectra of the planar magnetron coatings and their performance in cells. During our first series of CdS cell fabrications (see Section 4.0) one of the CdS coatings during each run was shielded during the Cu₂S deposition so that its photoluminescence characteristics could subsequently be examined and correlated with the cell properties achieved on the other substrates. The coating thicknesses were typically 4000 nm. CdS layers were examined from seven cell fabrication runs. No visible photoluminescence was observed for any of the coatings,

FIG. 1 Photoluminescence intensity spectrum for CdS film deposited by planar magnetron reactive sputtering. Intensity spectrum of evaporated film shown for comparison. Reactive sputtered film was deposited onto Nb coated glass substrate at 250°C using H₂S injection rate of 57 Pa-liters/sec. Evaporated film prepared at IEC.

even though the cells fabricated in these runs gave short circuit currents as high as 9.15 mA/cm^2 with efficiencies of 2.8%.

2.3 Hybrid Cell Fabrication with Sputtered CdS

Several CdS coatings, prepared by cylindrical magnetron reactive sputterings, had been shipped to IEC for use in the hybrid cell fabrication studies before it became apparent that we could deposit more effective CdS layers, at least in terms of the all-sputter-deposited cells, by using a planar magnetron. These coatings were therefore concluded to be unrepresentative of the best coatings currently being deposited. However, it was decided that the coatings would be processed into cells as a shakedown exercise, since it was necessary to develop techniques for applying the ion exchange method to relatively thin ($\sim 6000 \text{ nm}$) sputtered layers on glass substrates.

The cell fabrication consisted of using screen printing to define $10 \text{ mm} \times 10 \text{ mm}$ cell areas on the $25 \text{ mm} \times 25 \text{ mm}$ CdS/Nb coated glass substrates. The insulating material was cured in an H_2 ambient for 30 min at 170°C . Cu_2S was then applied by the dry ion exchange method to yield an approximate thickness of 150 nm . Standard IEC grid electrodes were applied and the cells were heat treated in H_2 at 150°C for 16 hours. Cell tests indicated large shunt currents. Cell performance was not improved by additional heat treatment at 170°C in H_2 for 40 hrs. Microscope examinations indicated numerous flaws in the CdS which were undoubtedly the cause of the shorting.

Planar magnetron reactive sputtered CdS coatings have now been sent to IEC. However, the need for fabricating hybrid cells with sputtered CdS layers has been decreased considerably by the success of the all-sputtered cells.

3. OPTIMIZATION OF Cu_2S DEPOSITION

3.1 Investigation of Cu_2S Reactive Sputtering

A series of experiments is being performed in which the Cu_2S reactive sputtering equilibration times in the multi-source cell deposition device (see Fig. 5), as manifested by the discharge voltage and coating resistivity, are being examined under various initial cathode and wall conditions selected

to expose the relative effects of these surfaces.^{1,4} Other deposition conditions such as the current density and H_2S injecting rate are being kept constant. The initial cathode and wall conditions being examined are as follows.

- 1) Both cathode and wall surfaces in "clean Cu state" formed by sputter-removing surface layers from the cathode and depositing elemental Cu onto the walls.
- 2) Cathode surface in clean Cu state and wall surfaces in "conditioned-state" formed by extended operation at the operating conditions in question (i.e., cathode current density and H_2S injection rate).
- 3) Cathode surface in conditioned-state and wall surface in clean Cu state formed by the deposition of elemental Cu.

The results of equilibration experiments with the starting conditions listed under (1) and (2) above were reported in Ref. 4. These data are summarized in Fig. 2B by curves (a) and (b) respectively. New data for the starting condition listed under (3) are now available and are given by curve (c). Figure 2A shows the resistivity versus H_2S injection rate for Cu_xS coatings deposited under otherwise constant sputtering conditions in previous work.⁵ The data in Fig. 2B were obtained at a constant H_2S injection rate corresponding to point (x) in Fig. 2A. The runs were of 15 minutes duration, with the substrates introduced through the vacuum interlock shown in Fig. 5.

The data show that the cathode and wall conditioning processes are inter-related. This is believed to be the case because the state of the coating on the walls at a given time influences the system's gettering ability for the injected H_2S .⁶ However, it is the cathode conditioning process which tends to be rate-limiting in determining the system equilibration time for producing coatings with a constant resistivity.

Figure 3 shows the variation in coating resistivity which occurred during a series of runs in which the system was first equilibrated at an H_2S injection rate (27 Pa-liters/sec) corresponding to the rate (x in Fig. 2A) used in Fig. 2B. The injection rate was then reduced to 17 Pa-liters/sec for a sequence of six runs, and then returned to 27 Pa-liters/sec. The data indicate relatively short conditioning times for modest changes in H_2S

FIG. 2 Resistivity of copper sulfide coatings formed by reactive sputtering Cu in Ar+H₂S. (A) Variation of coating resistivity with H₂S injection rate; data from Ref. 5. (B) Equilibration of operation conditions at fixed H₂S injection rate corresponding to (x) in Fig. 2A and three different initial states for cathode and wall surfaces (see text).

FIG. 3 Copper sulfide resistivity variation during series of Cu & H₂S reactive sputtering experiments in which the H₂S injection rate was abruptly increased and then decreased in a system with initially conditioned surfaces.

injection rate in an initially conditioned system.

3.2 Hybrid Cell Fabrication with Sputtered Cu₂S

Hybrid cells, which combine sputter-deposited Cu₂S with solar cell quality evaporated CdS, are being fabricated to provide an evaluation of the sputtered Cu₂S that is independent of the CdS sputtering process.^{1,4} The substrates are standard IEC cell base layers (i.e., 25 mm x 25 mm Zn coated copper sheet, 0.03-0.04 mm thick, onto which evaporated CdS has been deposited to a nominal thickness of 25 μ m). The substrates are shipped to Telic from IEC along with resistivity data for the CdS, and in some cases performance data for conventional cells fabricated from other pieces of the same material.

During each Cu₂S sputter deposition run two CdS substrates and one glass (Corning 7059) reference substrate are coated. The reference coating is used to check the thickness and resistivity of the Cu₂S. Typically one heterojunction from each run is given a Au top grid electrode at Telic (consisting of 0.05 mm lines with a 0.75 mm spacing) and sent to Lockheed. The other heterojunction is sent ungridded to IEC for analysis.

Two sets of hybrid cells have been fabricated thusfar on the program. In the first set, Cu₂S coatings 75 nm, 150 nm, and 300 nm thick were deposited at substrate temperatures of 40°C and 120°C with an H₂S injection rate which yielded resistivities in the range from $4 \times 10^{-3} \Omega\text{-cm}$ to $7 \times 10^{-2} \Omega\text{-cm}$.¹ Cell heat treatments at Lockheed in Ar-2% H₂ at 155°C gave maximum efficiencies of 2.4 to 2.7% for cells with 75 nm Cu₂S layers deposited at 40°C with resistivities of $\sim 10^{-2} \Omega\text{-cm}$.¹ The dependence of J_{sc} on the Cu₂S thickness and resistivity in these cells suggested that the performance of the Cu₂S layer may have been limited by a low minority carrier diffusion length.¹ Therefore a second series of hybrid cells was fabricated with 75 nm, 150 nm, and 300 nm thick Cu₂S layers deposited at 40°C with H₂S injection rates which yielded resistivities in the range from 0.1 to 0.5 $\Omega\text{-cm}$.⁴ Heat treatments of these cells at Lockheed in Ar-2% H₂ at 155°C gave efficiencies in the 1.5 to 1.9% range.⁴ Spectral response measurements indicated a significant reduction in

quantum efficiency for the thick (300 nm) Cu_2S layers and significant absorption in the CdS for the cells with thin (75 nm) Cu_2S layers.

Data from the IEC analysis of the cells from the first series were reported in Ref. 4. Heat treatments were done in pure hydrogen at 170°C rather than in the Ar-H_2 ambient used at Lockheed. Cell efficiencies were in the range 1.6 to 5.75% without AR coatings. The best efficiencies were achieved for cells with 150 nm thick Cu_2S layers deposited at $120\text{--}140^\circ\text{C}$. Unfortunately, the second series of hybrid cell Cu_2S depositions was made at a substrate temperature of 40°C before the above results from IEC analysis were available.

Data are now available for cells from the second group which were examined at IEC. Screen printing was used to define a 10 mm x 10 mm cell area in the center of the substrate. The insulating material was cured in an H_2 ambient for 30 min at 170°C . Laser scans were used to examine the uniformity of the photovoltaic response. The results of these examinations are summarized in Table I. Although the spatial uniformity of the photovoltaic response in these cells is improved over that of the first series, it is still inferior to the standard IEC cells.

Gold grid electrodes consisting of 0.012 mm lines with 0.32 mm line to line spacing were deposited onto the hybrid heterojunctions by evaporation. The cells were heat treated at 175°C in H_2 for periods of 16 hrs (overnight) or 64 hrs (weekend). Ta_2O_5 antireflection coatings were deposited after a period of several heat treatments. In all cases except cell 1719, the improvement in performance with an AR coating was less than 10%. Table II shows representative performance data for this group of cells. In all cases except cell 1719, the data correspond to the maximum performances that were achieved prior to depositing the AR layer (this is done to facilitate comparison with previous cells). The highest efficiency was 4.69% for cell 1782. As with the first series, the best efficiency was achieved for a Cu_2S thickness of 150 nm. The highest short circuit current corresponds to 14.12 mA/cm^2 at 100 mW illumination. Although the 4.7% efficiency is not as high as the 5.74%

TABLE I

LASER SCAN EVALUATION OF Cu_2S UNIFORMITY
(Sputtered Cu_2S /Evaporated CdS Hybrid Cells)

<u>Telic Cell Number</u>	<u>IEC Substrate</u>	<u>Cu_2S Thickness</u>	<u>Cu_2S Temperature</u>	<u>Optical Microscope Examination</u>	<u>Laser Scan Uniformity observation</u>
1719	1047	300 nm	$\sim 45^\circ\text{C}$	Evidence of nonuniform etching. Cracks in Cu_2S and CdS layers.	Large dead zone over 50% of active area.
1779	1047	300 nm	$\sim 40^\circ\text{C}$	"	Relatively uniform.
1782	1055	1500 nm	$\sim 40^\circ\text{C}$	Fewer cracks than other cells. Dots of unetched material in square grid pattern.	Relatively uniform.
1785	1055	750 nm	$\sim 40^\circ\text{C}$	Evidence of nonuniform etching. Cracks in Cu_2S and CdS layers.	Relatively uniform.

TABLE II

PERFORMANCE OF HYBRID CELLS EXAMINED AT IEC
(Sputtered Cu_2S /Evaporated CdS)

Telic cell number	IEC substrate number	Cu_2S thickness	Cu_2S temp.	Cu_2S resistivity	Anneal ⁽⁵⁾ time	J_{sc} ⁽⁶⁾	V_{oc}	FF	η
1719	1047 ⁽¹⁾	300 nm	$\sim 45^\circ\text{C}$	$0.1 \Omega\text{-cm}$ ⁽³⁾	334 hr	4.40 mA/cm^2	0.48V	66.8	1.60%
1779	1047 ⁽¹⁾	300 nm	$\sim 40^\circ\text{C}$	$0.54 \Omega\text{-cm}$ ⁽⁴⁾	81 hr	9.92 mA/cm^2	0.41V	63.8	2.95% ⁽⁷⁾
1782	1055 ⁽²⁾	150 nm	$\sim 40^\circ\text{C}$	$0.42 \Omega\text{-cm}$ ⁽⁴⁾	121 hr	12.96 mA/cm^2	0.44V	71.9	4.69% ⁽⁷⁾
1785	1055 ⁽²⁾	75 nm	$\sim 40^\circ\text{C}$	$0.5 \Omega\text{-cm}$ ⁽⁴⁾	64 hr	13.22 mA/cm^2	0.43V	59.0	3.84% ⁽⁷⁾

(1) CdS thickness = $33 \mu\text{m}$, resistivity = $2.4 \Omega\text{-cm}$.

(2) CdS thickness = $31 \mu\text{m}$, resistivity = $2.9 \Omega\text{-cm}$.

(3) Cu_2S deposited with H_2S partial pressure of 1.50 mTorr. (Pumping speed for $\text{H}_2\text{S} \sim 100$ liters/sec.)

(4) Cu_2S deposited with H_2S partial pressure of 1.25 mTorr.

(5) Heat treatments were made at 170°C in 100% H_2 to increase the short circuit current.

(6) Tested under simulated solar illumination at 87.5 mW/cm^2 .

(7) No antireflection layer.

achieved in the first series (substrate temperature of 140°C), it is higher than any of the low substrate temperature cells in the first series. This improvement is possibly due to the higher Cu₂S resistivity used in the second series. Therefore it is believed that the new data demonstrate that the 5.7% cell which was fabricated during the first series was not an anomaly and that even higher efficiencies can be expected when cells are fabricated at 120°C with higher resistivity Cu₂S on substrates which have been more uniformly etched. Our ability to uniformly etch the substrates should improve with experience. Accordingly, three (CdZn)S substrates have been sent to Telic for use in a third series of Cu₂S hybrid cell depositions.

4. ALL-SPUTTER-DEPOSITED CELLS

4.1 Introduction

Significant progress has been made during this reporting period in fabricating all-sputter-deposited cells in which the CdS layers adjacent to the junction were deposited by planar magnetron reactive sputtering following the procedures described in Ref. 4. A short circuit current of 12 mA/cm² and an efficiency of 3.14% have been achieved for a cell (#2464) with no anti-reflective coating. Short circuit currents of greater than 8 mA/cm² have been achieved for 18 cells. Open circuit voltages are typically between 0.50 and 0.53V. Fill factors as high as 0.72 (cell 2155) have been achieved. The as-deposited junctions are remarkable in their apparent quality. They yield diode ideality factors of near unity and J₀ values of typically about 3x10⁻⁸ mA/cm². Junction recombination velocities of a few times 10⁵ cm/sec are implied.

The achieved short circuit current of 12 mA/cm² (without AR layer) approaches a range of values (15-18 mA/cm² with AR layer) which is estimated to be a reasonable expectation for a planar thin film cell with the configuration currently being used.⁷ The junction recombination losses appear to be largely eliminated. The primary remaining problems are to optimize the Cu₂S layer and to improve the consistency of cell fabrication.

4.2 Basic Cell Configuration

The basic configuration of the all-sputtered cells deposited during the present reporting period is shown in Fig. 4. The substrates are 25 mm x 25 mm x 1.2 mm Corning 7059 glass plates. The rear electrode is Nb. It was initially 100 nm thick and was then increased to 400 nm. The CdS layers are typically about 4000 nm thick. The major portion of the CdS layers were generally undoped and were deposited by reactive sputtering using a planar magnetron source with a Cd target. A thin layer of In doped CdS, typically about 250 nm thick, was placed adjacent to the Nb to assure ohmic contact in most of the cells. This layer was deposited by reactive sputtering using a cylindrical-post magnetron having a target doped typically with 0.1 at.% In. The Cu₂S layer was deposited by reactive sputtering using a cylindrical-post magnetron with a Cu target.

All the layers described above were deposited during a single pumpdown using the multi-source deposition apparatus shown in Fig. 5 and described in detail in Ref. 2. The apparatus was configured with a planar magnetron having a Cd(99.9999%) target and three cylindrical-post magnetrons having Nb, In-doped Cd, and Cu targets. The Au grid electrode was deposited in a separate chamber by evaporation using a mechanical mask. The cell area defined by the grid system was about 130 mm². Antireflection coatings were not used in these cell fabrications.

4.3 Effect of Deposition Conditions

Experiments were conducted to explore the effects of various deposition conditions on the all-sputtered cells. These experiments can conveniently be divided into four groups. The first group explored variations in the CdS-layer deposition conditions with fixed conditions for the Cu₂S layer. The deposition conditions and performance of these cells are summarized in Table III. The second group involved a first attempt at varying the deposition conditions for the Cu₂S layer, with some additional variations in the CdS layer. The data for these cells is summarized in Table IV. The third group, summarized in Table V, comprises a collection of experiments in which

FIG. 4 General configuration of all-sputter-deposited cells prepared during this reporting period. Undoped CdS layer was deposited by planar magnetron reactive sputtering.

FIG. 5 Schematic illustration of multisource deposition apparatus. One of cylindrical magnetron sputtering sources has been replaced with a planar magnetron.

TABLE III

FIRST GROUP OF PLANAR MAGNETRON ALL-SPUTTERED CELLS
 Varied CdS Deposition Conditions with Common Cu₂S Layer⁽¹⁾

Cell Number	Undoped CdS layer			CdS(0.1% In) base layer			Cell Properties ⁽³⁾			
	Temp.	H ₂ S ⁽²⁾	Thickness	Temp.	H ₂ S ⁽²⁾	Thickness	J _{sc}	V _{oc}	FF	η
2082	250°C	4 mTorr	4000 nm	-	-	-	7.60 mA/cm ²	0.50V	0.37	1.4%
2083	"	"	"	-	-	-	7.88 mA/cm ²	0.50V	0.45	1.8%
2091	300°C	4 mTorr	4000 nm	-	-	-	6.74 mA/cm ²	0.47V	0.42	1.4%
2092	"	"	"	-	-	-	-	0.46V	Shunt conductance	
2097	200°C	4 mTorr	4000 nm	-	-	-	8.46 mA/cm ²	0.47V	0.45	1.8%
2098	"	"	"	-	-	-	7.83 mA/cm ²	0.42V	0.52	1.7%
2103	250°C	3 mTorr	4000 nm	-	-	-	5.84 mA/cm ²	0.50V	0.65	1.9%
2104	"	"	"	-	-	-	5.56 mA/cm ²	0.50V	0.55	1.5%
2110	200°C	3 mTorr	4000 nm	-	-	-	6.70 mA/cm ²	0.48V	0.56	1.8%
2111	"	"	"	-	-	-	6.24 mA/cm ²	0.49V	0.54	1.6%
2116	250°C	4 mTorr	4000 nm	-	-	-	9.45 mA/cm ²	0.50V	0.57	2.7%
2117	"	"	"	-	-	-	9.15 mA/cm ²	0.50V	0.62	2.8%
2122 ⁽⁴⁾	250°C	4 mTorr	3750 nm	250°C	4 mTorr	250 nm	4.90 mA/cm ²	0.50V	0.50	1.4%
2123 ⁽⁴⁾	"	"	"	"	"	"	4.60 mA/cm ²	0.55V	-	-
2131	250°C	5 mTorr	3750 nm	250°C	4 mTorr	250 nm	8.08 mA/cm ²	0.50V	0.61	2.4%
2132	"	"	"	"	"	"	7.58 mA/cm ²	0.50V	0.53	2.0%
2137	200°C	5 mTorr	3750 nm	250°C	5 mTorr	250 nm	6.1 mA/cm ²	0.46V	0.25	0.7%
2138	"	"	"	"	"	"	6.2 mA/cm ²	0.42V	0.25	0.7%
2143	250°C	4 mTorr	3750 nm	250°C	4 mTorr	250 nm	8.83 mA/cm ²	0.52V	0.59	2.7%
2144	"	"	"	"	"	"	9.10 mA/cm ²	0.50V	0.61	2.8%
2145	"	"	"	"	"	"	8.85 mA/cm ²	0.51V	0.45	2.0%

TABLE III(Continued)

FIRST GROUP OF PLANAR MAGNETRON ALL-SFUTTERED CELLS
 Varied CdS Deposition Conditions with Common Cu₂S Layer⁽¹⁾

-20-

Cell Number	Undoped CdS layer			CdS(0.1% In) base layer			Cell Properties (3)							
	Temp.	H ₂ S (2)	Thickness	Temp.	H ₂ S (2)	Thickness	J _{SC}	V _{OC}	FF	η				
2155	250°C	4 mTorr	3750 nm	250°C	4 mTorr	250 nm	7.5C mA/cm ²	0.50V	0.72	2.74%				
2156	"	"	"	"	"	"	9.46 mA/cm ²	0.50V	0.65	3.0%				
2157	"	"	"	"	"	"	Shunt conductance							
2158	250°C	4 mTorr	3750 nm	250°C	4 mTorr	250 nm	8.9C mA/cm ²	0.51V	0.66	3.0%				
2159	"	"	"	"	"	"	8.70 mA/cm ²	0.51V	0.63	2.8%				
2160	"	"	"	"	"	"	8.60 mA/cm ²	0.52V	0.65	2.9%				
2161	250°C	4 mTorr	3750 nm	250°C	4 mTorr	250 nm	8.90 mA/cm ²	0.48V	-	-				
2162	"	"	"	"	"	"	8.54 mA/cm ²	0.50V	-	-				
2163	"	"	"	"	"	"	8.08 mA/cm ²	0.50V	0.64	2.6%				
2167	250°C	4 mTorr	1000 nm	250°C	4 mTorr	3000 nm	Glass substrate warped by heat treatment.							
2168	"	"	"	Heat treatment at ~500°C for 60 min.										
2169	"	"	"											
2173	250°C	4 mTorr	1000 nm	250°C	4 mTorr	3000 nm	7.04 mA/cm ²	0.40V	-	-				
2174	"	"	"	"	"	"	1.91 mA/cm ²	0.40V	-	-				
2175	"	"	"	"	"	"	5.86 mA/cm ²	0.41V	-	-				
2179	250°C	4 mTorr	3750 nm	250°C	4 mTorr	250 nm	Shipped to IEC.							
2180	"	"	"	"	"	"	9.25 mA/cm ²	0.53V	0.63	2.75%				
2181	"	"	"	"	"	"	Shipped to IEC.							
2188	250°C	4 mTorr	2000 nm	250°C	4 mTorr	6000 nm	~1 mA/cm ²	~0.1V	-	-				
2189	"	"	"	"	"	"	~1 mA/cm ²	~0.1V	-	-				
2190	"	"	"	"	"	"	~1 mA/cm ²	~0.1V	-	-				

TABLE III(Continued)

FIRST GROUP OF PLANAR MAGNETRON ALL-SPUTTERED CELLS
Varied CdS Deposition Conditions with Common Cu₂S Layer⁽¹⁾

Cell Number	Undoped CdS layer			CdS(0.1% In) base layer			Cell Properties ⁽³⁾			
	Temp.	H ₂ S ⁽²⁾	Thickness	Temp.	H ₂ S ⁽²⁾	Thickness	J _{sc}	V _{oc}	FF	η
2200	250°C	4 mTorr	3000 nm	250°C	4 mTorr	1000 nm	9.86 mA/cm ²	0.50V	0.52	2.38%
2201	"	"	"	"	"	"	7.50 mA/cm ²	0.46V	-	-
2202	"	"	"	"	"	"	8.10 mA/cm ²	0.48V	-	-

All cells deposited on Corning 7059 glass plates with 100 nm thick Nb base electrode.

- (1) Cu₂S layer 150 nm thick deposited at 120°C with Ar pressure of 2.0 mTorr and H₂S pressure of 2 mTorr before discharge ignited. Pumping speed for H₂S ~100 liters/sec.
- (2) H₂S partial pressure before discharge ignited, Ar pressure 1 mTorr.
- (3) Measured at 100 mW/cm²; cells do not have AR coatings.
- (4) Severe arcing encountered during deposition of CdS layer.

TABLE IV
SECOND GROUP OF PLANAR MAGNETRON ALL-SPUTTERED CELLS
First Attempt at Variation of Cu₂S Deposition Conditions

Cell Number	Undoped CdS layer			CdS (0.1% In) base layer ⁽²⁾ Thickness	Cu ₂ S ⁽³⁾		Cell Properties ⁽⁴⁾			η
	Temp.	H ₂ S ⁽¹⁾	Thickness		Temp.	H ₂ S	J _{sc}	V _{oc}	FF	
2245	250°C	4 mTorr	3750 nm	250 nm	120°C	1.25 mTorr	0.5 mA/cm ²	0.15V	-	-
2246	"	"	"	"	"	"	shunt conductance			-
2247	"	"	"	"	"	"	shunt conductance			-
2254	250°C	1.33 mTorr ⁽⁵⁾	3750 nm	250 nm	120°C	1.25 mTorr	0.4 mA/cm ²	0.10V	-	-
2255	"	"	"	"	"	"	0.4 mA/cm ²	0.10V	-	-
2256	"	"	"	"	"	"	shunt conductance			-
2260	250°C	4 mTorr	3750 nm	250 nm ⁽⁶⁾	120°C	1.25 mTorr	0.2 mA/cm ²	0.15V	-	-
2261	"	"	"	"	"	"	0.3 mA/cm ²	0.12V	-	-
2262	"	"	"	"	"	"	0.5 mA/cm ²	0.16V	-	-
2266	250°C	4 mTorr	2000 nm	3000 nm ⁽⁶⁾	120°C	1.25 mTorr	0.2 mA/cm ²	0.10V	-	-
2267	"	"	"	Heat treated	"	"	0.5 mA/cm ²	0.10V	-	-
2268	"	"	"	400°C-60 min.	"	"	0.5 mA/cm ²	0.10V	-	-

- (1) H₂S partial pressure before discharge ignited. Pumping speed for H₂S ~100 liters/sec. Ar pressure = 1 mTorr.
- (2) In-doped CdS deposited using cylindrical-post magnetron. Substrate temperature = 250°C. H₂S partial pressure before discharge is ignited = 4 mTorr. Ar pressure = 1 mTorr.
- (3) Cu₂S layer thickness = 150 nm. Ar pressure = 2 mTorr. H₂S partial pressure is before discharge ignited.
- (4) Measured at 100 mW/cm²; cells do not have AR coatings.
- (5) Run made with planar magnetron operating at 1/3 the current (sputtering rate) that was used in other depositions.
- (6) Glass substrate with 400 nm thick Nb base electrode. All other cells fabricated with 100 nm thick Nb base electrodes.

TABLE V

THIRD GROUP OF PLANAR MAGNETRON ALL-SPUTTERED CELLS
Collection of Experiments involving primarily variations in CdS/Substrate Interface

Cell Number	Undoped CdS layer ⁽¹⁾		In Doped Base layer ⁽²⁾		Substrate	Cu ₂ S ⁽³⁾ Temp.	Cell Properties ⁽⁴⁾			
	H ₂ S	Thickness	In Content	Thickness			J _{sc}	V _{oc}	FF	η
2275	4 mTorr	4000 nm	-	0	400 nm	120°C	7.1 mA/cm ²	0.50V	0.60	2.13%
2276	"	"	-	"	Nb/glass	"	shunt conductance			
2277	"	"	-	"	"	"	8.0 mA/cm ²	0.49V	-	-
2281	1.33 mTorr ⁽⁵⁾	3750 nm	0.1%	250 nm	400 nm	120°C	shunt conductance			
2282	"	"	"	"	Nb/glass	"	5.6 mA/cm ²	0.44V	~0.25	~0.62%
2283	"	"	"	"	"	"	6.2 mA/cm ²	0.48V	~0.30	~0.89%
2290	4 mTorr	2000 nm	0.1%	3000 nm	400 nm	120°C	shunt conductance			
2291	"	"	Heat treated		Nb/glass	"	~1 mA/cm ²	0.18V	-	-
2292	"	"	400°C-60 min.		"	"	shunt conductance			
2299	4 mTorr	5000 nm	-	0	Nb/glass	120°C	~6 mA/cm ²	0.48V	-	-
2300	"	"	-	"	IEC Zn/Cu ⁽⁶⁾	"	~2 mA/cm ²	0.18V	-	-
2301	"	"	-	"	IEC Zn/Cu ⁽⁶⁾	"	~6 mA/cm ²	0.24V	-	-
2305	4 mTorr	3750 nm	0.1%	250 nm	400 nm	45°C	2305 - little PV effect as-deposited J _{sc} = 2.65 mA/cm ² , V _{oc} ~0.44 after heat treatment for 90 min at 135°C in H ₂			
2306	"	"	"	"	Nb/glass	"				
2307	"	"	"	"	"	"				
2365	4 mTorr	3750 nm	0.1%	250 nm	400 nm	160°C	~4 mA/cm ²	~0.2V	~0.25	
2366	"	"	"	"	Nb/glass	"	shunt conductance			
2367	"	"	"	"	"	"	shunt conductance			
2374	4 mTorr	3750 nm	1.0%	250 nm	400 nm	120°C	5.5 mA/cm ²	0.40V	-	-
2375	"	"	"	"	Nb/glass	"	6.0 mA/cm ²	0.45V	0.50	1.35%
2376	"	"	"	"	"	"	5.7 mA/cm ²	0.44V	-	-
2380	4 mTorr	6000 nm	1.0%	250 nm	400 nm	120°C	-	-	-	-
2381	"	"	"	"	Nb/glass	"	0.6 mA/cm ²	0.10V	-	-
2382	"	"	"	"	"	"	2.1 mA/cm ²	0.20V	-	-

TABLE V (Continued)

THIRD GROUP OF PLANAR MAGNETRON ALL-SPUTTERED CELLS
Collection of Experiments involving primarily variations in CdS/Substrate Interface

Cell Number	Undoped CdS layer ⁽¹⁾		In Doped Base layer ⁽²⁾		Substrate	Cu ₂ S ⁽³⁾		Cell Properties ⁽⁴⁾		
	H ₂ S	Thickness	In Content	Thickness		Temp.	J _{sc}	V _{oc}	FF	η
2386	4 mTorr	6000 nm	0.1%	250 nm	400 nm	120°C	1.31 mA/cm ²	0.20V	-	-
2387	Etched in HCl for 40 sec ⁽⁷⁾		"	"	Nb/glass	"	0.6 mA/cm ²	0.16V	-	-
2388			"	"		"	0.6 mA/cm ²	0.16V	-	-
2392	4 mTorr	4000 nm	-	0	400 nm	120°C	4.44 mA/cm ²	0.40V	-	-
2393	"	"	-	"	Nb/glass	"	4.86 mA/cm ²	0.40V	-	-
2394	"	"	-	"		(8)	-	-	-	-
2401	4 mTorr	4000 nm	-	0	400 nm	120°C	Etch test indicates that CdS was removed during heat treatment.			
2402	Heat treated		-	"	Nb/glass	"				
2403	400°C-60 min.		-	"		"				

- 1) Substrate temperature = 250°C. Ar pressure = 1 mTorr. H₂S partial pressure given is value before discharge was ignited. Pumping speed for H₂S ~100 liters/sec.
- 2) In-doped CdS deposited using cylindrical-post magnetron. Substrate temperature = 250°C. H₂S partial pressure before discharge is ignited = 4 mTorr. Ar pressure = 1 mTorr.
- 3) Cu₂S layer thickness = 150 nm. Ar pressure = 2 mTorr. H₂S pressure = 2 mTorr before discharge was ignited. Pumping speed for H₂S ~100 liters/sec.
- 4) Measured at 100 mW/cm², cells do not have AR coating.
- 5) Run made with planar magnetron operating at 1/3 the current (sputtering rate) that was used in the other depositions.
- 6) Zn-plated copper foil substrate material supplied by IEC. (This is the same material that is used for evaporated cells.)
- 7) Substrates 2387 and 2388 were removed from vacuum chamber and etched in HCl at 60°C for 60 seconds prior to depositing Cu₂S layer.
- 8) No Cu₂S layer deposited.

variations were made in the substrate material, the indium content of the doped CdS layer, the deposition rate for the planar magnetron deposited CdS layer, and the substrate temperature for deposition of the Cu_xS layer. The effects of heat treating and of etching the CdS before depositing the Cu_2S were also examined. The fourth group in Table VI comprises a series in which the Cu_2S deposition conditions were varied with a common CdS layer. In all cases the completed cells were shipped under vacuum to Lockheed where their photovoltaic properties were measured.

When the planar magnetron all-sputtered cell studies were begun, conditions for depositing the CdS layer (H_2S partial pressure of 0.53 Pa--corresponding to an H_2S injection rate of 57 Pa-liters/sec and substrate temperature of 250°C) were selected from the planar magnetron reactive sputtering studies described in Ref. 4. These conditions are actually identical to those which had been used for most of the cylindrical magnetron cell studies.² The Cu_2S deposition conditions were selected to be identical to those which had yielded an efficiency of 5.74% in the hybrid cell studies (H_2S partial pressure of 0.27 Pa--corresponding to H_2S injection rate of about 27 Pa-liters/sec and substrate temperature of 120°C).⁴ Subsequent work has indicated that these conditions may be near optimum.

Figures 6 and 7 (data from Table III) show the effect on the short circuit current of varying the H_2S injection rate (Fig. 6), and the substrate temperature for deposition of the CdS layer (Fig. 7), for a constant Cu_2S layer. All the cells are in the as-deposited state (i.e., no heat treatment). The sensitivity of the current-generating Cu_2S layer to the deposition conditions used for the CdS layer is apparent. Figures 8 and 9 show similar data for the open circuit voltage. The V_{OC} appears to be relatively insensitive to the H_2S injection rate used for depositing the CdS layer (Fig. 8), but to be quite dependent on the substrate temperature (Fig. 9). There is insufficient data to define the exact trends. The dashed curves are included only as a guide to viewing the data. However, the originally selected deposition conditions for the CdS do appear to be near optimum, at least for the selected Cu_2S

TABLE VI

FOURTH GROUP OF PLANAR MAGNETRON ALL-SPUTTERED CELLS
 Varied Cu_2S Deposition Conditions with Common CdS Layer⁽¹⁾

Cell Number	Cu ₂ S Layer ⁽²⁾		As Deposited Cell Properties ⁽⁴⁾				Condition	After Anneal			
	Temp.	H ₂ S ⁽³⁾	J _{sc}	V _{oc}	FF	η		J _{sc}	V _{oc}	FF	η
2407	120°C	2.0 mTorr		Poor adhesion			-	-	-	-	-
2408	"	"		"			-	-	-	-	-
2409	"	"		"			-	-	-	-	-
2413	110°C	2.0 mTorr		Poor adhesion			2 1/2 hr/H ₂ /130°C	2.7 mA/cm ²	0.28V	~0.25	-
2414	"	"	1.6 mA/cm ²	0.18V	-	-	-	-	-	-	-
2415	"	"		Poor adhesion			-	-	-	-	-
2424	130°C	2.0 mTorr	0.7 mA/cm ²	0.54V	0.12	-	-	-	-	-	-
2425	"	"	0.6 mA/cm ²	0.49V	0.16	-	-	-	-	-	-
2426	"	"	0.15 mA/cm ²	0.38V	0.15	-	-	-	-	-	-
2430	120°C	2.0 mTorr	7.8 mA/cm ²	0.51V	0.60	2.4%	-	-	-	-	-
2431	"	"	7.7 mA/cm ²	0.50V	0.65	2.5%	-	-	-	-	-
2432	"	"	7.4 mA/cm ²	0.51V	0.61	2.2%	-	-	-	-	-
2436	120°C	2.0 mTorr		Shunt conductance			-	-	-	-	-
2437	"	"	7.0 mA/cm ²	0.51V	-	-	-	-	-	-	-
2438	"	"		Shunt conductance			-	-	-	-	-
2442	110°C	2.0 mTorr	5.86 mA/cm ²	0.45V	-	-	-	-	-	-	-
2443	"	"	5.25 mA/cm ²	0.46V	-	-	-	-	-	-	-
2444	"	"	4.90 mA/cm ²	0.43V	-	-	-	-	-	-	-
2445	130°C	2.0 mTorr	5.08 mA/cm ²	0.45V	-	-	-	-	-	-	-
2446	"	"	5.82 mA/cm ²	0.51V	-	-	-	-	-	-	-
2447	"	"	3.94 mA/cm ²	0.49V	0.61	1.17%	-	-	-	-	-
2451	80°C	2.0 mTorr	0.77 mA/cm ²	0.02V	-	-	1 hr/H ₂ /120°C	4.85 mA/cm ²	0.49V	-	-
2452	"	"	0.77 mA/cm ²	0.03V	-	-	15 hr/H ₂ /120°C	4.77 mA/cm ²	0.51V	-	-
2453	"	"	1.0 mA/cm ²	0.04V	-	-	-	-	-	-	-

TABLE VI (Continued)

FOURTH GROUP OF PLANAR MAGNETRON ALL-SPUTTERED CELLS
 Varied Cu₂S Deposition Conditions with Common CdS Layer⁽¹⁾

Cell Number	Cu ₂ S Layer ⁽²⁾		As Deposited Cell Properties ⁽⁴⁾				Condition	After Anneal			
	Temp.	H ₂ S ⁽³⁾	J _{sc}	V _{oc}	FF	η		J _{sc}	V _{oc}	FF	η
2457	120°C	1.5 mTorr	9.6 mA/cm ²	0.52V	0.62	3.10%	-	-	-	-	-
2458	"	"	9.8 mA/cm ²	0.52V	0.56	2.85%	-	-	-	-	-
2459	"	"	7.7 mA/cm ²	0.52V	0.65	2.60%	-	-	-	-	-
2463	120°C	1.75 mTorr	8.4 mA/cm ²	0.52V	-	-	-	-	-	-	-
2464	"	"	11.7 mA/cm ²	0.51V	0.48	2.89%	1 hr/H ₂ /125°C	12.0 mA/cm ²	0.52V	0.51	3.14%
2465	"	"	7.16 mA/cm ²	0.49V	-	-	-	-	-	-	-
2469	120°C	1.25 mTorr	Shunt conductance				-	-	-	-	-
2470	"	"	Not photovoltaic				1 1/2 hr/H ₂ /123°C	0.6 mA/cm ²	0.16V	-	-
2471	"	"	Shunt conductance				-	-	-	-	-
2475	120°C	2.5 mTorr	7.14 mA/cm ²	0.50V	-	-	-	-	-	-	-
2476	"	"	7.03 mA/cm ²	0.51V	-	-	1 1/2 hr/H ₂ /123°C	7.03 mA/cm ²	0.52V	-	-
2477	"	"	5.68 mA/cm ²	0.45V	(shunt conductance)		-	-	-	-	-
2490	120°C	2.25 mTorr	4.2 mA/cm ²	0.50V	-	-	-	-	-	-	-
2491	"	"	7.1 mA/cm ²	0.44V	-	-	-	-	-	-	-
2492	"	"	7.1 mA/cm ²	0.52V	-	-	-	-	-	-	-
2499	120°C	2.0 mTorr	4.96 mA/cm ²	0.50V	-	-	-	-	-	-	-
2500	"	"	4.74 mA/cm ²	0.46V	-	-	-	-	-	-	-
2501	"	"	Shunt conductance				-	-	-	-	-
2509	120°C	1.75 mTorr	9.25 mA/cm ²	0.53V	-	-	-	-	-	-	-
2510	"	"	8.70 mA/cm ²	0.49V	-	-	-	-	-	-	-
2511	"	"	9.49 mA/cm ²	0.49V	-	-	-	-	-	-	-
2517	120°C	1.50 mTorr	9.30 mA/cm ²	0.52V	-	-	-	-	-	-	-
2518	"	"	9.27 mA/cm ²	0.53V	-	-	-	-	-	-	-
2519	"	"	10.07 mA/cm ²	0.52V	-	-	-	-	-	-	-

TABLE VI (Continued)

FOURTH GROUP OF PLANAR MAGNETRON ALL-SPUTTERED CELLS
Varied Cu_2S Deposition Conditions with Common CdS Layer⁽¹⁾

All cells deposited onto Corning 7059 glass plates with 400 nm thick Nb base electrode.

- (1) CdS layer consists of a 250 nm thick base layer of CdS doped with 0.1% In, deposited using a cylindrical-post magnetron at 1 mTorr of Ar and 4 mTorr of H_2S (before discharge ignited) with substrate temperature of 250°C, and a 3750 nm thick top layer of undoped CdS, deposited using a planar magnetron and same deposition conditions (H_2S partial pressure and substrate temperature) as the base layer.
- (2) Cu_2S layer thickness = 150 nm.
- (3) H_2S partial pressure before discharge ignited (pumping speed for H_2S $\sim$ 100 liters/sec).
- (4) Measured at 100 mW/cm²; cells do not have AR coatings.

FIG. 6 Dependence of the short circuit current in the all-sputtered cells (as-deposited state) on the H₂S injection rate used to deposit the CdS layer with other deposition conditions listed on the figure held constant. The dashed curve is drawn only to assist in reading the figure; maxima at intermediate injection rates are clearly possible.

FIG. 7 Dependence of the short circuit current in the all-sputtered cells (as-deposited state) on the substrate temperature during the CdS deposition with other deposition conditions listed on the figure held constant. The dashed curve is drawn only to assist in reading the figure; maxima at intermediate temperatures are clearly possible.

FIG. 8 Dependence of the open circuit voltage in the all-sputtered cells (as-deposited state) on the H₂S injection rate used to deposit the CdS layer with other deposition conditions listed on the figure held constant. The dashed curve is drawn only to assist in reading the figure; maxima at intermediate injection rates are possible.

FIG. 9 Dependence of the open circuit voltage in the all-sputtered cells (as-deposited state) on the substrate temperature during the CdS deposition with other deposition conditions listed on the figure held constant. The dashed curve is drawn only to assist in reading the figure; maxima at intermediate temperatures are clearly possible.

layer. Consequently a relatively large number of cells (26) have been deposited under these conditions. The average J_{sc} for these cells is 8.26 mA/cm² with a standard deviation σ of 0.78 mA/cm² (9%). The average V_{oc} is 0.50V with a standard deviation of 0.013V (2.5%). Thus although the number of data points for the "off-optimum" conditions is limited, they tend to fall considerably outside $\pm \sigma$.

Figures 10 and 11 (data from Table VI) show the dependence of the short circuit on the H₂S injection rate (Fig. 10), and substrate temperature (Fig. 11), used in depositing 150 nm thick Cu₂S layers onto CdS deposited under the apparent optimum conditions suggested by Figs. 6 to 10. Similar data for the open circuit voltage are shown in Figs. 12 and 13. Again the dashed curves are drawn only to assist in viewing the data. The originally selected substrate temperature of 120°C appears to be near optimum for producing maximum J_{sc} and V_{oc} . Although there is considerable scatter in the data, an H₂S injection rate that is slightly less than the 27 Pa-liters/sec used as a starting point appears to be optimum for achieving maximum values for both J_{sc} and V_{oc} . An important observation is that the conditions which yield maximum values for J_{sc} and V_{oc} do not appear to be mutually exclusive.

The best all-sputtered cells produced to date are summarized in Table VII. Note that most of the cells are in their as-deposited state. Attempts to use heat treatment to improve the performance of all-sputtered cells deposited under the "near optimum" conditions described above have in general been thwarted by a tendency of the cells to develop a high series resistance or an I-V characteristic typical of a back-to-back diode. Thus evidence of a blocking contact was seen in several of the first cells produced (2082-2117) when I-V characteristics were taken at 200°C and in all of them after heat treatment at 170-180°C in H₂. This led to the use of the In-doped base layer for most of the subsequent cells (see Tables IV through VI). Cells fabricated with the 250 nm thick In doped base layer did not develop the back-to-back diode characteristic at 200°K, but often did so after heat treatment in H₂ for several hours at 170-180°C. Consequently, more modest heat treatments

FIG. 10 Dependence of short circuit current in the all-sputtered cells (as-deposited state) on the H₂S injection rate used to deposit the Cu₂S layer with other deposition conditions listed on the figure held constant. Dashed curve is drawn only to assist in reading the figure. Arrow denotes observation that injection rate of 17 Pa-liters/sec yielded cells with negligible short circuit current.

FIG. 11 Dependence of the short circuit current in the all-sputtered cells (as-deposited state) on the substrate temperature during the Cu₂S deposition with other deposition conditions listed on the figure held constant. Dashed curve is drawn only to assist in reading the figure; maxima at intermediate temperatures are clearly possible.

FIG. 12 Dependence of the open circuit voltage in the all-sputtered cells (as-deposited state) on the H₂S injection rate used to deposit the Cu₂S layer with other deposition conditions listed on the figure held constant. Dashed curve is drawn only to assist in reading the figure. Arrow denotes observation that injection rate of 17 Pa-liters/sec yielded cells with negligible open circuit voltage.

FIG. 13 Dependence of the open circuit voltage in the all-sputtered cells (as-deposited state) on the substrate temperature during the Cu₂S deposition with other deposition conditions listed on the figure held constant. Dashed curve is drawn only to assist in reading the figure; maxima at intermediate temperatures are clearly possible.

TABLE VII
HIGHEST PERFORMANCE ALL SPUTTERED CELLS PRODUCED TO DATE

<u>Cell Number</u>	<u>J_{sc}</u>	<u>V_{oc}</u>	<u>FF</u>	<u>η</u>	<u>Heat Treat</u>
2117	9.15 mA/cm ²	0.50V	0.62	2.8%	None
2144	9.10 mA/cm ²	0.50V	0.61	2.8%	None
2156	9.46 mA/cm ²	0.50V	0.65	3.0%	None
2158	8.94 mA/cm ²	0.51V	0.66	3.0%	None
2159	8.70 mA/cm ²	0.51V	0.63	2.8%	None
2160	8.60 mA/cm ²	0.52V	0.65	2.9%	None
2463	12.0 mA/cm ²	0.52V	0.51	3.14%	1 hr/H ₂ /125°C

at 130°C in H₂ have been used in our more recent work (see Table VI).

Cell 2463 in Table VII is an exception to the above description. This cell, which had a relatively good as-deposited performance, underwent slight improvements in J_{sc} (11.7 to 12.0 mA/cm²), V_{oc} (0.51 to 0.52V) and FF (0.48 to 0.51) after a modest heat treatment at 125°C. Cells with Cu₂S layers deposited at temperatures significantly below the apparent optimum of 120°C shown in Fig. 11 generally did not have well developed junctions in their as-deposited state. In these cases the cell performance improved considerably on heat treatment. For example, cells 2451 and 2452, with Cu₂S layers deposited at 80°C, were ohmic in their as-deposited state, but developed reasonable characteristics, i.e., J_{sc} ~ 5 mA/cm² and V_{oc} ~ 0.50V, after heat treatment in H₂ at 120°C.

A few experiments have been conducted to explore the effects of the thickness and indium content of the doped CdS base layer on the cell performance. Doped base layers having an In content of 0.1 at.% and thicknesses of from 250 nm to 6000 nm have been deposited in combination with undoped planar magnetron CdS surface layers of from 1000 to 4000 nm in thickness. (See cells 2173-75, 2188-90, and 2200-02.) The key parameter appears to be the thickness of the undoped CdS layer. Cells in which this layer was less than 3000 nm had significantly reduced V_{oc} (e.g., cell 2173) and in some cases also low J_{sc} (cell 2188). When the In content of the base layer was increased to 1.0 at.%, even cells with 4000 nm thick undoped layers deposited over 250 nm doped layers exhibited low V_{oc} (cells 2374-2476). Clearly the number of cells examined is insufficient to develop definite conclusions. However, based on these observations we have adopted the working hypothesis that it is desirable to keep In away from the junction.

A fill factor of 0.72 was achieved for cell 2155 when a scribe was used to reduce the active area of a larger cell which had been characterized by a shunt conductance problem. This suggested that the Nb layer was contributing significant series resistance. Accordingly, the Nb thickness was increased from 100 to 400 nm for cells 2260 and beyond.

Several special experiments were conducted in which one or two cell deposition runs were made with various perturbations to the basic cell fabrication process that had yielded the highest performance cells. The data are somewhat inconclusive because of the small number of samples involved. However, in no case was the cell performance superior to that of the cells produced under the optimum conditions suggested by Figs. 6.-13. Thus cells 2300 and 2301 were deposited onto the standard Zn coated Cu substrate material used by IEC. Although a J_{sc} as high as 6 mA/cm^2 was achieved for cell 2301, the V_{oc} was only about 0.2V. In the case of cells 2386-88 the sputtered CdS coatings were removed from the chamber and etched in 25% (by volume) HCl at 60°C for 40 sec before being returned to the chamber for sputter deposition of the Cu_2S layer. The cell performance was poor. In the case of cells 2266-68, 2290-92, and 2401-03 the CdS layers were heat treated in vacuum for typically 60 min at $400\text{-}500^\circ\text{C}$ before the Cu_2S layer was deposited. The cells were characterized by high shunt conductances. The Cu_2S layer in cell 2386 was removed by etching in KCN. No evidence of a CdS layer remained. Apparently most of the CdS layer evaporated during the vacuum heat treatment, thereby causing the high shunt conductance.

The improvement in performance for the all-sputtered cells occurred when we began using the planar magnetron source to deposit the undoped CdS layer that is adjacent to the junction. One difference between the planar magnetron and the previously used cylindrical magnetrons is that the deposition rate is about a factor of three higher in the planar magnetron case.⁴ Therefore an experiment was conducted in which the planar magnetron discharge current (sputtering rate) and the H_2S injection rate were reduced by a factor of three. The cells (2281-83) gave performances ($J_{sc} \sim 6 \text{ mA/cm}^2$, $V_{oc} \sim 0.46$, $FF \sim 0.25$) which were poor compared to the other planar magnetron cells but similar to what has previously been obtained with the best cylindrical magnetron cells.

4.4 Special Cell Characterization Studies

A series of studies have been conducted at Lockheed to characterize the photo-electron charge generation and collection processes within the all-sputtered cells.

The I-V characteristic of the CdS/Cu₂S solar cell can be described by an equation of the following form if the series resistance and shunt conductances effects can be neglected.⁸

$$J = J_0 \left[\exp \left(\frac{qV}{AkT} \right) - 1 \right] - \eta_c J_L = \frac{I}{A_j} \quad (1)$$

where

$$J_0 = J_{00} \exp \left(- \frac{\phi_B}{kT} \right) \quad , \quad (2)$$

$$J_{00} = q N_c S_i \quad , \quad (3)$$

and

$$\eta_c = \frac{\mu F}{S_i + \mu F} \quad , \quad (4)$$

with

$$F = \left[\frac{2qN_D^*(V_D - V)}{\epsilon \epsilon_0} \right]^{1/2} \quad (5)$$

In the above equations:

- J is the cell current density,
- V is the cell voltage,
- J_L is the light generated current which reaches the junction,
- ϕ_B is the junction barrier potential,
- q is the electronic charge,
- A is the diode ideality factor,
- A_j is the junction area,
- kT is the temperature (in energy units),
- N_c is the effective density of states at the CdS band edge (2x10¹⁸cm⁻³),
- S_i is the interface recombination velocity,

η_c is the interface collection factor,
 μ is the electron mobility in the CdS,
 F is the electric field at the junctions,
 V_D is the diffusion potential (0.8V),
 $\epsilon\epsilon_o$ is the CdS dielectric constant,
 N_D^* is the CdS donor density.

At short circuit conditions ($V=0$) one has

$$J_{sc} = \eta_c J_L = \left(\frac{\mu F}{S_i + \mu F} \right) J_L \quad (6)$$

with

$$F = \left(\frac{2qV_D N_D^*}{\epsilon\epsilon_o} \right)^{1/2} = \frac{2V_D}{W} \quad (7)$$

where W is the depletion layer width.

Figure 14 shows the I-V characteristic in the as-deposited state for one of the all-sputtered cells deposited on the present program using planar magnetron reactive sputtering to form the CdS layer. Note that the characteristic is relatively flat in the vicinity of the J_{sc} point; i.e., no voltage dependence in reverse bias. This implies that $\mu F \gg S_i$ in Eq. (6); i.e., that the combination of low recombination velocity and high junction electric field is sufficient to make $\eta_c \sim 1.0$ so that very little of the light-generated current J_L which reaches the junction is lost. See Eq. (6). Typical conditions for achieving $\eta_c \sim 0.95$ are⁹: $S_i/\mu \sim 5 \times 10^3$ V/cm⁻¹, which implies $S_i \sim 1.5 \times 10^5$ cm/sec at $\mu = 30$ cm²/V-sec; and $F \sim 10^5$ V/cm, which implies that $W \sim 200$ nm. That these conditions are being achieved for the all-sputtered cells presently being deposited has been shown by independent I_{sc} vs V_{oc} and junction capacitance measurements which are described below. It should be noted that this was not the case in the all-sputtered cells, with cylindrical magnetron reactively sputtered CdS, which were prepared on the previous program. (See section 2.1.) In those cells $\mu F \ll S_i$, and J was proportional to $V^{1/2}$ under reverse bias, as would be predicted by combining Eqs (1), (4) and (5).²

FIG. 14 I-V characteristic for typical all-sputtered cell deposited under near-optimum conditions.

Combining Eqs (1) and (6) under open circuit voltage conditions ($V = V_{oc}$, $J = 0$) yields

$$V_{oc} = \frac{AkT}{q} \ln \left(\frac{J_{sc} + J_0}{J_0} \right) \quad (8)$$

The slope of a plot of V_{oc} versus $\log I_{sc}$ thus yields the A-factor and the zero-voltage intercept yields J_0 . Figure 15 shows such a plot for cell 2143. The data were obtained by using a neutral density filter to reduce the light intensity reaching the cell from an AM1 source. The data indicate an A-factor of 1.0 and a J_0 of 2.3×10^{-8} . A-factors were typically between 1.0 and 1.2, with J_0 values between 2×10^{-8} and 2×10^{-7} , for cells deposited under the near optimum conditions described in the preceding section. $J_0 \leq 5 \times 10^{-8} \text{ mA/cm}^2$ has been suggested as being indicative of a junction where interface recombination is not a serious loss mechanism.¹⁰

Figure 16 shows $\log I_{sc}$ vs V_{oc} data taken at temperatures of 197°K and 300°K for cell 2180. J_0 values at the two temperatures were then used to determine J_{00} and ϕ_B from Eq (2). S_i was then determined from J_{00} using Eq (3). The implied values were $\phi_B = 0.95 \text{ eV}$ and $S_i = 1.88 \times 10^5 \text{ cm/sec}$. Thus an independent measurement of the junction recombination velocity for a typical cell shows it to be in a range where serious recombination losses would not be expected.

C-V measurements have been made on cells 2083 and 2155 in the dark and under one third AM1 illumination. The dark $1/C^2$ versus V curves show the characteristic abrupt change in slope which is generally associated with the presence of a compensated region of small carrier concentration adjacent to the junction.⁸ The implied widths for the compensated region were about 2000 nm, with carrier concentrations of about $3 \times 10^{14} \text{ cm}^{-3}$, for both cells. These data for the all-sputtered cells, in the as-deposited state, are comparable to those obtained for the typical IEC evaporated cells after heat treatment. Under one third AM1 illumination the $1/C^2$ versus V curves had

FIG. 15 $\log I_{SC}$ versus V_{OC} data for typical all-sputtered cell deposited under near-optimum conditions.

FIG. 16 Log I_{sc} versus V_{oc} data at two temperatures which were used to determine junction barrier potential and recombination velocity (see text).

the form generally associated with depletion layer collapse due to hole trapping.⁸ The implied depletion layer widths were about 200 nm with carrier concentrations of $\sim 2 \times 10^{16} \text{ cm}^{-3}$. These results for the all-sputtered cells are again nearly identical to those seen for the IEC cells under AM1 illumination. The implied diffusion voltages for the all-sputtered cells were 0.6 to 0.8V. Thus evidence from several independent measurements indicates that the junctions formed in the all-sputtered cells in the as-deposited state are very similar to those formed in the high performance IEC cells after heat treatment.

In the course of making the C-V measurements considerable dispersion was noted over the frequency range from 100 Hz to 100 KHz. In reviewing the theory of capacitance measurements, or more particularly admittance measurements, it was apparent that considerable dispersion in the measured impedance (admittance) is actually to be expected for depletion layers within which there exists a spatially varying majority carrier concentration. This occurs because the width of depletion layer, that satisfies the condition that the dielectric relaxation time be large compared to the period corresponding to the probing frequency, and that therefore is implied by measurements at a given frequency, depends inversely on the average carrier concentration within the layer. High frequencies imply thicker depletion widths than low frequencies. The development and application of this theory will be described in the final report.

Figure 17 shows relative spectral response data for one of the all-sputtered cells in the dark and under 20% AM1 illumination. The relative shape of the curve is virtually identical in both cases. The lack of shape variation may be a consequence of the low interface recombination velocity which makes the collection efficiency relatively insensitive to the junction electric field [see Eq (4)].

Figure 18 shows the reflectance over the wavelength range from 400 nm to 1100 nm for cell 2145 which had a J_{sc} of 8.85 mA/cm^2 . This data is typical

ALL-SPUTTERED CELL - QUANTUM EFFICIENCY

FIG. 17 Relative spectral response of short circuit current, with and without bias illumination, for typical all-sputtered cell deposited under near-optimum conditions.

FIG. 18 Reflectance versus wavelength for top surface of typical all-sputtered cell deposited on glass substrate without antireflection coating.

for the all-sputtered cells deposited on glass substrates. The reflectance is 30% or greater over the wavelength range of the solar spectrum. Therefore antireflection coatings should be quite effective in increasing the performances of these devices.

4.5 Cell Stability

Formal stability tests of the all-sputtered cells are premature until the cells are optimized sufficiently to place the efficiency into the 5% range. Nevertheless the stability of these thin film devices with reactively sputtered Cu_2S layers is a vital question. Therefore one of the early 3% cells (2457) was set aside and tested periodically after storage, with no electrical loading, under laboratory conditions. After ~ 700 hrs the V_{oc} remained unchanged at (0.52V). However, the J_{sc} had decreased from 9.45 mA/cm^2 to 8.17 mA/cm^2 ($\sim 14\%$) and the fill factor from 0.62 to 0.52 ($\sim 16\%$), giving an efficiency decrease from 3% to 2.2% (27%). Heat treatment for 2 hrs at 130°C increased J_{sc} to 8.72 mA/cm^2 , the fill factor back to 0.62, and the efficiency to $\sim 2.8\%$.

5. IMPROVED DEVICE DESIGN

No formal work on this task was conducted during this reporting period. Future work will examine the use of antireflective coatings on the all-sputtered cells and the fabrication of cells with back walled configurations which should provide greater protection of the Cu_2S layer from the atmosphere.

6. PLANAR MAGNETRON SPUTTERING

Planar magnetron work during this reporting period has involved the fabrication of all-sputtered cells. This work is described in Section 4.0.

7. DEVICE CHARACTERIZATION AND FABRICATION

Work at Lockheed during this reporting period has involved the characterization and heat treatment studies on the all-sputtered cells which were described in Section 4.3 and the special cell characterization studies described in Section 4.4. The latter include: (1) $\log I_{sc}$ vs V_{oc} measurements to determine

the junction A-factor and barrier height, the J_0 value, and the interface recombination velocity; (2) C-V measurements to determine the depletion layer width and donor density in the CdS; (3) spectral sensitivity measurements in the dark and under an AM1 bias; and (4) reflectance measurements for the top surface of the cells. Additional work has been done to gain insight into the physical basis for dispersion effects which have been seen during the C-V measurements. This analysis will be included in the final report.

Work at IEC during this reporting period has involved photoluminescence measurements on planar magnetron sputtered CdS coatings (Section 2.2), the fabrication of hybrid cells by depositing ion exchange Cu_2S onto sputtered CdS (Section 2.3), and characterization and heat treatment studies on hybrid cells with sputtered Cu_2S layers (Section 3.2). Evaporated (CdZn)S coatings have been prepared and sent to Telic for use in forming hybrid cells with sputtered Cu_2S layers.

8. SUMMARY STATUS

Continued encouraging results have been achieved with hybrid cells which combine sputtered Cu_2S with evaporated CdS. Although there is reason to believe that the sputtered Cu_2S layers in the second series of cells described in this report were not deposited under optimum conditions (substrate temperature), an efficiency of 4 3/4% (no AR coating) was achieved. This result tends to confirm the efficiency of about 5 3/4% which was achieved in the first series. These 4 3/4% and 5 3/4% cells have short circuit currents, under 100 mW/cm² illumination, of 14 mA/cm² and 20 mA/cm² respectively, which with optimized AR coatings should approach those achieved in the conventional IEC cells. Laser scan measurements show that the spatial uniformity of hybrid cells is inferior to that of the typical IEC cells. Therefore performance improvements in the hybrid cells with sputtered Cu_2S layers are expected when the deposition conditions for the Cu_2S layer are optimized and when Telic has gained more experience in performing the pre-deposition etch of the CdS layer.

The hybrid cells were originally fabricated primarily as a method for evaluating the sputtered Cu_2S . However, the success which has been achieved with these cells suggests that hybrid cells with evaporated CdS layers and sputtered Cu_2S layers might provide an effective configuration for large scale all-vacuum production. Accordingly, our future plans call for the fabrication of cells in which sputtered Cu_2S would be deposited onto evaporated (CdZn)S. In addition, Cu_2S will be deposited directly onto glass substrates having predeposited Au grids or Sn-doped In_2O_3 base electrodes. The Cu_2S coated substrates will then be sent to IEC, where CdS will be evaporated onto the Cu_2S to form junctions. The purpose is to form cells which are configured to enclose the Cu_2S under a protective CdS layer which may improve the cell stability.

A few hybrid cells have been fabricated which combine sputtered CdS with ion-exchange-formed Cu_2S . The devices were characterized by high shunt conductances. However, the need for fabricating hybrid cells of this type has been largely removed by the success which has been achieved with the all-sputtered cells.

All-sputter-deposited thin film (CdS-4000 nm) Cu_2S /CdS cells with efficiencies of $\sim 3\%$ in the as-deposited state (with no antireflection coating) have repeatedly been obtained during the present reporting period. The maximum efficiency achieved is 3.14%. On various individual cells, critical solar cell parameters of $J_{\text{sc}} = 12 \text{ mA/cm}^2$, $V_{\text{oc}} = 0.53\text{V}$, and $\text{FF} = 0.72$ have been achieved. If these parameters could be combined into a single cell, this would result in an efficiency of 4.5%. Cell reflectivity measurements show that 30% or more of the incident radiation is lost by reflection for wavelengths corresponding to the solar spectrum (400 nm to 1100 nm). Thus an optimized antireflection coating could increase the efficiency to about 6%.

Studies of the influence of individual layer deposition conditions on cell performance indicate a strong coupling between the properties of the Cu_2S and CdS layers. Fortunately, however, the conditions which maximize

J_{sc} , V_{oc} , and the fill factor do not appear to be mutually exclusive. Thus significant improvements in efficiency should be possible. An approximate analysis has been made to estimate the short circuit current which might reasonably be expected for a thin film Cu_2S/CdS cell having the configuration being used.⁷ The analysis assumes that the Cu_2S layer optical properties can be described by Molder's single crystal data.¹¹ Measured values are used for the spectral reflectance of the rear Nb electrode over the wavelength range of the solar spectrum. Ninety percent of the incident light is assumed to enter the Cu_2S and make a single pass down to the Nb surface and back through the Cu_2S with no absorption in the CdS. Short circuit currents calculated for various Cu_2S thicknesses and minority carrier diffusion lengths are shown in Fig. 19.

The junctions in the all-sputtered cells deposited under near optimum conditions are remarkable in their as-deposited properties. Junction A-factors under light are near unity with J_0 values of $\sim 5 \times 10^{-8}$ mA/cm². I-V characteristics, J_0 versus temperature, and spectral response measurements imply a low interface recombination velocity ($\sim 5 \times 10^5$ cm/sec). C-V measurements indicate that the as-deposited depletion layer widths are comparable to those in the IEC cells after heat treatment (~ 2000 nm) and that they collapse under AM1 illumination to values (~ 200 nm) which are again comparable to the IEC cells and thereby produce strong fields at the junction. Thus the important goal in the present program of increasing the junction electric field and reducing the interface recombination losses has been achieved.

The improvement in performance of the all-sputtered cells began when we started to use planar magnetron reactive sputtering to deposit the CdS adjacent to the junction. The planar magnetron source was used because of its promise for providing off-stoichiometric CdS with a lower resistivity than we achieved with the cylindrical magnetrons. However, the planar magnetron only produced a resistivity reduction in the three-to-ten range.⁴ It is hard to believe that this is cause of the improved cell performance. The planar magnetron also

FIG. 19 Theoretical estimate of the influence of the minority carrier diffusion length and the Cu₂S coating thickness on the short circuit for a front walled planar cell. Reflectance, $R(\lambda)$, at rear electrode is taken to be measured dependence for sputtered Nb deposited onto a Corning 7059 substrate.

provides a factor of three larger deposition rate because of the more directed coating flux. Experiments in which the planar source was operated at 1/3 the normal deposition rate have been inconclusive. The improvements in performance of the cells may in fact have nothing to do with the planar source per se. This point will be explored at a later date.

The Cu_2S layers in the all-sputtered cells deposited to date have been 150 nm thick. The maximum short circuit current achieved thusfar of 12 mA/cm^2 could become about 15 mA/cm^2 with an optimized antireflection layer. This is seen in Fig. 19 to imply an L_n of between 100 and 200 nm, which is a reasonable value, typical of that achieved in the conventional cells. This provides additional evidence that the junction recombination losses are negligible and that the performance of the sputtered Cu_2S layers can be comparable to that for ion exchange type Cu_2S . Thus performance is being approached in the all-sputtered cells which may be near the limit for a truly planar device of the type being examined. An important observation in this work is that the control in deposition parameters which is afforded by the sputtering process may ultimately make it possible to deposit high performance cells with no requirement for post-deposition heat treatments.

Future work will concentrate on optimizing the Cu_2S thickness and improving our deposition procedures so that J_{sc} of 12 mA/cm^2 or greater can consistently be achieved in combination with maximum values for the other cell parameters. Attention will be given to the use of antireflection layers and to small scale surface roughness which could increase the short circuit currents above the planar cell values given in Fig. 19. It is also planned that the back-wall type all-sputtered cells will be fabricated. The objective would be to provide an alternative cell configuration for use in evaluating the performance of the sputtered layers, and also to provide a device configuration that would offer greater protection for the Cu_2S layer and that therefore might improve the cell stability.

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